SLAC NATIONAL ACCELERATOR LABORATORY

Solid-State Powered X-band Accelerator

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ABSTRACT

In this report we disseminate the hot test results of an X-band 100-W solid state amplifier chain for linear accelerator (linac) applications. Solid state power amplifiers have become increasingly attractive solutions for achieving high power in radar and maritime applications. Here the performance of solid state amplifiers when driving an RF cavity is investigated. Commercially available, matched and fully-packaged GaN on SiC HEMTs are utilized, comprising a wideband driver stage and two power stages. The amplifier chain has a high power-added-efficiency and is able to supply up to ~1.2 MV/m field gradient at 9.2 GHz in a simple test cavity, with a peak power exceeding 100 W. These findings set forth the enabling technology for solid-state powered linacs.

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1. Introduction

Overwhelming demand for high energy particle beams in physics, medicine and other areas of science has substantially stimulated the application of linear accelerators (linac) in rapidly growing technologies including X-ray diagnostics and therapy, geophysical and terrestrial imaging [1], [2]. One important aspect of conventional linear accelerators is the driving method, usually comprising high power microwave (HPM) sources such as klystrons [3], [4]. For high gradient linacs, the field gradient would exceed 30 MV/m, with high surface fields. However, conventional drivers for linacs capable of producing MW of power are not suitable in practical terms for airborne applications due to weight and sophistication of klystron systems. An attractive approach for alleviating this challenge, especially for moderate to low-gradient linacs, is the use of solid state power amplifiers (SSPAs) to drive the linac. Such a technique promises a cheap power with large scale integration capability, the absence of high voltage power supplies and significantly lower weight for airborne applications compared to conventional drivers [5]. A possible deployment for such solid-state accelerator would be on a low-earth orbit (LEO) satellite for X-ray imaging, surveying or any other high energy scientific experiment. In Fig. 1 an example of a linac on a satellite is depicted conveying the concept of a high energy beam that would interact with the earth's magnetic field, with application to weather forecasting and geomagnetic research in general [6]. In principle, the design of a solid-state driven-linac is similar to conventional linac with only a few variations to accommodate solid-state technology [7].

Against this background, we explore a novel scheme for a modular X-band solid-state based accelerator. The concept of solid-state driver has been proposed in [8] whereby an RF cavity is being fed with modular RF power amplifiers and a power combining circuitry. It was already shown in [7]–[10] , that high pulsed RF power can be generated by operating many of the high power RF-modules and some experimental studies of generation of few tens of KW as corresponding to an electric field gradient of tens of MV/m. Although such concept may offer means to potentially lower fabrication cost, provide high integration, better thermal management, better reliability, and achieve graceful degradation compared to traditional high power vacuum technology (e. g. klystrons) for certain applications, it is still debatable whether such solid state technology can compete with the existing vacuum electronics technology in terms of scalability, efficiency, effective cost and maturity of the respective design.

From the power amplifier circuity level, Silicon-Carbide (SiC)-based junction gate field-effect transistors (JFETs) such as Gallium Nitride (GaN) high electron mobility transistors (HEMTs) have been typically utilized thanks to their large band gaps and capability of handling high RF power [11]–[14]. A significant advantage of the GaN on SiC- HEMT is the fast and robust body diode that enables an operation without additional freewheeling diodes or circulators (for flyback elimination) [14] . At low current levels, the transistor operates in a linear regime providing a constant drain current independent of pulse length and drain voltage. However, at very high current levels, the drain current starts to degrade due to self-heating effects with increasing drain voltage and pulse length. Less current degradation is expected during RF operation (namely graceful degradation), in particular with highly efficient push-pull switch mode power amplifier topologies. In terms of power added efficiency (PAE), class F or (inverse-F) [15] power amplifier is often considered since it provide the lowest possible power dissipation at the drain path and therefore typical PAE exceeds 50% at saturation level for optimized loads (although being narrow band) [15], [16].

In this document we report results of testing a modular 100 W solid state amplifier based on GaN off-the-shelf packaged GaN transistors, achieving a gradient of ~1.2 MV/m.

Fig. 1. Conceptual application of a solid-state accelerator in space. (Left) Earth's magnetic field lines. (Right) A solid-state accelerator shooting a high energy beam that interacts with the earth's magnetic field for applications involving geomagnetism, geophysical and terrestrial X-ray imaging, for instance.

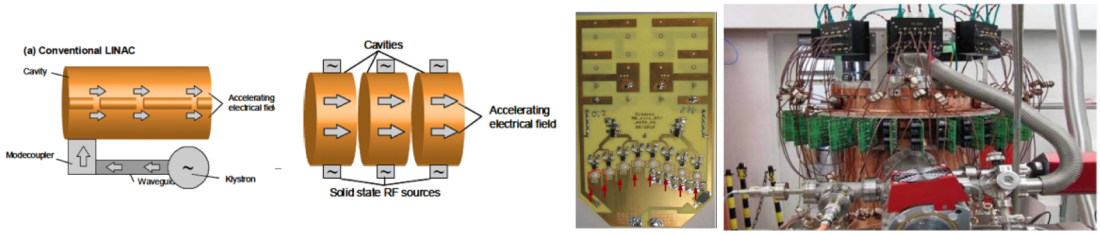

Fig. 2. (Left) Conventional linac drive (klystron) versus solid-state driver concept. (Right) A modular solid-state power amplifier that is used to power a UHF cavity, in which field gradient is ~15 MV/m with 10000 W peak power [8].

2. Amplifier chain test

In this section, we report the assembly and test of a 100-W peak power amplifier chain operating at 9.3 GHz, with a resonant cavity as a load, as depicted in the schematic in Fig. 3. We have utilized two types of GaN matched and full-packaged transistors from RF Lambda and Cree [17], [18], which constitute the driver stage and the output stages (two) respectively. The datasheets and information can be obtained in [17], [18].

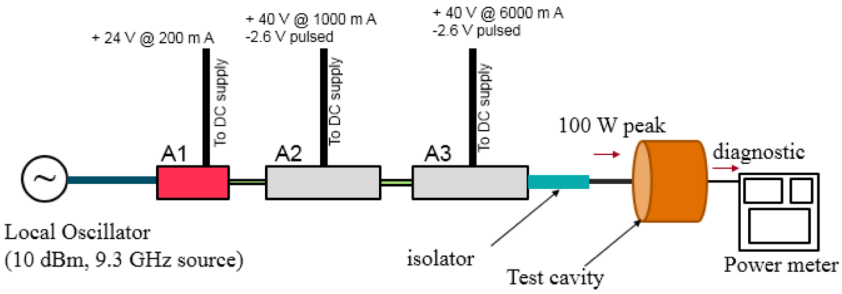

Fig. 3. Assembly and test configuration of the proposed 100-W peak power amplifier. The input stage A1 is a high gain low power driver (23 dB gain, 32 dBm maximum output power). The two power stages A2 and A3 are identical and they have lower gain and can reach a saturated power level of 51 dBm.

2.1. Stage A1 test at 9.3 GHz

The test of the A1 stage requires a DC power supply of V_{dd}=+24 V. The schematic of the test setup is as shown in Fig. 4, in which a local oscillator is feeding the driver amplifier, and the output is measured using a power meter. In Fig. 5, the

output power and gain are shown versus the bias voltage for two different frequencies of interest, namely 9.3 GHz and 11.4 GHz. The achieved gain at 9.3 GHz with V_{dd}= 24 V is 23.5 dB, with a maximum output power of ~32.5 dBm, whereas for 11.4 GHz and the same bias the gain drops to ~18 dB.

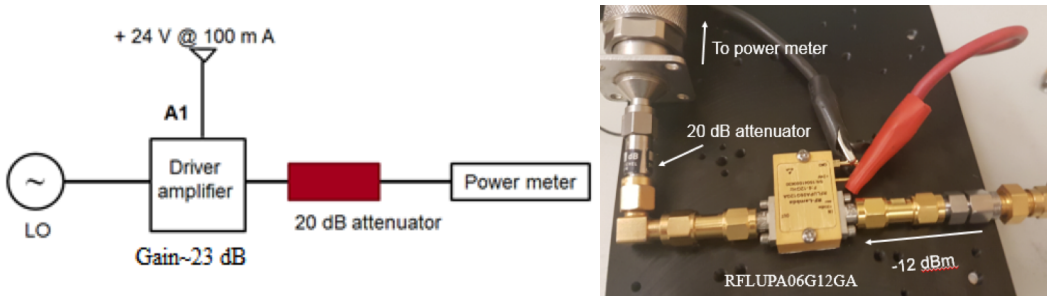

Fig. 4. Schematic of the test setup of the first stage amplifier.

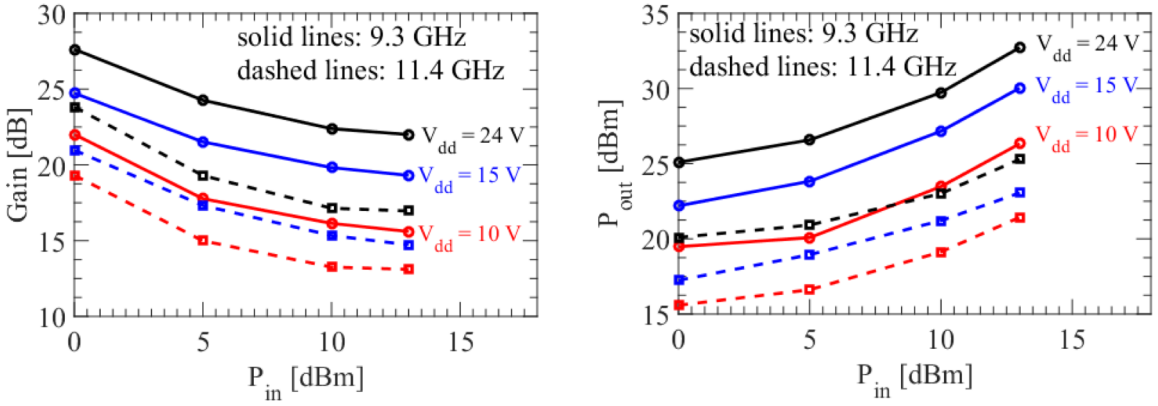

Fig. 5. (Left) Gain and (right) output power of the first stage amplifier versus drain bias voltage (DC) at different frequencies.

2.2. Coupling of power to 11.4 GHz cavity

The driver stage in Section II.A is utilized to investigate the response of a resonant cavity load. As can be seen in Fig. 6, the drive stage is coupled to an 11.4 GHz pillbox cavity using with a directional coupler to diagnose the amount of reflected power. In Fig. 7, the power reflected from the cavity is measured and shown as symbols varying as a function of frequency for different bias voltage levels. The input power is -12 dBm. In addition, a Lorentzian fitting formula is superimposed in Fig. 7 which has the following form

$$P_{\text{out}} = P_d - \frac{P_L / Q_0^2}{(\omega - \omega_0)^2 + \frac{1}{Q_0^2}} \qquad (1)$$

where P_d is the baseline power (reflected from the cavity), P_L is the estimated "minimum" reflected power by the load at resonance, Q is the intrinsic quality factor of the cavity, and ω_0 is the resonance angular frequency. The fitting formula agrees very well with the measured response when the loaded Q is ~1900. Note that this is not the highest Q that can be

obtained for this aluminum pillbox cavity. In other words, to achieve the expected Q for this cavity (~3800 from simulation at critical coupling) attention must be paid to the quality of the electrical contact between the cavity and the cap as well as the surface finish of the metal especially for aluminum (refer to Sec IV for details).

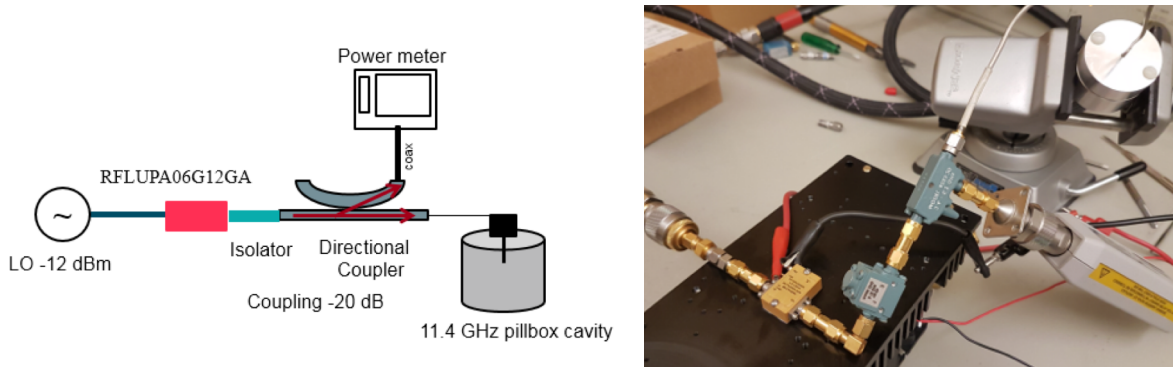

Fig. 6. Test setup of driving a resonant cavity at 11.4 GHz with a high power transistor. The directional coupler has a 20 dB coupling to the power meter.

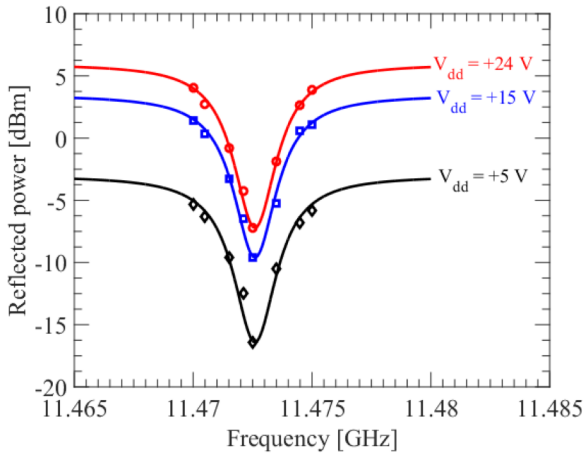

Fig. 7. Normalized reflected power measured from the setup in Fig. 6 shown as symbols, while solid lines represent a Lorentzian fit.

2.3. Stage A2 test

Next, the power stages (A2 as well as A3) are tested. Note that here we have utilized a test board from Cree that has an elaborate drain and gate biasing network. A ~450 µf capacitor at the drain path prevents a short rise time of the pulse, and thus most of the drain current is supplied from that capacitor. In order to mitigate this issue, a longer pulse is required. We have pulsed the gate bias from -5 V (transistor is off, i.e., no drain current), to -2.6 V (pinch of voltage is ~2.9 V, and at -2.6 V the drain current is ~1000 mA under idle condition, i.e., no RF drive). Therefore, by pulsing the gate between -5 and -2.6 V we have achieved pulsed operation of the transistor.

The test schematic of the power stage is shown in Fig. 8 and a broadband low-barrier Schottky diode detector (LBSD) detector model Keysight 8473B is used for power measurement. The result of the test is depicted in Fig. 9. The small signal

gain measured for this stage up to 13 dB for an input power of ~13 dBm, at 40V drain bias. The gain is expected to saturate at roughly 10 dB for ~40 dBm input power. In Appendix A, some important remarks about the safe operation modes of the transistor are reported along with simulation results of the transistor from the model provided by Cree.

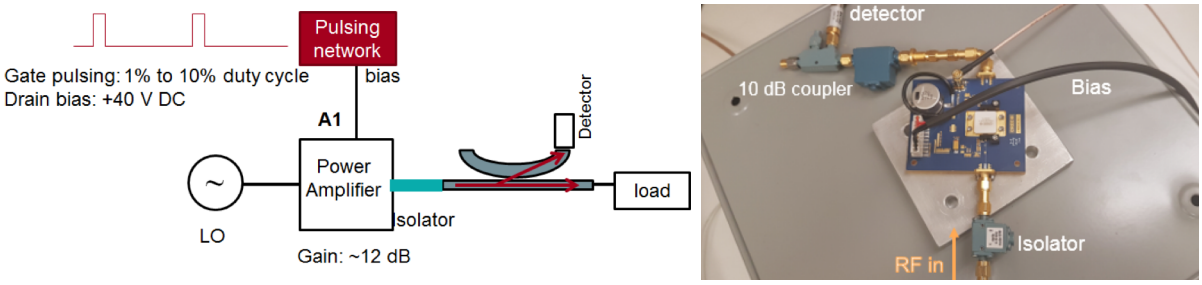

Fig. 8. Test setup of the power amplifier stage, using the test board. The biasing network provides a pulsed gate with variable duty cycle.

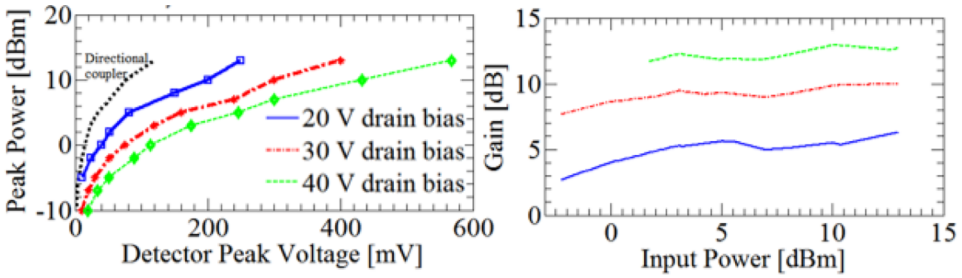

Fig. 9. Measured response of the output stage. (Left) Peak power for different drain bias (DC). (Right) The measured gain for the same.

2.4. Full chain test

The three-stage amplifier chain test is reported here. The maximum saturated output power achieved was 145 W, in agreement with device datasheet. The assembly of the chain is shown in Fig. 10, where the output stage is coupled to a detector by a 10 dB coupler. The attenuator at the output stage of the chain yields approximately 22.1 dB of attenuation. Therefore the coupled power to the detector is ~32.1 dB lower than the power coupled to the broadband load. The insertion loss of the chain connectors and isolators are ~3.4 dB.

Test 01. In this test we have used a relatively short gate pulse as shown in Fig. 11. The pulse has a narrow peak (~1.5 ms in total width and 60 Hz repetition rate) and does not exhibit a flat top due to the large time constant in the gate path. Nonetheless such short pulse allowed the transistors (in stages A2 and A3) to adequately turn on and off. The output power from the chain is measured to be 46.6 dBm at input power level of 10 dBm, showing an overall peak gain of 36.6 dB (there exists a 3.4 dB insertion loss along the chain).

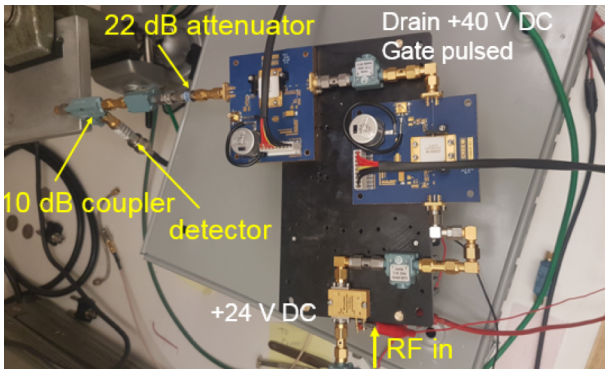

Fig. 10. Assembly of the three stage amplifier chain. Isolators are placed between stages.

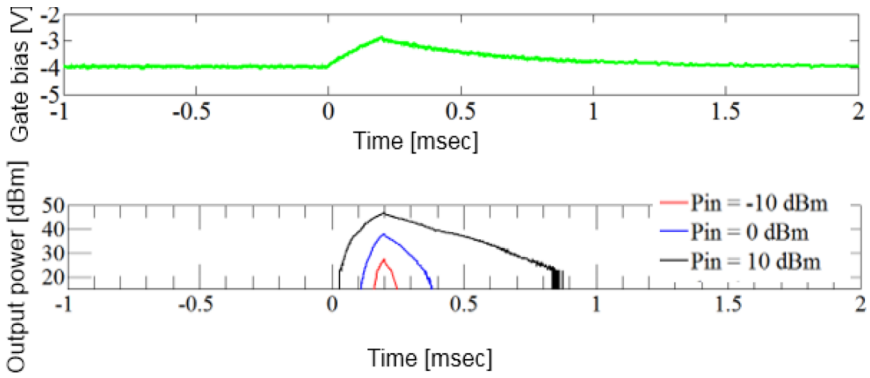

Fig. 11. First test results of the full chain response. (Top) Gate pulse that is strongly affected by the protection capacitors in the test board. (Bottom) Measured power trace for three different input power levels.

Test 02. The second test is performed utilizing a wider gate pulse than the one used in test 01 (~5 ms in total width and 1 Hz repetition rate) and the duty cycle is ~0.5%. The results are shown in Fig. 12 and 13. As the second stage enters saturation, the peak drain currents are measured to be in the order of 7.8 A. The peak power achieved in this test is 50.55 dBm (~113.4 W) for 13 dBm input power and +45 V bias, whereas for drain bias voltage of 40 V the peak output power is ~47.5 dBm. In Fig. 14 we also report the drain current as a function of the input RF power and we see the effect of saturation as the input power approaches 13 dBm. Observe also that the output pulse width is getting relatively wider as the input RF power increases; due to the gate overdrive.

In Table 1, the result of Test 02 of the amplifier chain at 9.3 GHz is summarized. Remarkably, we measured an impressive 35% overall power added efficiency (PAE) with gain of 37.54 dB and a total peak DC current of 8.15 A. Note that the total average power dissipated in the chain at 13 dBm input and +45 V drain current is 23.76 W while the output average power is 0.443 W.

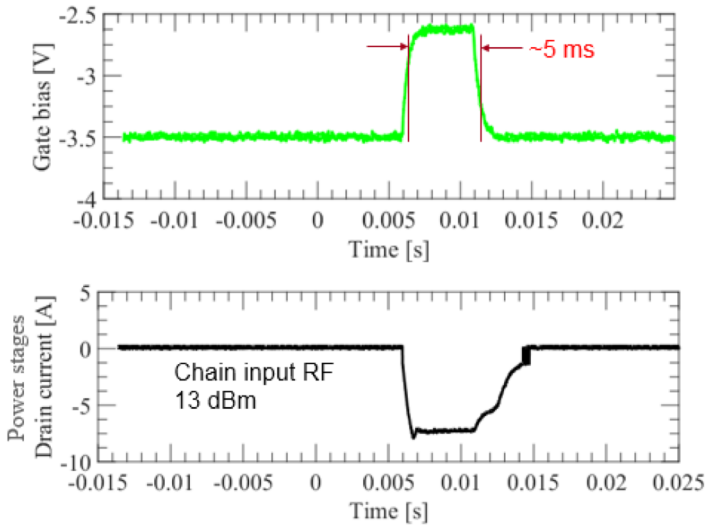

Fig. 12. Second test results of the full chain response. (Top) Gate pulse with a larger pulse width than the one in Fig. 11, with a flat top. (Bottom) Measured drain current for 13 dBm input power.

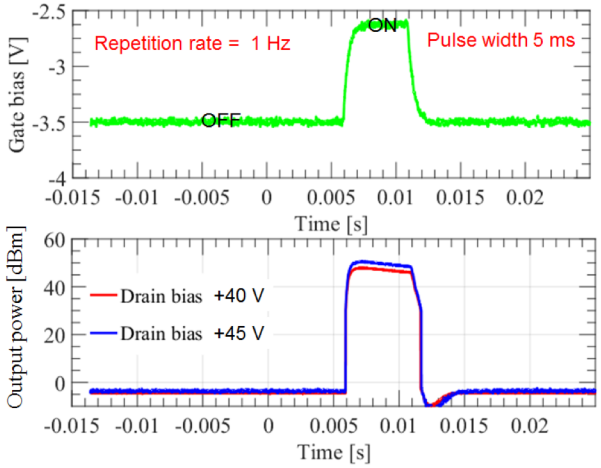

Fig. 13. (TOP) Same as in Fig. 12. (Bottom) Measured output power trace for two different drain bias voltages.

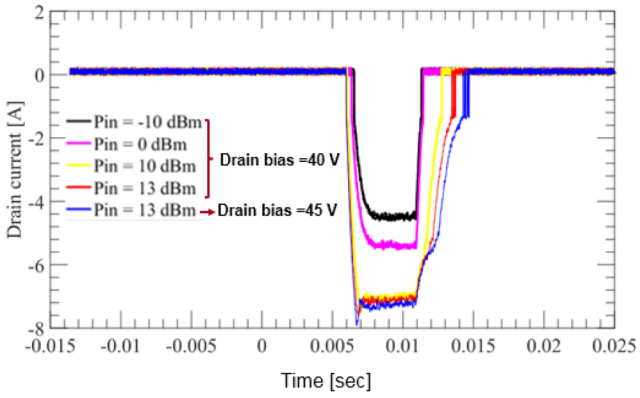

Fig. 14. Measured drain currents for different levels of input RF power and drain voltage.

Table 1. Test results of the three stage amplifier chain at 9.3 GHz

Pin [dBm]	-10 dBm	0 dBm	10 dBm	13 dBm	13 dBm
Drain bias	+40 V, DC	+40 V, DC	+40 V, DC	+40 V, DC	+45 V, DC
Gate bias pulsed	-2.6 V, 5ms	-2.6 V, 5ms	-2.6 V, 5ms	-2.6 V, 5ms	-2.6 V, 5ms
Peak drain current [A]	4.6	5.52	7.48	7.64	7.92
Pout, avg [dBm]	6.376	16.09	23.58	23.95	26.47
Pout, peak [dBm]	29.95	39.75	47.46	47.90	50.55
Max chain gain [dB]	39.95	39.75	37.46	34.9	37.54
3 dB pulse width	4.62	4.67	4.74	4.79	4.82
Overall maximum PAE	0.52%	4.16%	18.26%	19.78%	31.29%

3. X-band test cavity

To demonstrate coupling of 100 W to a resonant load, a pillbox test cavity was fabricated. The cavity diameter and length are 12.5 mm and 10 mm, respectively and designed to operate with the TM_{010} mode. A coaxial probe is used to critically couple the power to the cavity and the probe diameter and length are 2.2 mm and 1.25 mm. The cavity has a weakly coupled port for diagnostics. Note that the copper cavity has to be "crushed" to achieve a good electrical contact and provide a high Q factor (similar to expected value from full-wave simulation).

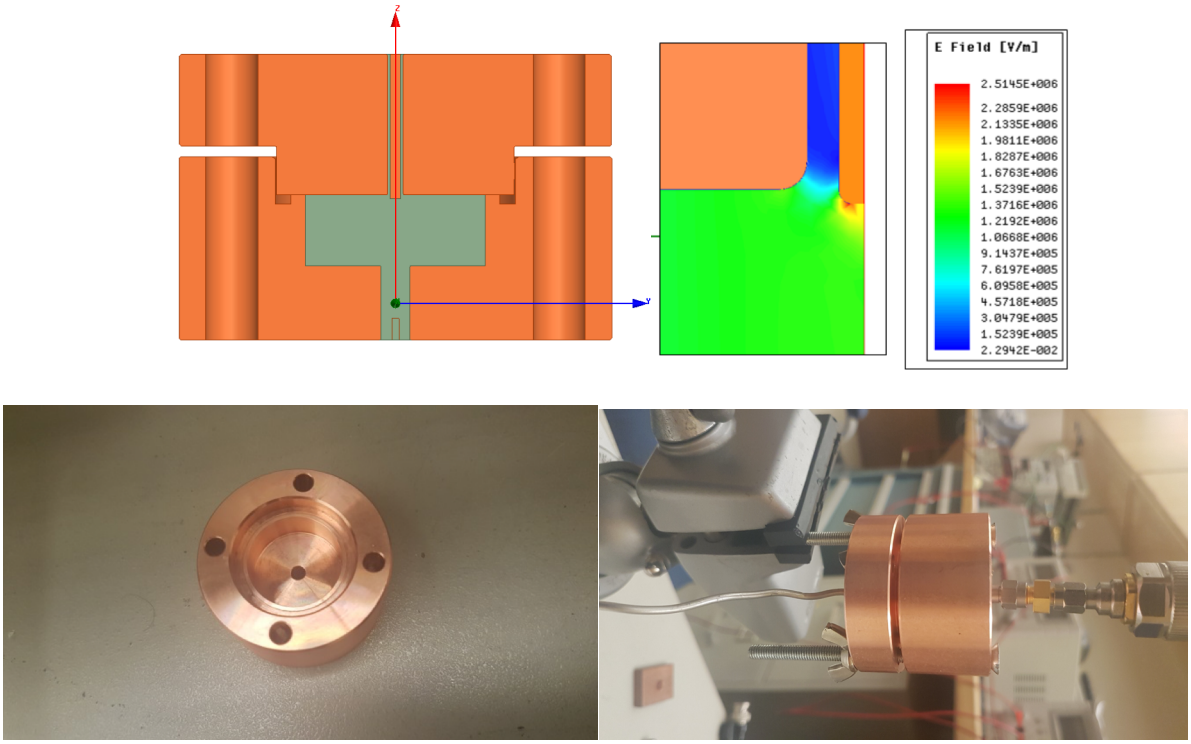

Fig. 15. (Top left) Cross section of a copper Pillbox cavity designed at 9.2 GHz. (Top right) The calculated field gradient under critical coupling showing a field gradient of ~1.2 MV/m with a hot spot around the probe of about 2.5 MV/m. The cavity is critically coupled from one side and weakly coupled from the other side using coaxial probes, so that the loaded Q factor is ~3200.

3.1. Cavity cold test

The cavity was cold tested using HP 83250 VNA. The achieved S11 was < -40 dB and the weakly coupled port S21 was ~-30 dB, as seen from the measured data in Fig. 16. The estimated loaded Q factor was in the order of 3200 under critical coupling, therefore the intrinsic Q factor is ~6400.

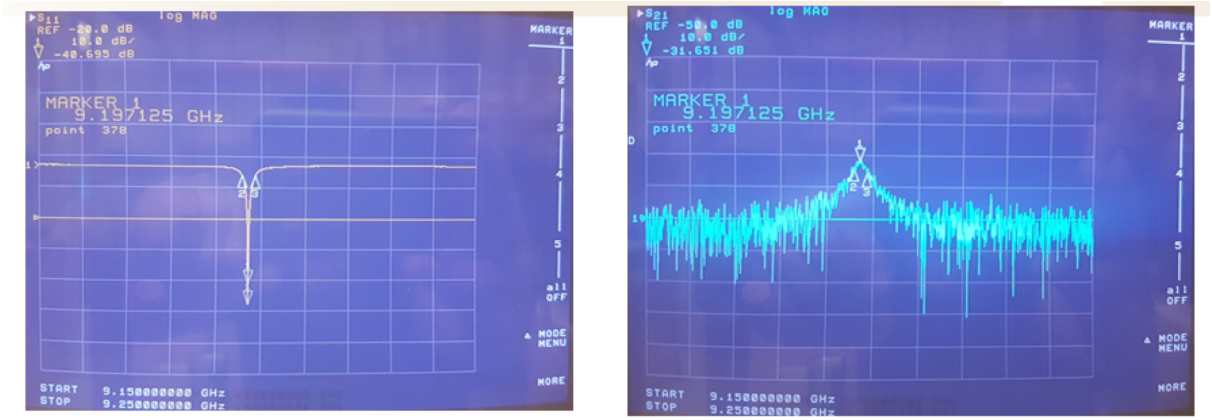

Fig. 16. (Left) and (Right) are measured S11 and S21 respectively of the pillbox test cavity in Fig. 15.

4. High power test

The high power chain was coupled to the test cavity and tuned to the resonance of the cavity. We have incorporated isolators to prevent reflection back to the chain and also included directional couplers for diagnostics. The measured incident and reflected power from the cavity are depicted in Fig. 17. Note that operating off resonance leads to measuring almost equal levels of incident and reflected powers, since the cavity behaves as a short circuit.

4.1. 50 dBm peak power coupled to test cavity

In Fig. 17 we show the incident and reflected power traces observed at the detectors for different operation conditions. The reflection coefficient measured is less than 27 dB; measured by observing the difference between incident and reflected power at 9.2 GHz. Operating off resonance (purple curve in Fig. 17) would result in almost equal incident and reflected power.

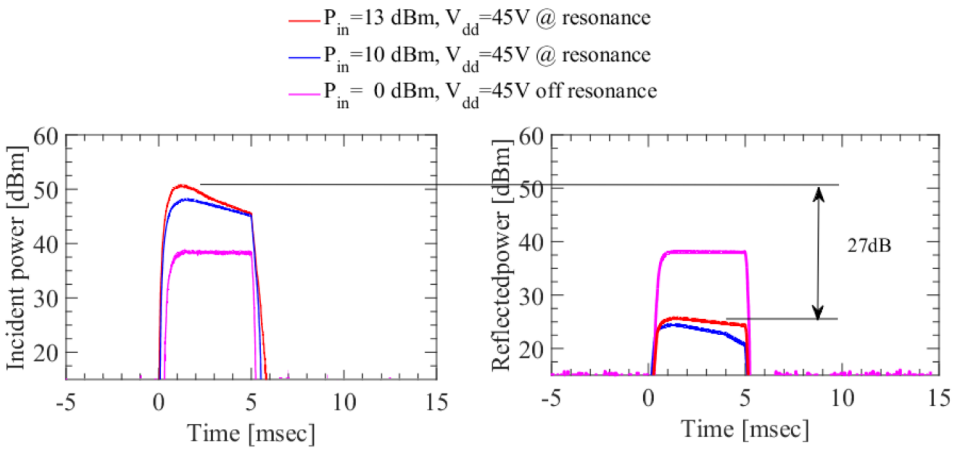

Fig. 17. Traces of the (left) incident and (right) reflected power from the cavity. Note that the measured reflection coefficient is <-27 dB.

4.2. Loaded Q factor hot test

The loaded Q factor under critical coupling is measured from hot test by sweeping the chain input frequency around resonance. The achieved loaded Q factor is ~3450, as seen from the reflected power in Fig. 18. For these conditions, we plot the field gradient at the resonance scaled with the input power in dBm in Fig. 18. The field gradient is calculated using HFSS for different input power and the same loaded Q obtained from measurements. Note that the field gradient exhibits a strong enhancement near the edges, while surface fields can go up to 1.8 MV/m for 50 dBm input power at 9.3 GHz.

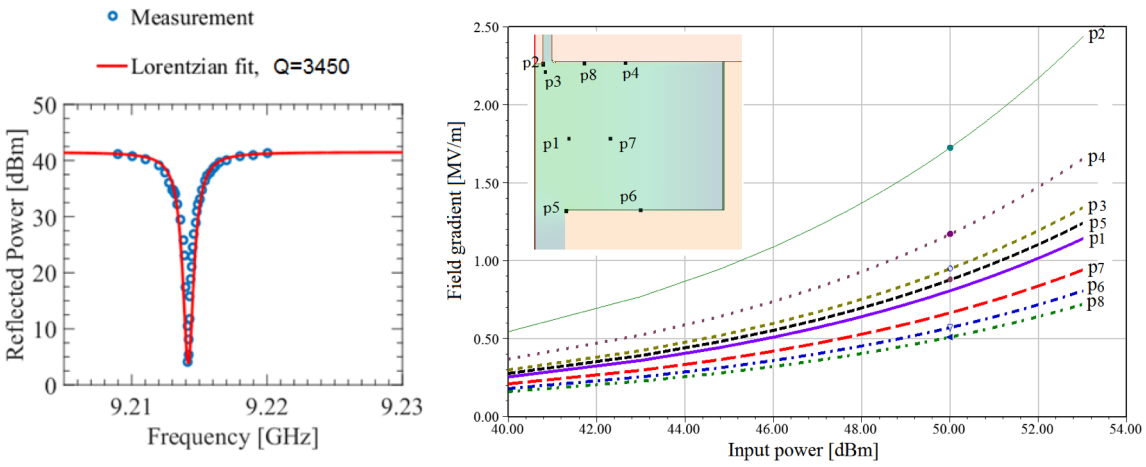

Fig. 18. Measured reflected power from the cavity varying the chain input frequency. The input power is 0 dBm. (Right) The expected field gradient scaling with input power at different points inside the cavity where field enhancement is expected, calculated using HFSS.

4.3. Breakdown test

RF breakdown is a critical aspect in the development of high power microwave sources and next generation linear accelerators since it limits the accelerating gradient of the linacs. The surface of a cavity as well as the probe has imperfections caused by grain boundaries, scratches, bumps, as well as the pointy tip of the probe etc. The electric fields at these small imperfections can be greatly enhanced compared to the gradient that is theoretically calculated. Breakdown manifests when a plasma

discharge is generated in the cavity. This is almost always associated with some of the cavity walls being heated until it vaporizes and the gas is then ionized by field emission. The exact mechanisms are still not well understood; though some theories and explanation was reported [19]–[22]. A typical breakdown threshold for air at sea level pressure (~760 torr) at room temperature (293 K) ranges from 1.8 to 3 MV/m depending on the air contents (gases, water, etc). In addition, the breakdown threshold is also strongly dependent on the pulse width and the duty cycle of the RF power. Typically, the cavity walls dissipate almost all the incident power under critical coupling and the temperature rises accordingly. This takes place right before a breakdown event. Also breakdown depends on the dark current.

To observe breakdown events, we monitored the reflected and transmitted power from the cavity. The breakdown test was performed by coupling 100 Watts to the cavity. A typical breakdown event would lead to a significant rise of the reflected power. An image captured during the breakdown event is shown in Fig. 19 where also the reflected power trace is shown. After breakdown, the Q is re-measured and we observe tangible degradation of the coupling (from -38 dB to -24 dB) while the Q factor remained the same. The reason behind that is potential damage to the probe from breakdown spark (X-ray). Note that the reflected power is less than the expected 50 dBm due to the power absorbed by the plasma forming inside the cavity.

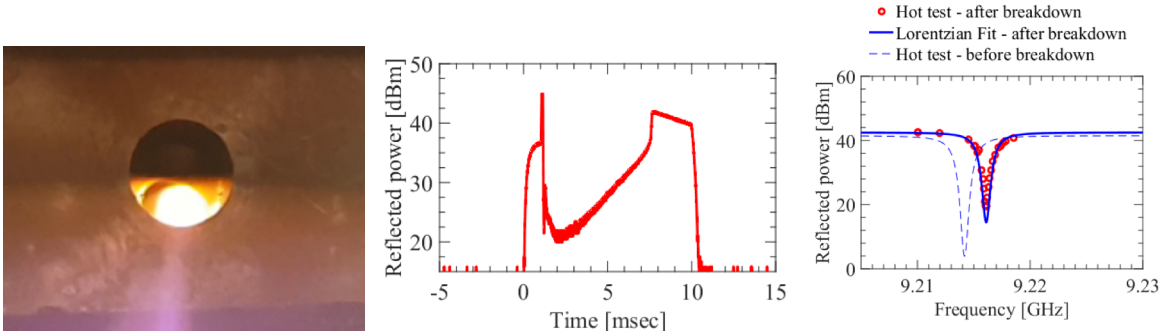

Fig. 19. (Left) An image of the forming plasma inside the cavity during breakdown event. (Middle) Reflected power from the cavity during breakdown. (Right) Change of the Q factor and the coupling post-breakdown.

5. Amplifier design

In this section we report our preliminary investigations in designing and prototyping X-band solid state high power amplifiers using commercial dies. Unlike the work reported in Sections 2 through 4, here a circuit based design is carried out from topology level. We utilize an X-band unmatched die operating up to 26 GHz, since to our knowledge there is no commercially available, matched GaN transistors capable of producing 100 W at 11.4 GHz. Therefore, matching circuits as well as harmonic tuning has to be implemented. We report here a brief description of the circuit and some of the present and future work that is carried out at SLAC for producing solid state based power. A typical circuit schematic of the single stage, 90 W amplifier is shown in Fig. 20. All designs were developed using Keysight ADS. The basic elements of the circuit are designed as follows:

1. Input matching network: The matching network is designed in order to provide the transistor with an input optimum simultaneously matched impedance of 0.086+j0.06152 Ω. The matching also requires a biasing network (bias-Tee) with a RF suppression of at least -30 dB.
2. Output matching network: the output matching is designed to provide an output optimum simultaneously matched impedance of 0.193+j2.326 Ω, and the seen impedance at the drain toward the load at the second harmonic should be below 5 W in magnitude, while the same at the third harmonic should be larger than 1000 Ω in magnitude.
3. Bond wires are simulated using HFSS.

From circuit simulations (left plot in Fig. 21), the achieved gain for the fundamental frequency 11.4 GHz is around 12.5 dB and maximum output power achieved was 48 dBm at 8.5 dB of gain. The maximum power added efficiency (PAE) reached ~35%. Full-wave simulations using HFSS software were also carried out using Momentum and ADS CoEM simulations and there was a tolerable ~10% decrease in the gain; including models of the bond wires, see Fig. 21 on the right. This has also included some fine parameter optimization in the EM simulations due to the inaccuracies of the circuit model to capture radiation losses and bending effect.

The layout of the final amplifier in which the matching circuits are implemented in microstrip technology is shown in Fig. 22. The amplifier is implemented on a Roger 4350B substrate (height of 1.52 mm and dielectric constant of 3.48). Monte Carlo simulations are shown in Fig. 23 when the widths of the microstrip lines and other dimensions are varied randomly within 5% of the nominal design.

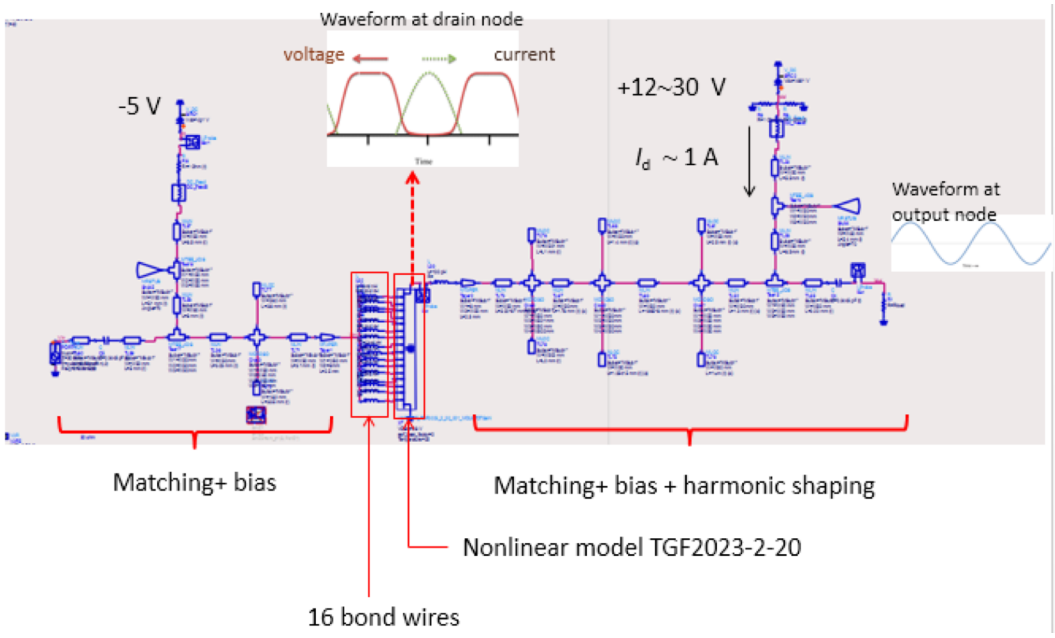

Fig. 20. Typical matching circuit and harmonic tuning of a 90-W amplifier incorporating un matched die as well as bond wires.

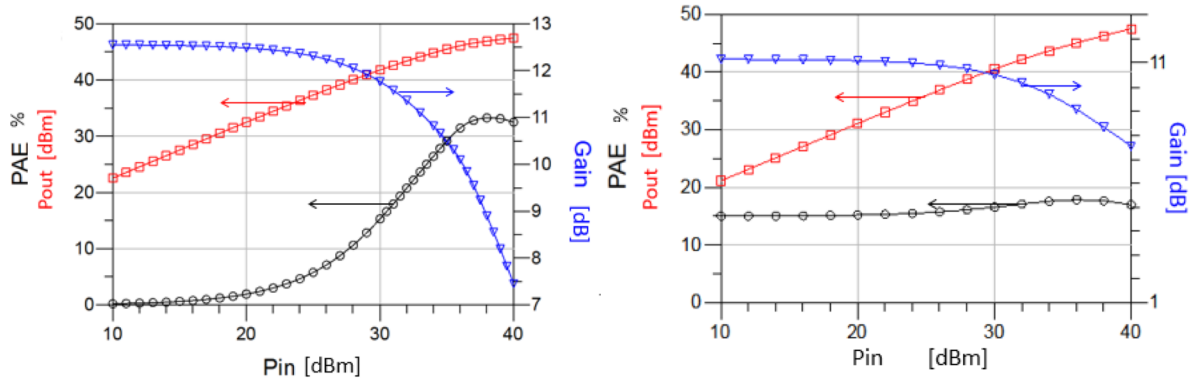

Fig. 21. (Left) Performance of the single stage amplifier designed using ADS. (Right) The same performance, but after optimizing the matching circuits using full-wave simulation.

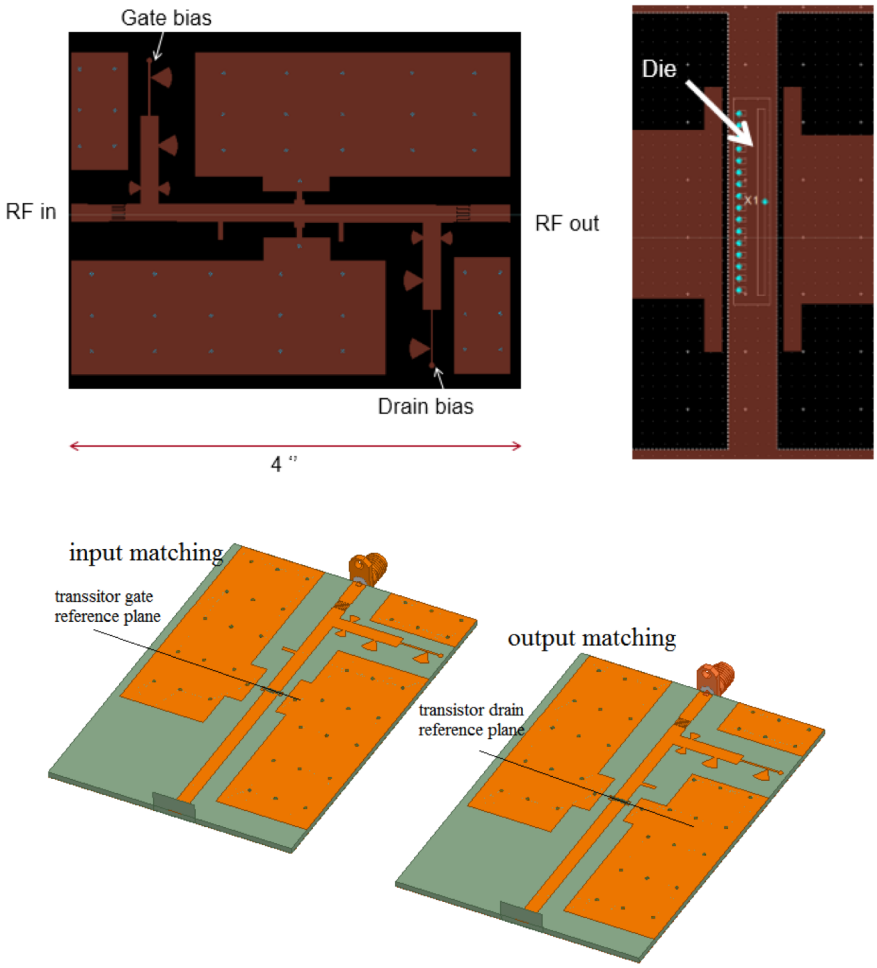

Fig. 22. (Top left) Final layout of the amplifier. (Top right) Zoomed-in layout showing the die placement. (Bottom) Layout of the

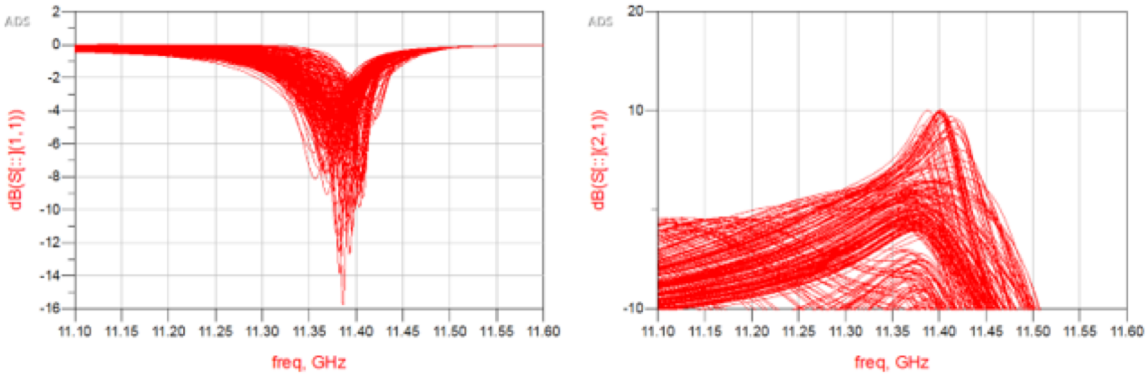

Fig. 23. Monte Carlo simulations showing the magnitude of S-parameters from the amplifier varying only the input matching network tolerances by 5%.

6. Conclusion and future work

We have performed testing of a three stage chain of X-band solid state amplifier capable of producing in excess of 100-W of peak power. We designed a test cavity made of copper that has a loaded Q of about 3400 in which we reported good agreement between full-wave simulations, cold test and hot test experiments in measuring the Q factor. Such high power produced by the solid state source has been coupled to a test cavity inside which the field gradient reached the level of 1.2 MV/m. We also reported a breakdown event at which we show a significant rise in the reflected power.

There are several outcomes of this project, (i) design and cold/hot test of a pillbox cavity which showed good agreement between simulations and measurements, (ii) At least 100 W of peak Power is successfully produced and coupled to the cavity, and (iii) Pulsing the amplifiers variable pulse length and duty cycle is achieved in order to allow fine control on the average power produced as well as potentially finding the best conditions for operating a linac based on solid-state sources.

The future effort in this project will be dedicated to, (i) Bond-wiring and testing the designed class-F 90 W amplifier, (ii) designing a practical linac cavity (nose cone) cell to enhance the field gradient, and (iii) optimizing the solid state source for efficiency, output power and size, and potentially designing a MMIC amplifier board having 40 dB gain and at least 100 w. The application of solid state source would also lead to utilization in RF guns.

Appendix A

The performance of a solid state demo amplifier is evaluated here using the simulation tool ADS. The transistor used is a GaN on SiC HEMT with model number CGHV96100F2. The date provided herein is based on simulations on the model provided by Cree, and provides an insight into the safe operation limits of the transistor.

Here we investigate the performance of a two identical cascaded power amplifier stages. Some important remarks about of the current and power ratings of these stages are as follows:

- The maximum rated drain current is 12A (peak or DC) for reliable operation (26A absolute maximum).
- The maximum drain voltage is 100 V.
- The absolute maximum gate current is ~30 mA. Gate voltage extremes are -10 V and +2 V.

- At 30 dBm input power, the drain current of one stage is ~ 2A and the next stage is ~7 A at the brink of saturation. These levels change slightly with different bias conditions, as seen in the plots below.
- To increase the output power level from the two-stage amplifier at 30 dBm input and -2.6 gate bias, drain voltage can be adjusted above 40 V. This can only provide ~1dB increase in the gain.
- Turing the gate biasing voltage up (more positively) will also lead to increasing the output power. However, the drain current increases linearly. At -2.6 V, the total drain current is ~8.5 A, however at -1 V the total drain current is ~15 A.
- Significant gate current is drawn beyond saturation, i.e., for input power level beyond 20 dBm.
- Theoretical efficiency always has a sweet spot around 30 dBm input RF power, nonetheless the output power can be adiabatically increased around that point by increasing the drain voltage and that would result in slight decrease in the efficiency.

In the following (Fig.A1 through Fig. A7) we provide some simulation results based on the ideal transistor model provided by Cree, and hence we investigate how the output power affects the drain current in the output stages. All simulations are done using Harmonic balance (implemented in Keysight ADS). Unless otherwise stated, currents are in [A] and voltage is in [V].

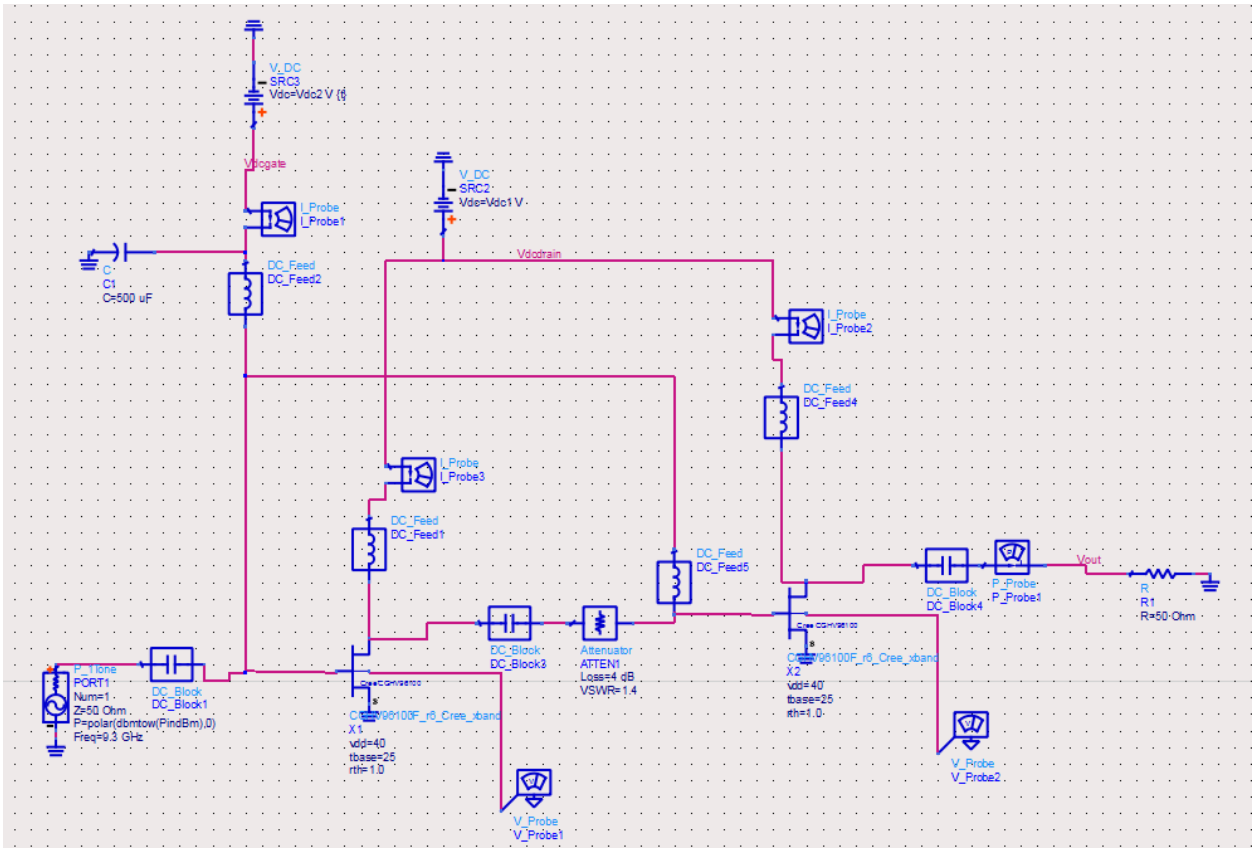

Fig .A1. Schematic of the two stage amplifier.

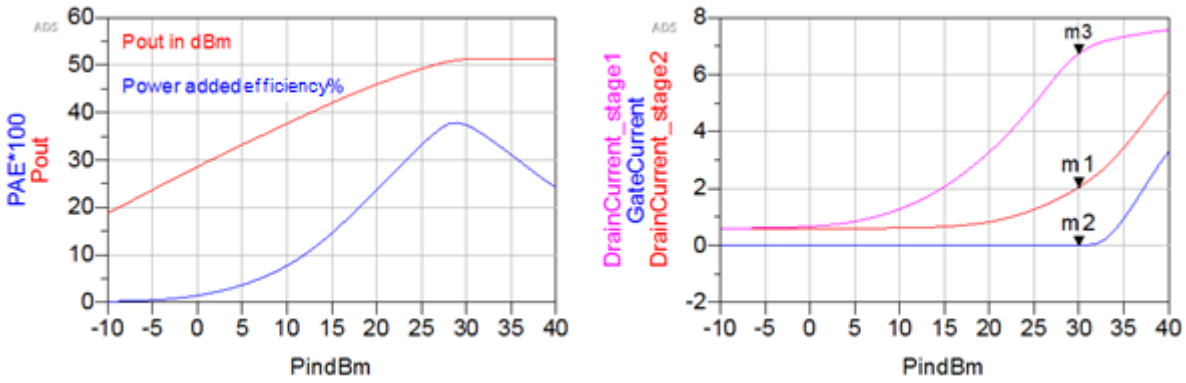

Fig. A2. (Left) Output power and efficiency of the two stage power amplifier. (Right) Gate and drain currents. Drain voltage is 40 V, and gate bias is -2.7 V.

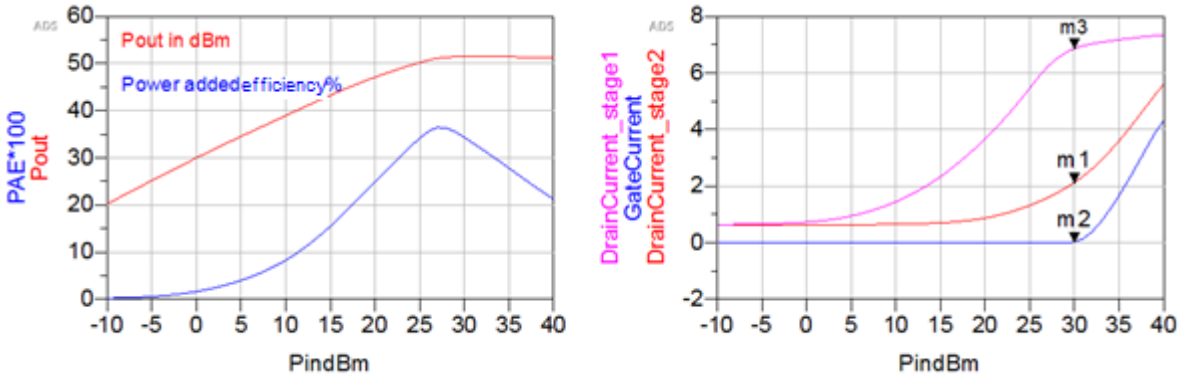

Fig. A3. Same as Fig 1, but here drain voltage is 45 V.

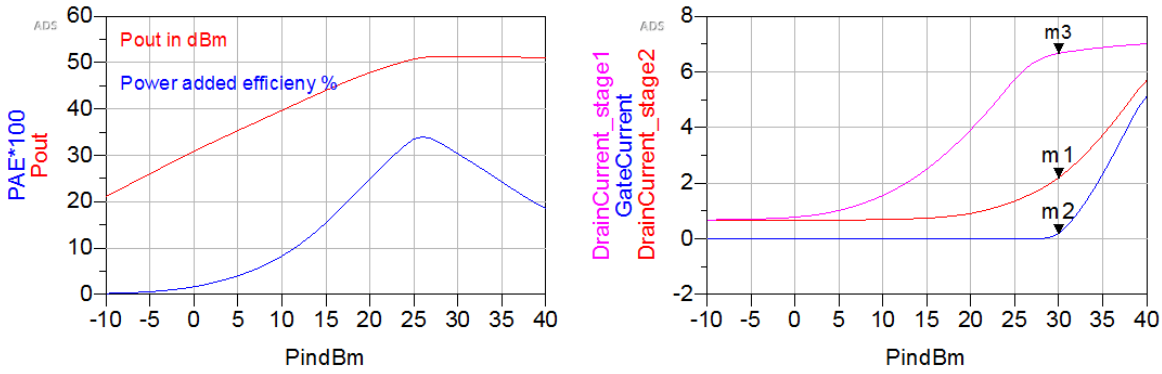

Fig. A4. Same as Fig 1, but here drain voltage is 50 V.

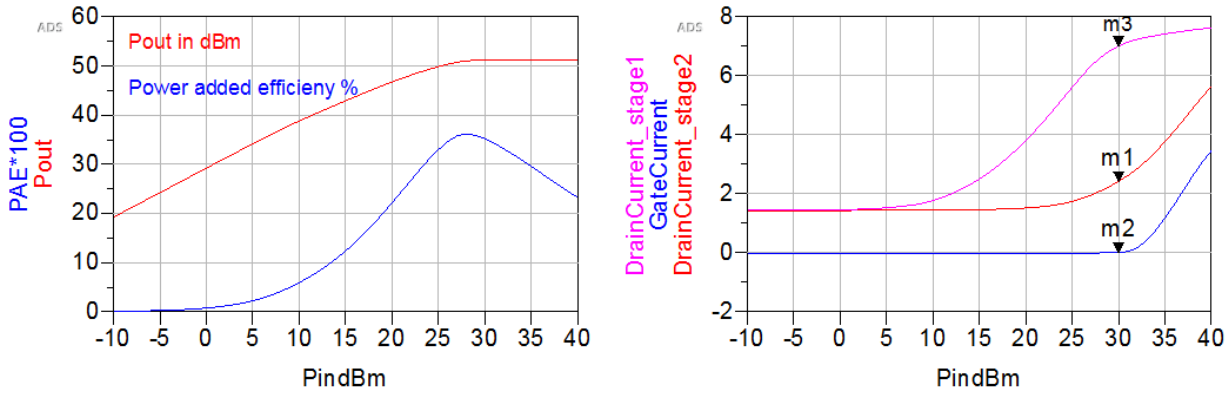

Fig. A5. Same as Fig 1, but here gate in voltage is -2.5 V.

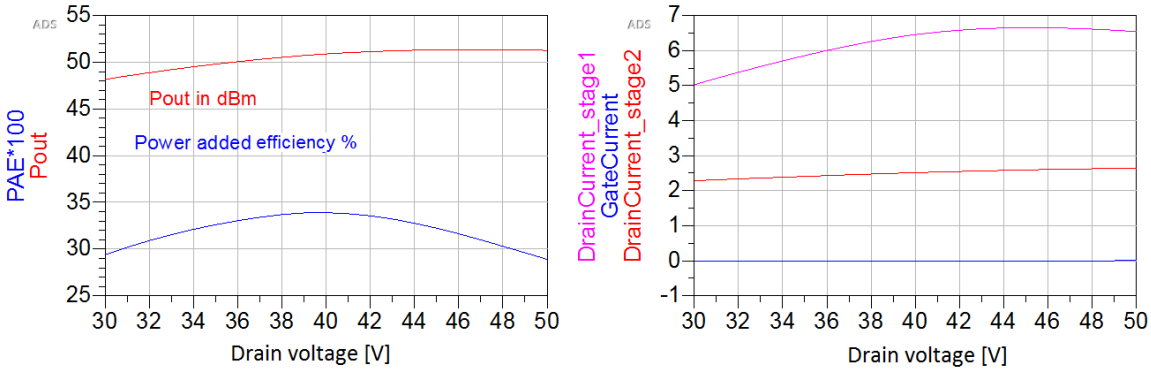

Fig. A6. (Left) Output power and efficiency of the two stage power amplifier varying as function of drain voltage. (Right) Gate and drain currents. Input power is 30 dBm, and gate bias is -2.7 V.

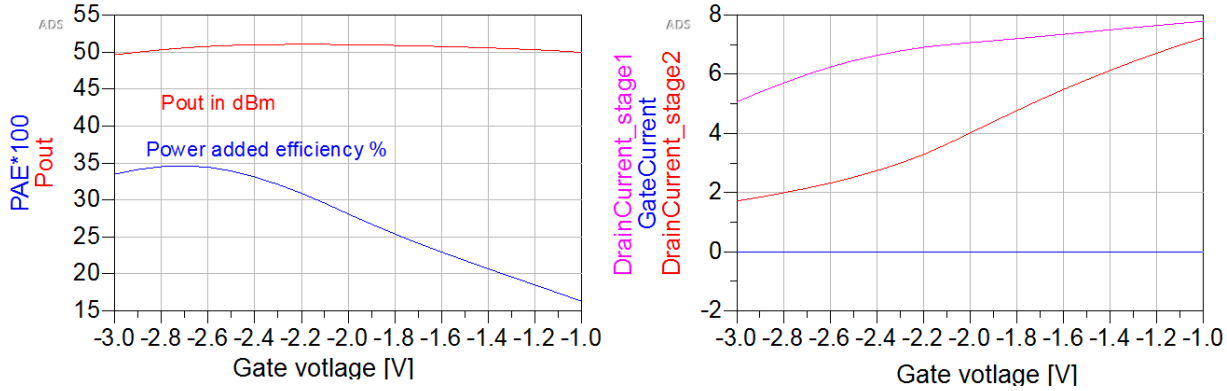

Fig. A7. (Left) Output power and efficiency of the two stage power amplifier varying as function of gate voltage. (Right) Gate and drain currents. Input power is 30 dBm, and drain bias is 40 V.

Appendix B

The 9.2 GHz cavity drawings are shown in Fig. B1 and B2.

Appendix C

The project budget and spending are listed in table C1.

Table C1. Components purchased, and pending.

Components	Supplier/Vendor	quantity	total price USD
Coaxial Isolators, 100 W peak	Raditek	2	178.5
Test board with Cree transistors	Mouser/wolfspeed	2	2361.37
Driver amplifier	RF Lambda	1	5190
Isolators, 10 W peak	Narda	3	846
PCB manfacturing	SF ciruits	15	1423.6
*Connectors, cables etc	Digikey	xx	xx
*Bond wires	Amtech	1	250 - 1000

* Pending costs

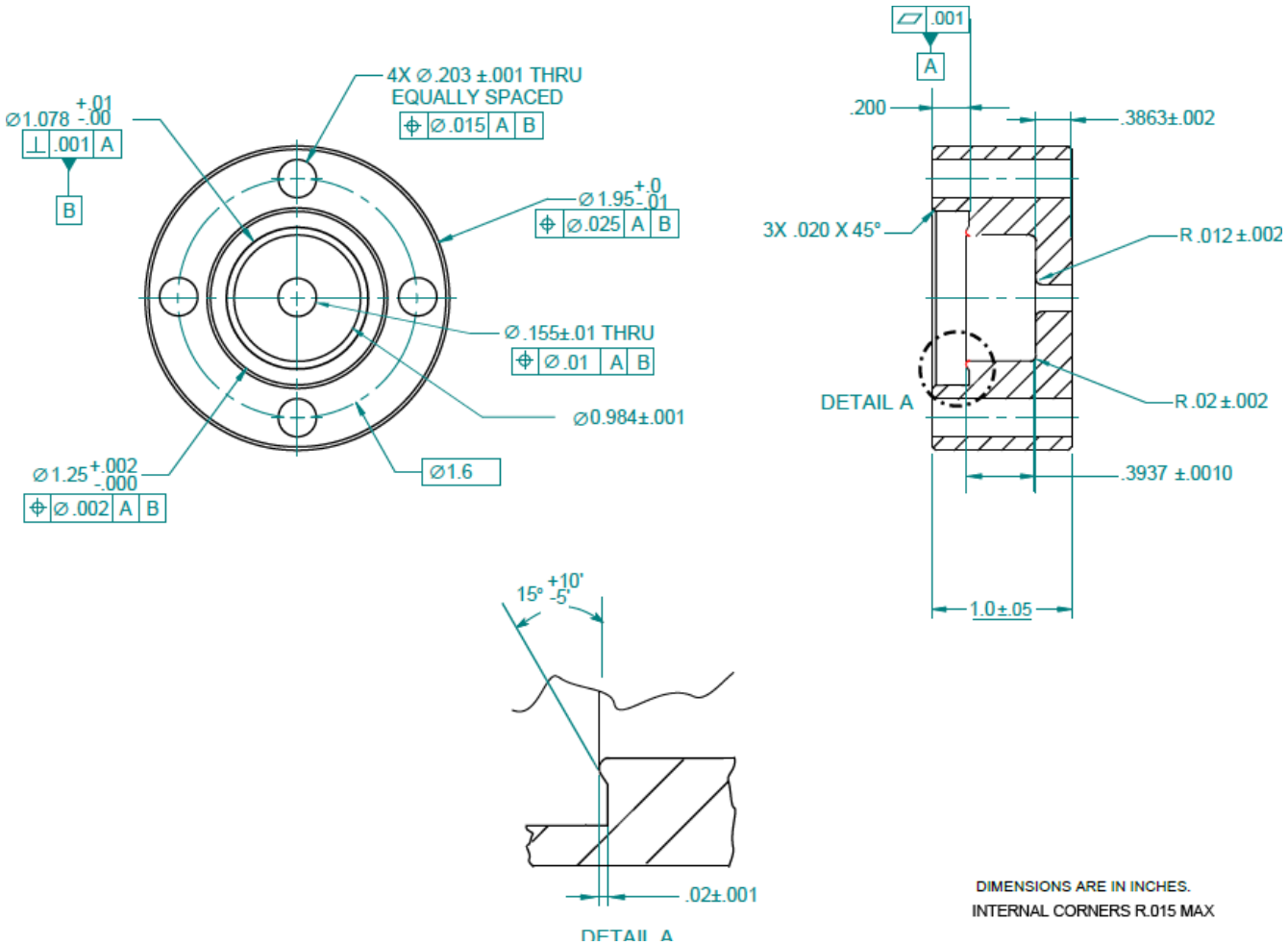

Fig. B1. Mechanical drawing of the test cavity showing all dimensions and tolerances.

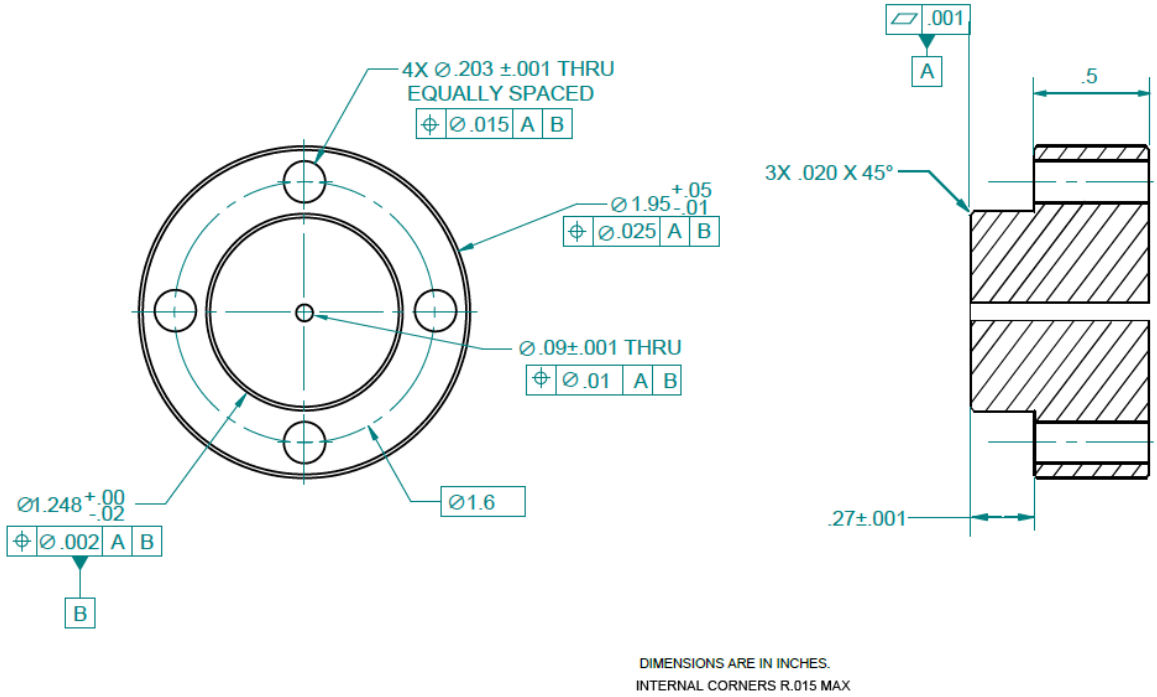

Fig. B2. Mechanical drawing of the test cavity cap showing all dimensions and tolerances.

Appendix D

In Fig. D1 we show how the measured signal from the amplifier chain by taking into account the DC leakage. Note that without a DC blocking stage, we see the data reported in Fig. D1, while adding a DC blocking waveguide results in the data shown in Fig. 17.

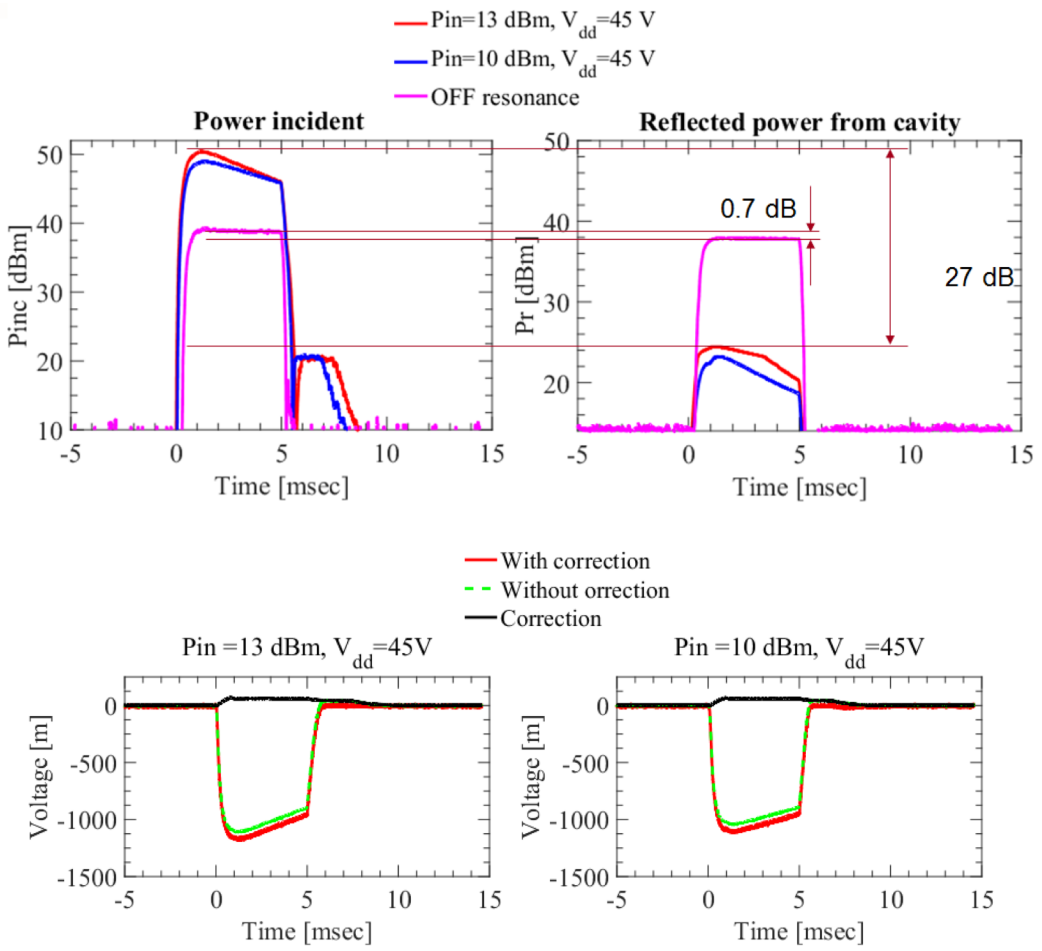

Fig. D1. Traces of the detector voltage with and without DC correction. (Top) Same as Fig. 17, but here there is a DC pusled accompanied byy the RF signal beyond 5 ms that lasts for ~3 ms. (BOttom) The applied correction to the signal, i.e., $V - IR$ where R is the OFF leakage resistance and I is the drain current. The measured leakage resistance is ~7.2 Ohm. The correction value is the DC leakage.

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