FASTBUS AT THE FRONT END

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SUMMARY

A major consideration in the initial design of FASTBUS was its applicability to front end hardware. A number of features have been incorporated to allow the front end designer a large degree of freedom but still maintain compatibility with the standard.

GENERAL

It is this author's view that we are in an era of great change in electronic equipment for high energy physics. Microprocessors and their cousins, the smart controllers, being incorporated in many designs. We are also now seeing devices such as FPLA's, PAL's, etc. becoming larger, faster, and more useful in replacing large amounts of "discrete" logic. On our doorstep are gate-arrays of all types. Smaller (100-1000 gates) in ECL provide the high speed we need; larger (1000-10,000+ gates) in slower logic families can be designed for certain specialized computations for physics.

All these new devices tend to be design intensive. Mistakes cannot be repaired by cutting plating and patching wires where necessary. The engineer must do more careful design checking before committing a design to hardware. At the same time, we are living with budgets which are not expanding. One solution not available is to hire more people to work on these new designs.

Where does FASTBUS fit in? Many papers over the past several years have discussed FASTBUS in terms of the handling and processing of data . To accomodate the microprocessor revolution this bus standard was definitely needed. CAMAC simply could not provide the necessary bandwidth or multiple control capabilities. Standard assignment of bits in control and status registers have been made for software compatibility. A FASTBUS diagnostic language (FDL) is in the final stage of testing and will be released shortly. FASTBUS also provides a well defined mechanical package. The printed board specification is standard commercial tolerances. The board itself rides in the card guide. Front panels are not necessary and can be eliminated if one feels the cost savings merit it. The voltages specified are standard. The power supplies are not part of the card cage specification so the user may tailor them to the specific system. FASTBUS fits all around the users design providing standard building block and frees the designer to concentrate on unique parts of the system.

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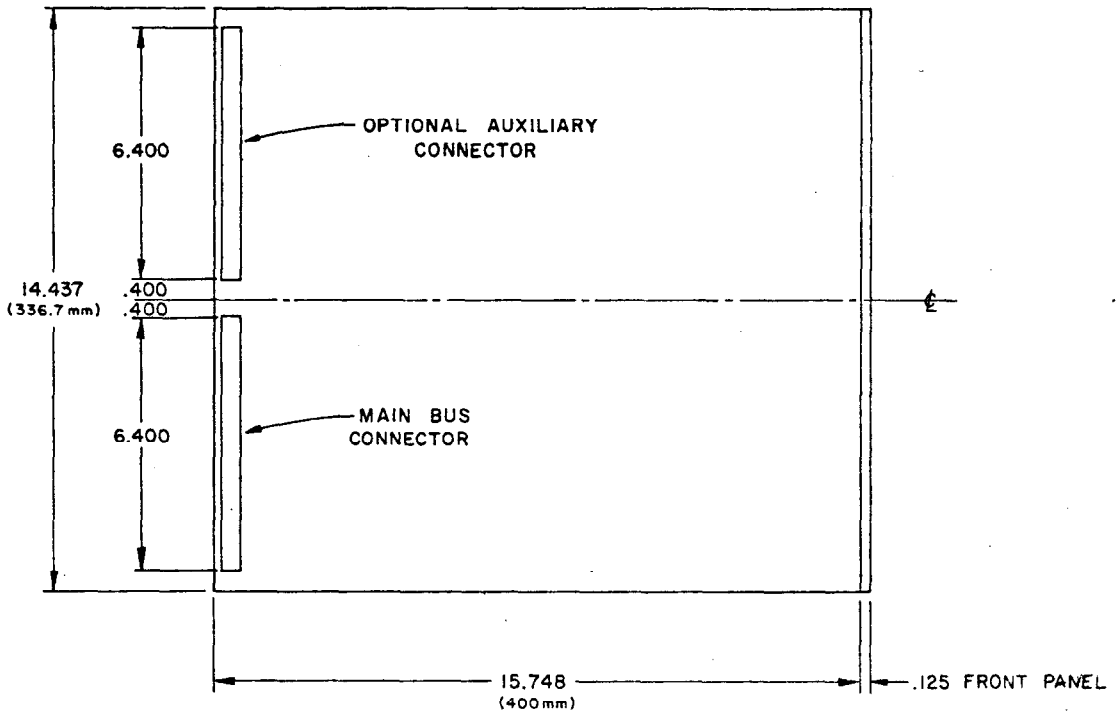
HARDWARE

The preliminary specifications were published for the purpose of evaluating the standard and, where necessary, fix problems with it before the final document was published. The review at the end of the FASTBUS prototyping period showed that not enough room had been alloted in the auxiliary area for making connections. The card size was increased by one 'U' (1.75 in.) and the connectors on the card repositioned. The board outline remains , as before, compatible with the Eurocard system. By maintaining this level of compatibility some economic gains are available to the user from the standardization of chassis parts.

The hardware used in a FASTBUS system can be as simple or as complex as necessary. The things that are specified in detail are the card size, the main bus connector, and the position of that connector on the printed circuit board. The specification for the chassis is that it accomodate the card and provide the connection to the main bus. The method of construction of the chassis and backplane is left to the user. Obviously, standard chassis will be sold by companies and, although they will contain features one does not need for some jobs, the user must decide if he can justify the design and prototyping cost of constructing his own version.

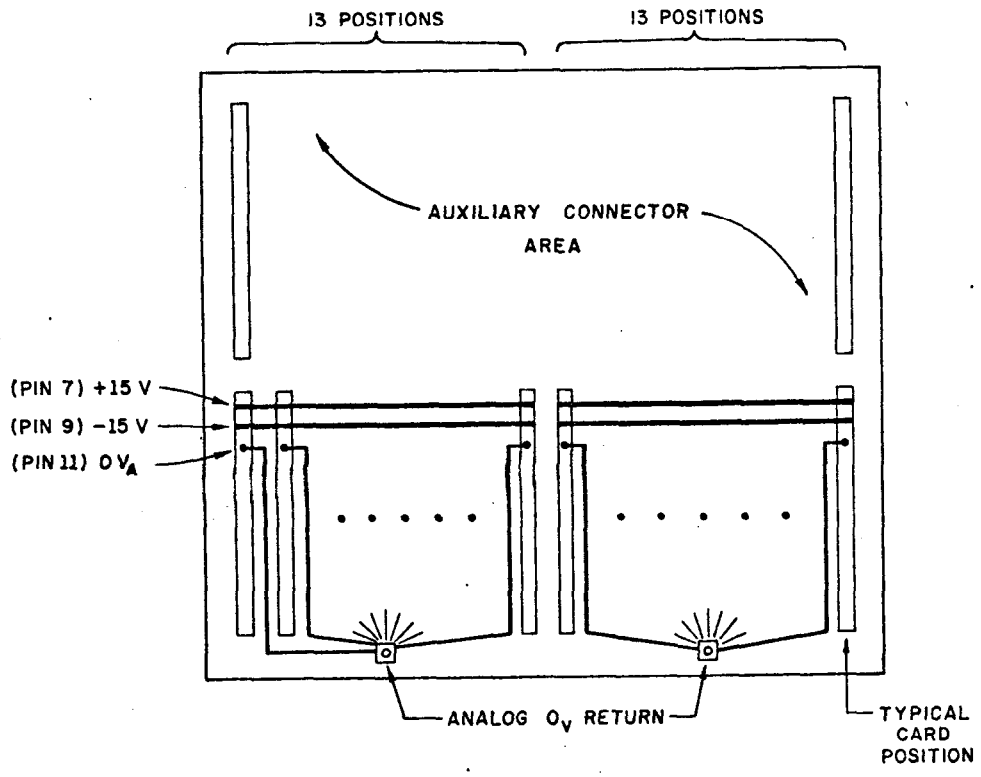
Both the main bus connector and the recommended connector in the auxiliary area are two piece post and box type on .100 in. grid. The main connector is two rows on this .100 in. grid providing 130 pins. If the user wishes, the recommended auxiliary connector can be identical with the main connector. These connector patterns are symmetrical about the horizontal centerline of the card. Figure 1 shows the essential dimensions.



VIEW FROM COMPONENT SIDE

FASTBUS CARD OUTLINE

FIGURE 1.



FASTBUS BACKPLANE
ANALOG POWER DISTRIBUTION

FIGURE 2.

The pins in the auxiliary area also project in the rear of the backplane. Since they are on .100 in grid many types of insulation displacement connectors may be directly attached. By using the auxiliary area as a feedthru panel, the usual mass (mess) of cabling that is hanging in the front of racks may be moved to the rear. Removing these cables from the front allows easy servicing of modules without disturbing the cabling to the detector or elsewhere.

If the user needs some special connectors, the recommended chassis design provides for methods of attaching transition printed circuit boards to these rear projecting pins. The main advantage here with the FASTBUS standard is the flexibility the designer has in solving cabling problems and still work with a standard design.

The MARK III experiment implemented the trigger using three prototype FASTBUS chassis. All signals that come into the trigger from the detector attach in the rear. There are a total of 1280 channels (2560 connections) made with flat ribbon cable using 34 position insulation displacement connectors. Most of these cables loop through the trigger giving a factor of two more connections. The experience with this technique has been very good. No connections have failed to date. About 75 prototype FASTBUS sized cards make up this system. Cards are easily serviced. The chance of making a cabling error when reconnecting has been effectively eliminated.

FASTBUS allows the user to purchase only the power required for each installation by decoupling the card cage and power system in the specification. A 'standard' package has been described for general use. This power supply will probably have its main use in single chassis installations or for lab test facilities. The power supply described in Appendix J can deliver 1500 watts on both the +5 and the -5 volt rails. Typically, one has a maximum of 1500 watts total in a FASTBUS chassis. Therefore one half the power is not being used at any one time. At $1.50 a watt installed this is about $2000 per power supply that would be wasted at each chassis in a large system. Large semiperminant FASTBUS installations can achieve significant cost savings by purchasing only the power actually required.

The backplane design for standard FASTBUS crates has tried to optimize the distribution of analog voltages. Figure 2 shows schematically the +15 volt, -15 volt, and the 0 volt return (quite ground) as implemented in the 50 SLAC prototype backplanes. The + and - 15 volt distribution is split into two parts, each supplying power to 13 card positions. The zero volt return for each of the 13 positions is brought to a single point on the backplane. This allows the analog designer to use a single point (radial) grounding technique to eliminate ground loops.

What about costs of multilayer backplanes? The current design is a nine layer board. The two outer layers contain the main bus. The inner layers, except for one which has the 'T' pin, carry just power. Three of the inner layers should be a minimun of four ounce copper, the rest are two ounce copper. A backplane such as this costs about $300 before the connectors are inserted. The advantage this construction method has is that after the connectors are press fit in place both the signal and power wiring are complete. Backplanes with only 2 layers can be purchased for about $100 but one still has to buy busbars and attach them. It is very difficult to deliver 300 amperes to a card cage and control the voltage drops correctly. Large copper sheets are very effective in delivering currents of this magnitude with drops of 10 millivolts or less over the entire backplane. The connector cost must be added to this, however, that cost is essentially independent of the method of mounting and attaching to the pins. On the average this cost will be six to eight cents per pin. The mated cost per line will be from fifteen to twenty cents per line. This is about what one pays for edgecard connections; remember the gold fingers are not free.

The last hardware problem most often encountered and least often considered at the initial design phase of a system is cooling. FASTBUS considered the cooling problem early in the writing of the standard. The guidelines for chassis construction, air flow, and heat removal in general are detailed in the document and its appendices. These should be of great help to the designer. In addition, many internal FASTBUS reports are available on this subject. The designer should seriously look at this portion of FASTBUS early in the design phase It is difficult, if not impossible to retrofit cooling into a 1500 watt chassis.

BUS COMPATIBILITY

The fundamental operations on the bus are asynchronous in nature. A bus master issues timing request signals which are expected to be answered by timing response lines. The standard protocol also has a synchronous data transfer operation specified, however this probably does not gain one any operating speed when the communication is confined to a single backplane.

To be compatible with standard FASTBUS devices only a minimum number of lines need to be obeyed. Ten lines are used to handle the multimaster arbitration. The bus has two lines (RB and BH) which are used to reset all devices on the bus. Two timing lines (AS and AK) define the master to slave lock. The ten arbitration lines along with these four lines must be used in a standard fashion.

The designer, if there are definite needs, can remain physically and electrically compatible by simply obtaining control of the bus in the standard fashion, obeying the protocol on the four lines mentioned above, and then running any protocol he desires on the remaining 46 bus lines.

If the user wishes to communicate from one chassis to another through standard Segment Interconnects two more timing lines

must be obeyed; DS and DK. Additionally, the direction of information flow must be consistant with the direction standard protocol would cause the Segment Interconnect to point its transceivers. The user could then invent a private protocol on the remaining 44 lines.

Within the standard backplane are additional lines for use by front end equipment. Two sets of daisy chain lines along with an associated return line may be used to sequentially scan modules. The disadvantage of this type of readout is the inability to skip bad units or remove a card and continue operating without patching the daisy chain across to the next unit. These systems are also difficult to trouble shoot due to the inability to sit on a suspected faulty unit and continuously access it.

Another point needs to be made about daisy chain systems. A study group, early in the design of FASTBUS, tried to see if significant readout speed was gained by using daisy chain instead of a handshake protocol such as FASTBUS. Their conclusion was that the daisy chain had no advantage over a handshake protocol. Some of the reasons in the past concerning economics of hardware I believe are no longer viable when one considers the total cost including testing and maintenance. A standard readout system comes out ahead.

In addition to the daisy chain lines a 'N' line type pin is available at each position in the chassis. These pins are the 'T' pins, so called because they connect in a 'T' fashion at each card slot to the corresponding data bus line. For example, the 'T' pin at position 5 is connected to Address/Data <Ø5>, etc. These lines may be used in conjunction with a control line to either point at one position or obtain one bit of data from a position. Since these pins are hooked to the 32 bit data bus, the operation may be carried out in parallel to all positions in the chassis simultaneously.

Fast readout schemes can be conceived using the 'T' pins. For example, the controller does a pattern read to the entire chassis. Each device containing data asserts its 'T' pin. This operation gives the controller cards which contain data. Next it points at the cards which previously indicated data present by a 'T' pin type addressing, or maybe converts the pattern data to a five bit geographical address and obtains the data in a more conventional FASTBUS manner.

MONITORING AND TESTING

Probably the most serious electronic problem facing large experiments, other than design time, is the testing and monitoring of the equipment. Access to large amounts of electronics is severely limited at colliding beam machines. When access is gained, it may be only for short periods. This means that problems must be diagnosed as much as possible remotely so efficient use is made of what access time is allotted.

FASTBUS has provisions in the standard to allow just this type of remote diagnostic capability. Designers are encouraged to implement control and status registers. Since these are standardized for the more common functions it is easy for other people familiar with FASTBUS to check the system. Computer readable ID numbers in modules insure that parts of the system are correctly in place. A quick computer scan of the system can save many hours of lost running due to misplugged modules.

The asynchronous nature of the FASTBUS control along with the Wait (WT) line lets monitoring modules stop operation, single step the bus, and possibly control the bus if necessary. This single stepping feature along with a 'back door' serial diagnostic system will let the FASTBUS user obtain a maximum amount of information even if the computer does not have access to a crate via the main bus. SLAC has a SNOOP module under construction to serve just this function. The bus protocol is under software control when it acts as a master. This allows the SNOOP to simulate some private protocols and serve as a diagnostic tool for more than just standard FASTBUS protocol devices.

The serial system in FASTBUS is similar to ETHERNET, although at the moment it operates at about 1ØØkhz instead of the 1Ømhz proposed for ETHERNET. When the LSI integrated circuits become available the serial diagnostic system will be upgraded. It is possible that ETHERNET devices may be coupled to FASTBUS and give the user another method of attaching computers and pheripheral equipment.

One issue raised when discussing the additional diagnostic registers is the added cost of the IC's. That is true; IC's and their cost of installation are not free. However, when accelerator time is costing many thousands of dollars an hour, the savings from a few IC's soon turn into large additional costs. With current budgets severely restricted, the accelerator operating time will become more valuable and force experimenters to use it more efficiently.

Next lets look at FASTBUS and testing. Often the last thing considered when building special systems is the design of test fixtures. Here again adherence to a standard can be of help. If one assumes a standard crate and power supply are available in the lab, a portion of the test fixture is automatically present. If one also has a general purpose register driven FASTBUS interface then the entire test fixture may be present with a little programming. Staying with a standard will also provide one automatically with extenders, test boxes with switches, or a host of other devices. How much effort has been wasted because a special piece of electronics didn't have all the tools to test it available? Following the standard also has the advantage of giving one the same tools away from home.

The problem is compounded when a good design at one place is used by someone at a

second place. The new user is now faced with no chassis, no test gear, no extenders, etc. The cycle repeats --- the first place cannot loan the equipment since they need it for their own operation and don't have a spare.

CONCLUSION

The FASTBUS standard has attempted to solve not only sophisticated communication and data processing problems but also provide a vehicle for building to a standard systems that were in the past only doable with special designs. This is not to imply that all electronics for High Energy Physics will be FASTBUS. A large amount of older equipment in CAMAC and other packages is still useable. Certain restrictions at the very front end electronics which directly mount on the detector require special layouts. There may also be some very fast triggers which also require special connections --- these may be, however, candidates for a FASTBUS hardware only package. It does seem to this author that once the signal processing passes the directly attached printed circuit boards that very serious considerations must be given before designing hardware which does not conform to all, or at a minimum, at least a portion of a standard.

FURTHER INFORMATION

Anyone interested in FASTBUS should obtain a copy of the latest document from:

Louis Costrell
National Bureau of Standards
Center for Radiation Research
Washington, DC 20234

Many additional internal FASTBUS committee reports and reprints of articles are also available. Approximately 140 such documents are cataloged. To obtain a list write:

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