HIGH RESOLUTION SILICON COUNTERS

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Summary

A brief description of our development of silicon strip counters is given, with some recent measurements of their performance. A few comments are made on the outlook for the use of these devices with colliders.

Introduction

First here is a brief review of the relevant characteristics of silicon as a detector. Wafers of monocrystalline silicon with resistivity ρ Ωcm and thickness t cm are doped suitably to form a diode structure which is depleted of majority carriers at a voltage V volts (for n-type silicon)

$$V \simeq 4\times10^{8}\frac{t^2}{\rho}$$

(70 volts depletes 300 μm of 5000 Ωcm material). The wafer is used as an ionization chamber which should have a leakage current ∿1 μa/cm^2 and gives 1 electron hole pair per 3.6 ev. energy loss, leading to a signal of some 2.5×10^4 electrons per 300 μm track length for a minimum ionization particle. The detector noise can be negligible, but the preamplifier noise is not, and depends on the bandwidth and detector capacity.

For pulse-shaping time constants of ∿200 nsec we obtain an rms amplifier noise of ∿500 electrons with a slope of 15 electrons/pf. This determines the thickness of silicon required. Typically strips on a 300 μm wafer have a peak signal/rms noise = 30/1. In fact 280 μm to 350 μm thickness are industrial standards and easy to handle. Typical numbers quoted will be for 300 μm material.

Physical Limitations to Measurement Accuracy

There is a spread of charge around a minimum ionization particle's trajectory due to electron (and hole) diffusion of some 5 μm radial width, and a much smaller spread due to space charge repulsion. These introduce a negligible error in the position of the centre of gravity of the charge (CGC). For tracks perpendicular to the counter surface high energy knock-on electrons give a lateral displacement of the CGC of ∿5 μm rms but if the signal amplitude is measured, and large signals are rejected (or suitably weighted) track coordinates may be measured with an rms error of ∿2 μm. For inclined tracks the small "Landau" fluctuations give rise to an additional error in coordinate measurement -- approximately equal to 1/30 × counter thickness for 45° inclination.

Design Considerations and Results

Some possible strip configurations are shown in Fig.1.

One coordinate can be read out on each strip (a), using charge division read out is only necessary every nth strip (b), counters have been constructed reading out x and y coordinates on one wafer (c).

We, a CERN,Munich collaboration, have chosen to start with a charge division system because we want to measure to σ < 10 μm for a charm vertex search at the

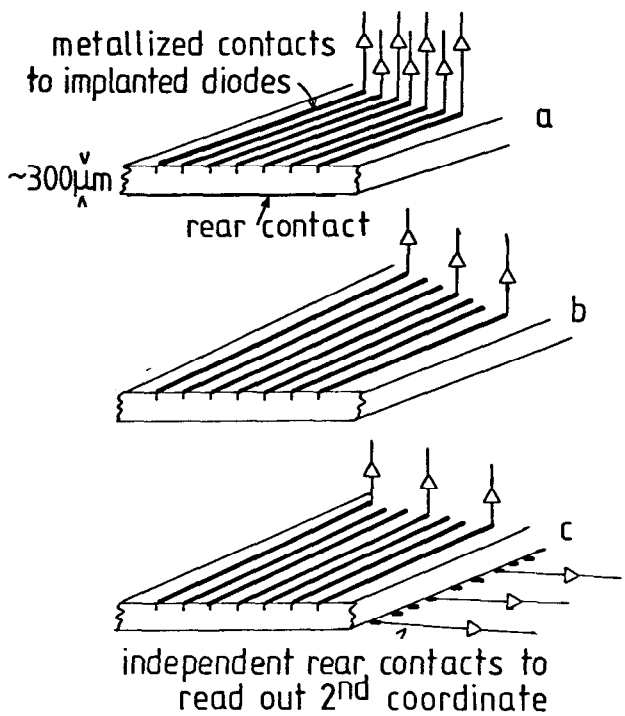

Fig. 1.

CERN SPS. Industrial bonding wire is at least 20 μm thick (and squashes on bonding) so although a 20 μm pitch pattern gives ∿7 μm resolution there is no convenient way to connect to each of a large array of such lines. The structure we have chosen is shown in Fig.2.

The active area is 24×36 mm^2. On this there are 1200 strip diodes of which 240 are bonded to a fanout card. The whole device has a leakage current of around 1 μamp (∿1 namp per diode) at its working voltage.

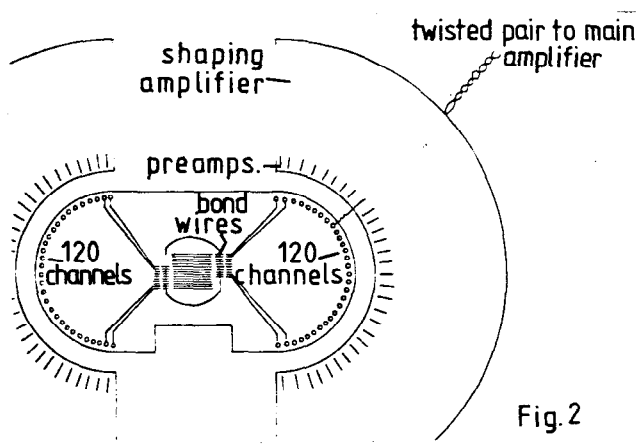

Fig.2

Although charge division will probably give ∿10 μm resolution across 120 μm spacing we need to read out every 60 μm in the forward direction where close track resolution is required. We have found also that although 20 μm pitch lithography is relatively easy a closer pitch is technically difficult for wafers of our size.

We have chosen charge-sensitive preamplifiers with shaping time constants of 180 nsec as a compromise between counting high fluxes and getting adequate signal/noise to use charge division. The noise per channel in the set-up is ∿600 electrons. We plan to use some 1200 channels. The arrangement used is shown in Fig.3.

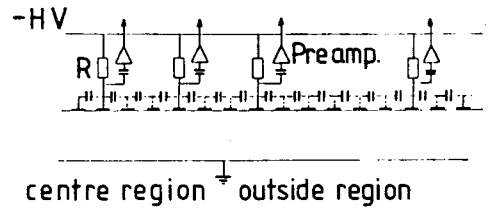

Fig. 3.

There is a capacitative divider network given by the interstrip capacities. The floating strips have to be charged up to the full bias voltage by a resistive layer. The resistive layer is only required to maintain the D.C. potential and does not enter into the charge division process. Fig.4 shows the resolution obtained in a 200 GeV beam for measurements across strips read out every 60 μm and every 120 μm.

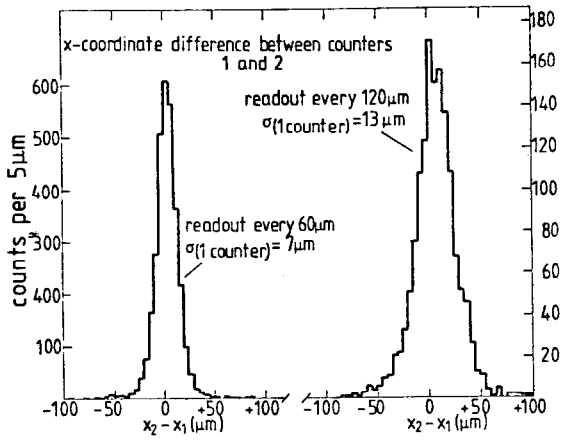

Fig. 4.

Possibilities for Colliders

The devices we have made are satisfactory for high energy external beam experiments where the particles are concentrated in a forward cone leaving "sideways" free for the fanout and electronics. However, a cylindrical array with 10 amplifiers every millimeter is a clumsy object. In fact a twisted pair cable fills ∿30 times more cross-section than the channel it reads out. Counters about 15 cm long could be read out with a signal/noise ratio of ∿30/1 but the problem of fitting amplifiers around a 10 or 20 cm diameter cylinder is difficult, and the cost deterring.

For any bunched beam collider it is clear that sequential readout is required. With on chip (or near chip) electronics reading, say, 10 strips in sequence the problems of space, cost, and cooling would be resolved. At MPI and CERN we are designing such systems.

Finally it is worth remembering that high resolution counters are only useful for high energy particles. 100 μm of silicon scatters as much as 10 cm of argon (at NTP).

With a detector a distance r_1 from a vertex for 100 μm of silicon, the scattering at r_1 introduces a lateral vertex error of 5 μm for 1 GeV particles with r_1 = 1 cm, and for 10 GeV particles with r_1 = 10 cm.