Low Noise Double-Sided Silicon Strip Detector for Multiple-Compton Gamma-ray Telescope [*]

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Abstract

A Semiconductor Multiple-Compton Telescope (SMCT) is being developed to explore the gamma-ray universe in an energy band 0.1–20 MeV, which is not well covered by the present or near-future gamma-ray telescopes. The key feature of the SMCT is the high energy resolution that is crucial for high angular resolution and high background rejection capability. We have developed prototype modules for a low noise Double-sided Silicon Strip Detector (DSSD) system which is an essential element of the SMCT. The geometry of the DSSD is optimized to achieve the lowest noise possible. A new front-end VLSI device optimized for low noise operation is also developed. We report on the design and test results of the prototype system. We have reached an energy resolution of 1.3 keV (FWHM) for 60 keV and 122 keV at 0°C.

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1. INTRODUCTION

The gamma-ray universe in the energy band above 0.1 MeV provides a rich ground to study nucleosynthesis and physics of particle acceleration beyond thermal emission. However, the energy band between 0.1 MeV and 100 MeV is poorly explored due to difficulties associated with the detection of such photons. The Compton telescope COMPTEL[1] abroad CGRO (Compton Gamma-Ray Observatory) demonstrated that a gamma-ray instrument based on the Compton scattering is useful for the detection of the gamma-ray in this energy band. COMPTEL provided us with rich information on a variety of gamma-ray emitting objects either in continuum and line emission. The continuum sources include spin-down pulsars, stellar black-hole candidates, supernovae remnants, interstellar clouds, active galactic nuclei (AGN), gamma-ray bursts (GRB) and solar flares. Detection has also been made of the nuclear gamma-ray lines from ^{26}Al (1.809 MeV), ^{44}Ti (1.157 MeV), and ^{56}Co (0.847 and 1.238 MeV).

Although COMPTEL performed very well as the first Compton telescope in space for MeV gamma-ray astrophysics, it suffered severely from large background, poor angular resolution, and complicated image decoding.[2] In 1987, T. Kamae *et al.* proposed a new Compton telescope based on a stack of silicon strip detectors (SSD).[3, 4] This technology presents very attractive possibilities to overcome the weaknesses of COMPTEL as described later in this document. This idea of using silicon strip detectors stimulated new proposals for the next generation Compton telescope.[5–7]

Recently, a new semiconductor detector based on CdTe (Cadmium Telluride) emerged as a promising detector technology for detection of MeV gamma-rays.[8] Taking advantage of significant development in CdTe technology, we have proposed a new generation of Compton telescope, a Semiconductor Multiple-Compton Telescope (SMCT). The SMCT is a hybrid semiconductor gamma-ray detector which consists of silicon and CdTe detectors. Excellent energy resolution is the key feature of the SMCT to achieve high angular resolution and background rejection capability. In addition, the ability to measure polarization, a wide energy band (0.1–20 MeV), a wide field of view (∼60°) and light weight are important features of the SMCT. Low noise Double-sided Silicon Strip Detectors (DSSDs) are fundamental elements of the SMCT. In this paper, we describe the optimization of the detector components to realize the fine energy resolution and the test results with prototype modules. Other applications for such low noise DSSD system and hybrid Si-CdTe system are described elsewhere.[9]
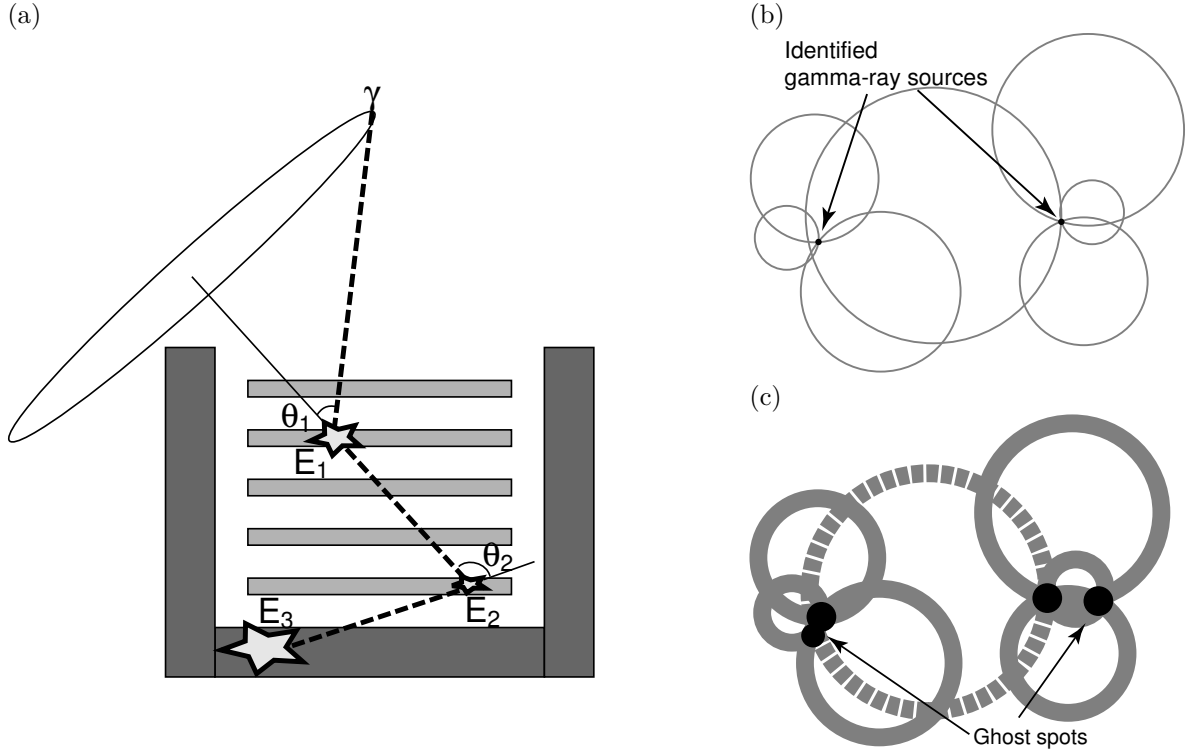
2. MULTIPLE-COMPTON TECHNIQUE

A simple Compton telescope consists of two components, a scatterer and an absorber. The direction of the gamma-ray can be confined in a cone by measuring the energy loss and position of the scattering in the scatterer and those of photoelectric-absorption in the absorber. In order to increase the detection efficiency of the gamma-ray, the scatterer has to be thicker and/or more dense. However, it also increases the probability of multiple-Compton scatterings in the scatterer, which was considered to be impossible to resolve. In order to solve this problem, a stack of many thin scatterers is used to record individual Compton scatterings in the Multiple-Compton technique. The order of the interaction sequences, hence the correct energy and direction of the incident photon, can be reconstructed by examination of the energy-momentum conservation for all possible sequences. This technique has proven to be a very powerful method to suppress backgrounds.

Figure 1 (a) illustrates a case with two Compton scatterings in the scatterer and one photoelectric-absorption in the absorber. In this situation, both scattering angles θ_1 and θ_2 can be obtained from the recoil electron energies as

$$\cos\theta_1 = 1 + \frac{m_e c^2}{E_1 + E_2 + E_3} - \frac{m_e c^2}{E_2 + E_3}, \quad \cos\theta_2 = 1 + \frac{m_e c^2}{E_2 + E_3} - \frac{m_e c^2}{E_3}, \tag{1}$$

where E_1, E_2 and E_3 are the energy deposits in each photon interaction. It is worthwhile noticing that θ_2 can be reconstructed from the hit positions of the three interactions. This over-constraint provides stringent background suppression that is crucial to observe faint or diffuse gamma-ray sources. Note that the photon does not have to be absorbed completely in this multiple-Compton technique since the incident photon energy can be inferred when three or more Compton scatterings are recorded, which means no need for a heavy calorimeter in the telescope. Another possible advantage of this technique is that recoil electrons with energies more than

Figure 1. (a) Concept of Multiple-Compton technique. (b) and (c) Illustration of processes to reconstruct source locations using photon candidates from two gamma-ray sources. The angular resolution in (b) is 10 times better than that in (c).

250 keV penetrate a 300-μm silicon detector and deposit energies in two layers of silicon detectors. Although the angular resolution is very poor for such low energy electrons due to multiple-Coulomb scattering, this information can still be used to constrain the direction of the incident photon to a partial cone.

High energy resolution for the recoil electron is the critical characteristic of Compton telescope since it determines the angular resolution of the incident photon, and background rejection capability using Compton kinematics. Figures 1 (b) and (c) illustrate processes to reconstruct gamma-ray source locations with different angular resolutions to demonstrate the importance of angular resolution. In these figures, a circle represents a projection of a cone reconstructed by the Compton kinematics onto a sky map for each photon candidate.[†] The width of the circles in figure 1 (b) is 10 times narrower than that in figure 1 . We can clearly identify two gamma-ray sources in figure 1 (b). In figure 1 (c), it is difficult to resolve them because ghost spots cannot be rejected due to poor resolution. In addition, the dashed circle can belong to two spots from different sources, further complicating the matter. Since the circle radius can be very large depending on the Compton scattering angle, we may suffer large background from any bright source in the field of view. Therefore, precise angular resolution is essential to resolve source locations and to suppress background from bright sources.

The DSSD is a primary candidate for the scatterer because Compton scattering dominates over other processes in sub-MeV range and the Doppler-broadening effect is small in silicon. Such double-sided devices are required to provide two dimensional measurement of the interaction position. Weak stopping power of the silicon detector at the upper end of the energy band can be supplemented by employing the CdTe detectors in the back portion of the layers. Figure 2 shows the probability of various photon interactions in 500 μm thick silicon and CdTe devices as a function of the photon energy. This figure clearly illustrates the advantage of a Si-CdTe hybrid approach to detect photons in a wide energy-band. For the photon energies below 0.5 MeV, silicon is a

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[†]The projection is not actually a circle. We use a circle for simplicity.
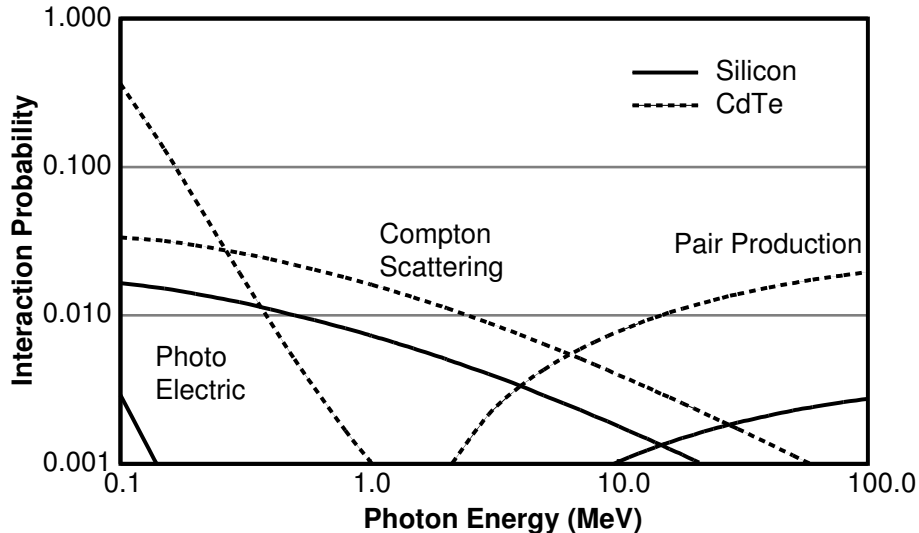
Figure 2. Probability of various photon interactions in 500 μm thick silicon and CdTe devices as a function of the photon energy.

better scatterer since the Compton scattering cross section is larger than that of the photoelectric absorption. Note that photoelectric absorption does not provide information on the incident photon direction. The DSSD layers measure the recoil electron energy of the first Compton scattering with maximal energy resolution while the CdTe layers enhance the probability of Compton scattering and/or photoelectric absorption in the back section. At higher energies, silicon becomes more or less transparent and CdTe detector becomes the dominant detector. Pair creation can also be utilized to measure both the energy and direction of gamma-rays above several MeV. However, the efficiency is significantly reduced above 20 MeV since the gamma-ray cannot be completely absorbed. In this case, a higher Z material is required to enhance photon absorption.

As discussed above, precise energy resolution is a crucial feature of the DSSDs to gain high pointing accuracy and large background rejection capability, utilizing the over-constraint from the kinematics of multiple-Compton scattering. Low electronics noise is required to accomplish such fine energy resolution by exploiting the small Doppler-broadening effect in silicon. A target noise value in equivalent noise charge (ENC) for the DSSD system is 100 e^- (RMS, Root Mean Squared), which corresponds to 1 keV (FWHM, Full-Width Half Maximum) for the silicon detector. This equates to an angular resolution of 1° at 30 keV or 0.3° at 2 MeV. Angular resolution at the upper end of the energy band is dominated by the position resolution of the detector.
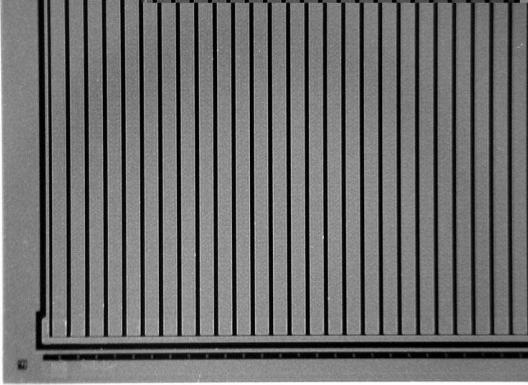
Possible instrument configurations and expected performance are discussed in ref 9.

3. LOW NOISE SSD SYSTEM

We have developed prototype modules for a low noise DSSD system in order to understand all noise sources in detail, which is fundamental to achieve the best possible energy resolution. A low noise DSSD system consists of a DSSD, an RC chip and a VA32TA front-end VLSI chip. The DSSD does not employ an integrated AC capacitor in order to maintain a strip yield close to 100%. The RC chip provides detector bias voltage via polysilicon bias resistors, as well as AC-coupling between strips and preamplifier channel inputs. Since the RC chip is a small device, the yield of the AC-coupling capacitor is not a concern. The VA32TA front-end VLSI is a 32-channel, low noise CMOS device which includes on a per-channel basis a preamplifier, shaper, sample/hold, analog multiplexer and discriminator. The DSSDs and RC chips are manufactured by Hamamatsu Photonics, Japan and the VA32TA is manufactured by Ideas ASA, Norway. Detailed description of each component is given below.

The p$^+$-strips are implanted on an n$^-$ silicon substrate to form p-n junctions. This side is called junction side. The n$^+$-strips are implanted orthogonal to the p-strips on the other side to provide second coordinate

(a) DSSD junction side   (b) DSSD ohmic side

Figure 3. Pictures of a DSSD for (a) junction side and (b) ohmic side. Strips are surrounded by guard ring.

measurement. This side is called ohmic side. The p^+-implant surrounds the individual n^+-strip to provide separation of n^+-strips. Figure 3 shows pictures of the junction and ohmic sides of the DSSD. Because the strip geometry is more complex on the ohmic side than on the junction side, the strip capacitance is larger on the ohmic side. For this reason, the primary function of the ohmic side is to provide position information of the second coordinate, and its noise performance is not measured in this test. We have produced five types of strip geometries in four types of devices (400-1, 400-2, 800-1, 800-2) as listed in Tables 1 and 2 to understand the noise dependence on parameters such strip pitch, strip gap and strip length. Wider strip pitch gives larger capacitance to the backplane and larger leakage current. Wider strip gap gives smaller capacitance to the adjacent strips although the risk of junction breakdown increases at high bias voltage. The 400-2a $\sim$ 400-2c configurations are implemented on the junction side of a single-sided SSD. (Ohmic side does not have strip structure.) All four types of devices are implemented on one silicon wafer. The thickness of the silicon wafer is fixed at 300 μm. Here we present results on the basic characteristics for types 400-2a, 400-2b and 400-2c SSDs. The C-V curve measurement yields the depletion voltage of 65 V, therefore the following measurements are performed at 70 V.

Table 1. Parameters for strip geometry of the double-sided SSD prototypes.

Type	Strip pitch [μm]	Strip gap [μm]	Strip length [cm]
400-1	400	100	2.56
800-1	800	100	2.56
800-2	800	100	1.27

Table 2. Parameters for strip geometry of the single-sided SSD prototype.

Type	Strip pitch [μm]	Strip gap [μm]	Strip length [cm]
400-2a	400	100	2.56
400-2b	400	130	2.56
400-2c	400	160	2.56

A bias voltage of up to 200 V was applied to test junction breakdown and no breakdown was observed. Leakage current is measured to be 0.5 nA/strip at 20°C and 0.05 nA/strip at 0°C. The strip capacitance is measured to be 6.3 ± 0.2 pF for 400-2a, 5.7 ± 0.2 pF for 400-2b and 5.2 ± 0.2 pF for 400-2c, which is somewhat larger than the values calculated based upon geometry of 5.1 pF, 4.8 pF and 4.5 pF, respectively. In the capacitance calculations, we take into account only capacitance to the backplane and adjacent strips. Measured values of the strip capacitance are used for the subsequent noise analysis.

The RC chip consists of bias resistors and AC-coupling capacitors. We employ 1 GΩ polysilicon resistor for the bias resistor. A resistance value of 1 GΩ is chosen to minimize thermal noise without compromising production stability. A MOS capacitor is employed for AC-coupling to ensure high voltage tolerance, since it needs to withstand the bias voltage of the DSSD and to protect the preamplifiers. The size of this MOS capacitor is 1.2 mm × 0.14 mm in order to obtain sufficient coupling capacitance while presenting a capacitance load to the preamplifier of less than 1 pF.
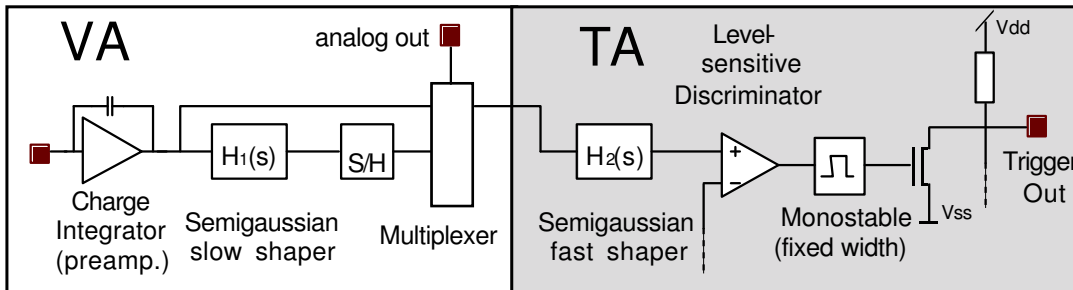

**Figure 4.** Block diagram of VA32TA front-end LSI.

We have developed the VA32TA front-end ASIC based on the VA32C amplifier VLSI and the TA32C trigger VLSI that are originally developed by Ideas. A detailed description of Viking-architecture chip is given elsewhere.[10, 11] The VA32TA is fabricated in the AMS 0.35 μm technology, which is measured to be radiation tolerant to 20 MRad or more.[12] A VA32TA consists of 32 channels of signal-readout. Each channel includes a charge sensitive preamplifier-slow CR-RC shaper-sample/hold-analog multiplexer chain (VA section) and fast shaper-discriminator chain (TA section) as illustrated in the block diagram of Figure 4. The front-end MOSFET size for the preamplifier is optimized for small capacitance load, to attain optimal noise performance. Expected noise performance is $(45 + 19 \times C_d)/\sqrt{\tau}\ e^-$ (RMS) in ENC or $(0.37 + 0.16 \times C_d)/\sqrt{\tau}$ keV (FWHM), where C_d is the load capacitance and τ is the peaking time, which can be varied from 1 to 4 μs. Feedback resistors for the preamplifier, as well as slow and fast shapers are realized with MOSFETs. Gate voltages of the feedback MOSFETs are controlled by internal DACs (Digital-to-Analog Converters) on chip. Bias currents for various components are also controlled by the internal DACs. Threshold levels can be adjusted for each channel using individual DACs to minimize threshold dispersion. A 200-bit register is required to hold the values for all internal DACs. Majority selector logic circuitry has been utilized for these registers to ensure the tolerance against Single-Event Upset (SEU), which is important for space applications. This majority selector circuitry uses three flip-flops for each bit and takes a majority of the three when they become inconsistent. This logic also generates a signal when such inconsistencies are detected.

We have assembled two prototype modules, one consists of SSD, RC chip and VA32TA (AC module) and the other module consists of SSD and VA32TA (DC module). Type 400-2 SSD is used for both modules. Figures 5 (a) and (b) show pictures of the AC and DC modules, respectively. Only 400-2b and 400-2c strips are connected to the readout system because of geometric constraints. Only the junction side is connected to the readout system in this test since energy resolution is determined by the noise performance on the junction side. The ohmic side is known to give worse noise performance due to larger strip capacitance and used primarily to provide the coordinate information and a trigger coincidence.
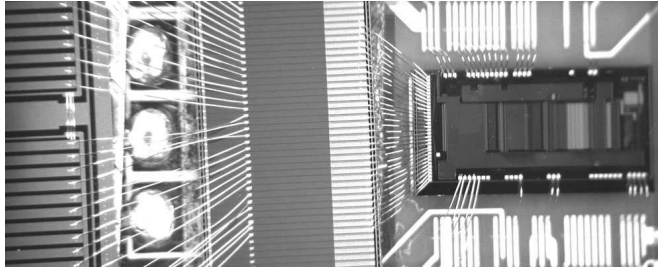
(a) AC configuration   (b) DC configuration
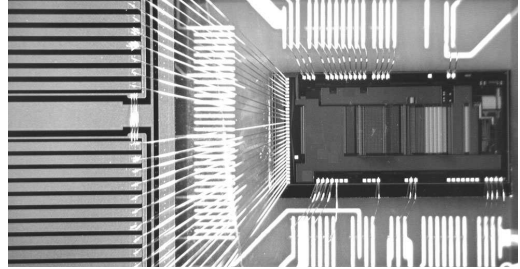
Figure 5. Pictures of prototype SSD modules with (a) AC and (b) DC configurations. The DSSD is located on the left and the VA32TA is located on the right. In the AC configuration, an RC chip is present between the SSD and VA32TA.

4. NOISE PERFORMANCE

We have taken into account the following noise sources in our analysis to optimize the component parameters:

- Preamplifier noise: linear dependence on the capacitance load and $1/\sqrt{\tau}$ dependence on the peaking time. Noise level varies from 0.8 keV (DC, $\tau = 4\ \mu$s) to 1.4 keV (AC, $\tau = 2\ \mu$s).

- Shot noise: $\sqrt{I}$ dependence on the leak current and $\sqrt{\tau}$ dependence on the peaking time. Noise level varies from 0.3 keV (0°C, $\tau = 2\ \mu$s) to 1.2 keV (20°C, $\tau = 4\ \mu$s).

- Thermal noise (bias resistor): $1/\sqrt{R}$ dependence on the bias resistance and $\sqrt{\tau}$ dependence on the peaking time. Noise level varies from 0.3 keV ($\tau = 2\ \mu$s) to 0.4 keV ($\tau = 4\ \mu$s).

We have also considered the thermal noise from the implant resistance of the RC chip and found it is less than 0.1 keV, hence considered negligible. Total noise is fairly independent of the peaking time beyond 2 μs because amplifier noise and other noise sources show opposite peaking time dependence and compensate each other.

Noise performance of the prototype system is measured at temperatures of 0°C and 20°C and at peaking times of 2 μs and 4 μs. This is useful to differentiate the noise contributions. Absolute gain of the system is calibrated using the X-ray spectra obtained below. Table 3 summarizes the measurement results and compares them with calculation results. This table does not include the result for the DC configuration at 20°C since it cannot be operated at optimum condition due to the effect of leak current from the SSD flowing into the preamplifier. Since the results for 400-2b and 400-2c do not show significant difference (less than 5% though the 400-2c consistently gives better noise performance), the average of the two types are shown in this paper. These

Table 3. Noise and energy resolution measured for the prototype modules in the AC and DC configurations at temperatures of 0°C and 20°C and peaking times of 2 μs and 4 μs.

Configuration	Temperature	Peaking time	Noise (FWHM)		Energy resolution (FWHM)	
			Expected	Measured	60 keV (^{241}Am)	122 keV (^{57}Co)
AC	20°C	2 μs	1.6 keV	1.7 keV	1.9 keV	2.1 keV
		4 μs	1.6 keV	1.7 keV	2.1 keV	2.3 keV
	0°C	2 μs	1.4 keV	1.6 keV	1.8 keV	1.9 keV
		4 μs	1.1 keV	1.4 keV	1.7 keV	1.8 keV
DC	0°C	2 μs	1.1 keV	1.2 keV	1.6 keV	1.6 keV
		4 μs	0.9 keV	1.0 keV	1.3 keV	1.3 keV

results confirm that the shot noise due to the leakage current becomes negligible at 0°C. In the DC configuration, the measured and expected noise values are in a good agreement for the measurements at either peaking time, which demonstrates that the noise sources from the SSD and the VA32TA are well understood. On the other hand, slight disagreement between measurement and calculation is observed for the AC configuration at 0°C, indicating additional noise sources in the RC chip which are not accounted for in the noise analysis. At 20°C the shot noise from the leak current becomes large and the disagreement becomes less significant. Further studies are required to identify the origin of the excess noise observed in the RC chip in this measurement.

5. X-RAY ENERGY RESOLUTION

The energy resolution for the X-ray detection is investigated using the 59.54 keV X-ray line from [241]Am and the 122.06 keV X-ray line from [57]Co. Absolute gain is calibrated for each channel using the same X-ray sources in such way that all channels give the correct peak height. We also correct for the gain dependence on the "common mode shift" where common mode shift refer to the voltage shift common to all channels in one chip.[‡] We attribute the origin of this dependence to the nonlinearity of the amplifier gain. A correction of approximately 0.2 keV is made for a 1 keV common mode shift. This correction is critical to operate the system at 20°C, since the magnitude of the common mode noise is 6 ∼ 10 keV at 20°C and 1.6 keV at 0°C. Larger common mode noise is observed for the longer peaking time at 20°C, implying a low frequency nature of the common mode noise. It should be noted that the peaking time of the fast shaper in the TA section is 0.3 μs, which helps to suppress the contribution from common mode noise.

Figures 6 (a) and 7 (a) show the sum of the energy spectra for all channels, except for the first and last strips where we observe larger noise. We observe a clear Compton edge just below 40 keV in the [57]Co spectrum. Peak positions other than 59.5 keV and 122.1 keV are somewhat shifted since gain calibration has not been performed for these energy points yet. In order to obtain the energy resolution, we fit the energy spectrum to a sum of two Gaussian functions to describe the peak and one threshold type function[§] to describe the continuum spectrum. The mean value of the second Gaussian is shifted by −1 ∼ −2 keV due to missing charge. The fraction of the second Gaussian is in general less than 15%. Figures 6 (b) and 7 (b) show the magnified energy spectra around the peak and the fit results.

Table 3 summarizes the results of the energy resolution measurements. Energy resolution is worse than the intrinsic noise performance of the system predominantly due to uncertainties of the gain calibration. Gain uncertainty can also explain the fact that the energy resolution is worse for higher energy.

This result demonstrates that the energy resolution of 1 keV is an achievable goal for the SCMT, considering the planned improvements discussed below.

6. CONCLUSIONS AND FUTURE PROSPECT

We have fabricated prototype modules for a DSSD system which is a crucial element of the SCMT. Intrinsic noise performance is measured to be 1.0 keV (FWHM) at 0°C in the DC configuration, which is in good agreement with the analytically calculated noise value of 0.9 keV. The energy resolution is measured to be 1.3 keV (FWHM) in the same configuration, demonstrating that the energy resolution of 1 keV is within our reach.

It is still of great importance to establish that the multiple-Compton technique can be used to measure the photon direction and polarization, as well as the energy by using a stacked DSSD setup. This is the logical step for us to pursue next.

Moreover, we also plan to develop a full-size DSSD module based on the information obtained with the present prototype. The size of the DSSDs will be 5 cm × 5 cm, which is the largest size possible with 4-inch wafers. This size translates into twice the capacitance load for amplifier in the DC configuration. Since the noise performance is dominated by the amplifier noise, improvements in the amplifier performance and reduction of
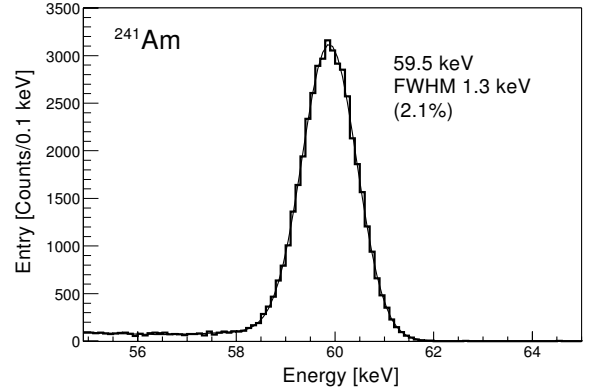

[‡]The coomon mode shift is calculated and subtracted for each event taking the average of the pulse height for every channel, excluding the channels with signal.

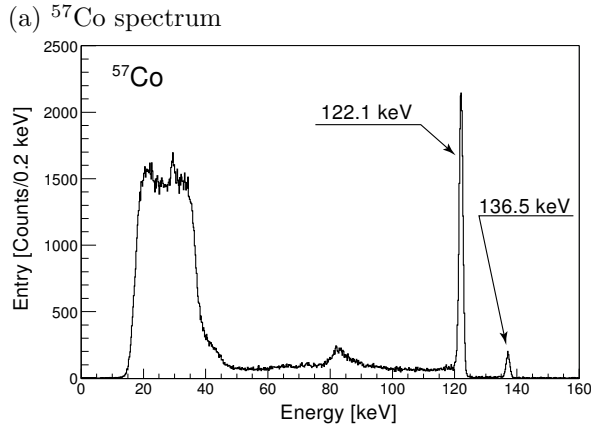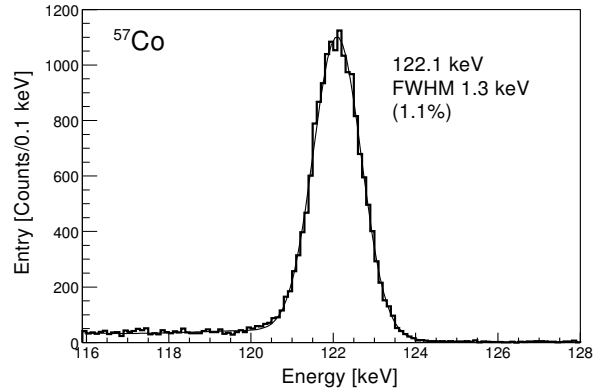[§]This function is expressed as $f(E) = p_1 \cdot (E_0 - E)^{p_2} \cdot e^{-p_3(E_0 - E)}, \;\; (E < E_0)$.
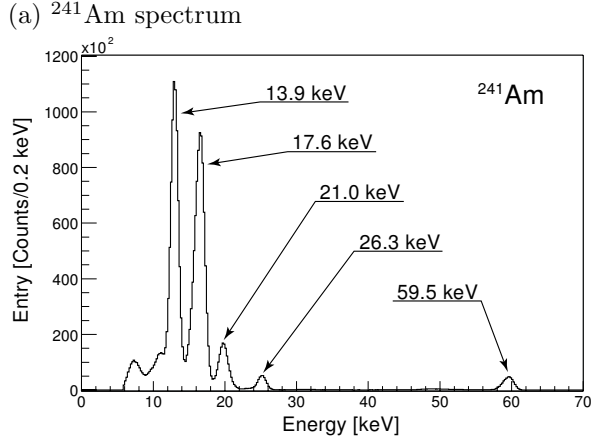
(a) ^{241}Am spectrum

(b) Fit on the 59.5 keV X-ray spectrum.

Figure 6. (a) Energy spectrum of ^{241}Am measured by the DC module at 0°C. (b) Magnified view around the 59.5 keV X-ray peak. The curve represents the fit result described in the text.

(a) ^{57}Co spectrum

(b) Fit on the 122.1 keV X-ray spectrum.

Figure 7. (a) Energy spectrum of ^{57}Co measured by the DC module at 0°C. (b) Magnified view around the 122.1 keV X-ray peak. The curve represents the fit result described in the text.

the load capacitance is essential to achieve 1 keV energy-resolution. Further improvement in the amplifier noise performance is expected by further optimizing the front-end MOSFET geometry in the 0.35 μm process¶ or by employing a JFET as the front-end FET instead of a MOSFET. We also plan to employ a thicker DSSD to reduce the capacitance to the backside.

In conclusion, we have demonstrated that energy resolution of a DSSD system is as low as 1.3 keV with the possibility of the future improvements. Such an ultra low noise DSSD system presents great possibilities for future hard X-ray and gamma-ray telescopes, such as the SMCT.

ACKNOWLEDGMENTS

¶The current MOSFET geometry is optimized in the AMS 1.2 μm process.

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