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Stacking faults in boron-implanted silicon give rise to streaks or rods of scattered x-ray intensity normal to the stacking fault plane. We have used the diffuse scattering rods to follow the growth of faults as a function of time when boron-implanted silicon is annealed in the range 925° - 1025°C. From the growth kinetics we obtain an activation energy for interstitial migration in silicon: $E_I = 1.98 \pm 0.06$eV. The measurements of intensity and size versus time suggest that faults do not shrink and disappear but rather are annihilated by a dislocation reaction mechanism.

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In a previous grazing-incidence diffuse x-ray scattering study[1] of implanted and annealed silicon, we have shown that stacking faults generated by boron implantation and annealing at high temperature give rise to streaks or rods of intensity normal to the plane of the fault. It is evident that the integrated intensity in a streak is proportional to the stacking fault density or total stacking fault area. The width of the streak is inversely proportional to the characteristic size of the stacking faults. In this work, we have used the diffuse scattering from stacking faults to follow their growth kinetics upon annealing at high temperatures. From our study we obtain an activation energy for the growth process, allowing us to determine the mechanisms of stacking fault growth. The main advantages of the x-ray diffuse scattering method are that no special sample preparation is necessary, and that an x-ray beam a few mm in size effectively provides an average measurement of stacking fault density and size. These parameters could also be obtained by cross-section transmission electron microscopy[2] (TEM), but such measurements suffer from the usual sample statistics problem in electron microscopy unless a truly large sample distribution is investigated. For our case, plan-view TEM experiments were inconclusive, revealing a tangle of dislocations which obscured the stacking fault loops.

Floating-zone (001) silicon wafers were implanted with a boron dose of 5E15 cm^{-2} at 32 keV. 1cm square samples were then processed by rapid thermal annealing (RTA) for various times in the temperature range 925 - 1025°C. To investigate the defects introduced after annealing,diffuse scattering measurements were carried out using synchrotron x-ray diffraction in grazing incidence geometry. Since the implanted layer extends only about 2000Å from the crystal surface, the grazing incidence geometry was necessary in order to minimize background x-ray scattering from bulk silicon. The diffracting planes were normal to the (001) crystal surface. Radial and angular scans were taken in the vicinity of the (220) surface Bragg peak using a position-sensitive detector (PSD). A narrow slit in front of the PSD was used to restrict the resolution element in the $\mathbf{q}_{radial}$ - $\mathbf{q}_{transverse}$ plane to a value that is small compared to the width of the stacking fault streaks. Maps of scattering in the $\mathbf{q}_{radial} - \mathbf{q}_{z}$ plane at three values of annealing time at 975°C are shown in Figure 1. The intensity map shows the scattering around the (220) Bragg peak. The streaks of scattered intensity are accurately perpendicular[1] to (111) and $(\bar{1}\,\bar{1}\,1)$ crystal planes. It is known from TEM studies[2] that these faults are extrinsic in nature, each consisting of a circular loop of an extra plane of atoms surrounded by a Frank-type partial dislocation loop with 1/3{111} Burgers vector.

To measure the integrated intensity in these streaks we have performed transverse scans in the $\langle 1\bar{1}0 \rangle$ direction around fixed points (2.07, 2.07, 0) and (2.1, 2.1, 0). Typical transverse scans for various annealing times at 975°C are shown in Figure 2. Note that the intensity scale for the last plot at 110 sec is magnified by a factor of 30 compared to the other two. The area under these curves gives the integrated intensity, which is a measure of the concentration of interstitial atoms in the faults. For convenience we shall refer to this as the stacking fault density. The full width at half maximum (FWHM) is inversely related to the average size of the stacking faults. At 10 sec, the curve is clearly wider than that at longer heat treatment times.

Plots of the integrated intensity vs. time of annealing at various temperatures are shown in Figure 3(a). Typically the integrated intensity rises initially, reaches a maximum and falls at longer times to zero. Plots of the stacking fault diameter as a function of time at various temperatures obtained from FWHM measurements are shown in Figure 3(b). Like the integrated intensity, the faults initially grow in diameter and reach a maximum value of about 900 – 1000 Å. However, in contrast to the integrated intensity, the size does not decrease but remains around the maximum value while the intensity decreases.

We use the results shown in Fig. 3(b) to analyze the loop growth kinetics as a function of time and temperature. From this analysis we can determine such poorly-known parameters as the activation energy for interstitial migration, the activation barrier for the incorporation of an interstitial in the lattice on a stacking fault, and the volume density of stacking faults. Various treatments for the growth of stacking faults have been proposed. Here we use the treatment of Huang and Dutton[3] which has been implemented in TSUPREM4[4]. This approach is convenient since all of the information on the interstitials and vacancies introduced by the implantation process, and their subsequent annealing kinetics both into the bulk and to the surface, are incorporated into TSUPREM4. The rate of growth of the stacking faults is given by the following relation[3]:

$$\frac{dr}{dt} = \left(\frac{\pi}{N_O}\right)\left(\frac{r_t}{r_a}\right)^2 \exp\left[-\frac{E_B}{kT}\right] D_O \exp\left[-\frac{D_I}{kT}\right]\left(I - I^*_{LOOP}\right) \quad , \qquad (1)$$

where r is the stacking fault radius, N_O is the {111} planar atomic density of silicon atoms (1.57E16/cm^2), r_t is the radius of a torus surrounding the Frank partial dislocation of the stacking fault, r_a is the interatomic silicon lattice spacing, E_B is the activation barrier for loop growth, D_O is the pre-exponential factor for interstial motion, and D_I is the activation energy for interstitial motion. The interstitial concentration at the surface of the torus, I,

is determined for each time interval by solving the interstitial continuity equation for $\left(\frac{dI}{dt}\right)$. The continuity equation contains a term involving the loop density ρ (see Huang and Dutton[3] for details). I^*_{LOOP} is the equilibrium interstitial concentration within the torus and is derived by taking into account the elastic energy associated with the dislocation loop. It is given by

$$I^*_{LOOP} = I^*_I \exp\left[\frac{\gamma\Omega}{bkT}\right]\exp\left[\frac{\mu b\Omega}{4\pi rkT(1-\nu)}\ln\left(\frac{8r}{b}\right)\right] \quad , \qquad (2)$$

Where γ is the stacking fault energy (≈ 70 mJ/m^2 for silicon), Ω is the atomic volume for silicon, **b** is the Burgers vector for the Frank partial dislocation 1/3(111), μ is the shear modulus, r is the dislocation loop radius, and ν is Poisson's ratio.

In the computation procedure for integrating Eq. (1), we determined the optimum parameter for barrier height for an interstitial in the crystal to hop to a site on the stacking fault: E_B = 0.26 eV. Keeping this barrier height constant for all temperatures, we were able to fit the experimental data for the radius versus time at various temperatures within tight limits of the two other variables in the calculation, the loop density, ρ = 7.8 (± 5) E13 cm^{-3}, and the activation energy for interstitial motion, E_I = 1.98 ± .06 eV. The loop density is consistent with loop densities estimated from cross section TEM

observations. In Fig. 3(b) the fits are shown as lines; the points show experimental data. Typical error bars for the 975° C data are also shown. For the highest temperature (1025°C), the growth phase of the loops was too fast to be experimentally accessible and we have arbitrarily fitted the growth kinetics to the radius measured at the shortest time. Even in this extreme case the calculation parameters are consistent with the other three temperatures.

To put these relatively high temperature observations into context with defect structures observed at lower temperatures, we note that when implanted silicon is annealed in the temperature range 650° - 850°C, the initial extended defects formed are mainly rod-like[5] along <110> with a {311} habit plane. The {311} defects have been identified as an extra plane of self-interstitial atoms, with aspect ratios of length to width typically about 10. Upon annealing, the larger defects grow at the expense of the smaller ones. Their kinetics have been ascribed to an Ostwald ripening process. The net concentration of interstitials in the defects never increases, but always decreases with time of anneal. The interstial atoms released during annealing contribute to transient enhanced diffusion (TED) during the annealing process. Increases in the diffusion coefficient a thousand fold over the bulk silicon value have been reported[6]. However, the large {311} defects

themselves are unstable; they appear to be a precursor[5] to more-stable Frank-type dislocation loops.

In contrast to the annealing behavior in the intermediate 650° - 850°C range of temperatures, rod-like {311} defects are not observed when implanted silicon is annealed in the temperature range 900° - 1070°C. If rod -like defects do form, they nucleate and dissolve at rates too fast to be accessible to RTA times. For this relatively high implant dose, the primary defects observed in this range of annealing temperatures are Frank-type interstitial stacking faults with Burgers vector 1/3(111), and tangles of dislocations. However, in contrast to dissolution kinetics alone observed for {311} defects, we observe initially a growth of both the stacking fault density and size as a function of time at high temperature. In our case the stacking fault growth is limited by both reaction rate and diffusion. The reaction barrier we determined, E_B = 0.26 eV, is smaller than that assumed in previous work[7]. In that work, the activation energy obtained from the shrinkage of stacking faults introduced by oxidation (OSF) was observed to be 0.4 eV larger than that for self-diffusion; the difference was assumed to be the barrier height. In later experiments[8] the activation energy for OSF shrinkage was found to be 4.8 eV, equal to the activation energy for self-diffusion in silicon[9] . We believe that that the value for the barrier found in

this work, as well as the work of Huang and Dutton, is more realistic. The activation energy for interstitial motion, $E_I = 1.98 \pm .06$ eV, implies that the formation energy for interstitials is $E_F = 4.75 - 1.98 = 2.77$ eV, assuming that self-diffusion occurs primarily by the interstitial mechanism. This value $E_I = 1.98$ eV is a little higher than that inferred from a detailed study of zinc metal diffusion[10] in silicon, $E_I = 1.77 \pm 0.12$ eV. However the values are not statistically different.

Another marked difference in the behavior of stacking faults from the {311} defect kinetics is that they do not shrink in size when they disappear. In fact, the size of the faults remains the same while the stacking fault density decreases and ultimately vanishes. The only way this could occur is through a dislocation reaction mechanism such as:

$$1/3\langle 111\rangle + 1/6\langle 11\text{-}2\rangle \rightarrow 1/2\langle 110\rangle \quad .$$

Here, a $1/6\langle 11\text{-}2\rangle$ Shockley partial nucleates on a Frank partial dislocation, sweeps through the fault and leaves a perfect dislocation loop with Burgers vector $1/2\langle 110\rangle$. In this reaction, the energy of the dislocations involved remains the same, but there is a resultant reduction in energy since the stacking fault energy is removed. Evidence for the transformation of Frank partials to perfect dislocation loops has been reported in many systems including Si.

While the enhancement in boron diffusion upon annealing at these higher temperatures is orders of magnitude less than at the lower temperature range, it can still be appreciable. For our case at 975°C, the enhancement is about a factor of 15 from SIMS measurements, rather than the thousand–fold increase at lower temperatures. We suggest that this can be attributed to the fact that interstitials tied up in the stacking faults and subsequently in the prismatic loops are not available for the enhancement of boron diffusivity at higher temperatures.

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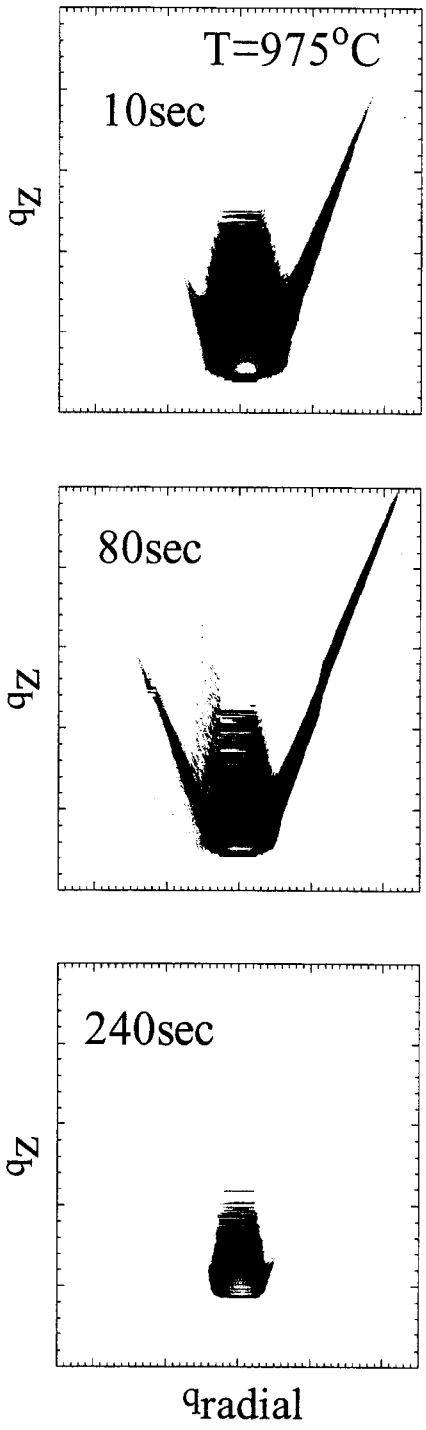
FIGURE CAPTIONS

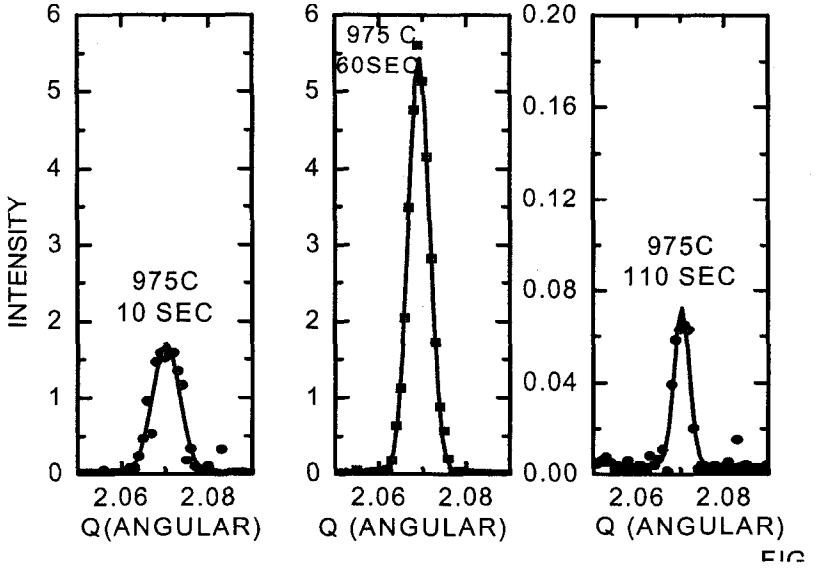
Figure 1. Diffuse scattering intensity in the $\mathbf{q}_r - \mathbf{q}_z$ plane for silicon implanted with a boron dose of 5E15 cm^{-2} at 32 keV, and RTA annealed at 975^{O} C for the times shown. Note the growth and decay of the rod-like streaks.

Figure 2. Angular scans through the streaks at (2.07, 2.07, 0) showing the initial increase and the final decrease of intensity with time of heating at 975^{O} C. Note that the scale for the 110 sec curve has been magnified by a factor of 30.

Figure 3. (a): Integrated intensity of the streak scattering versus time of anneal at the temperatures shown. (b): Stacking fault diameter derived from the width of the streak. Note that while the integrated intensity grows, reaches a maximum and subsequently decreases at long times of anneal, the stacking fault diameter grows and stays at it's maximum value even as the intensity falls to zero.



PATEL FIG. 1


INTENSITY
6
5
4
3
2
1
0
975C
10 SEC
2.06
2.08
Q(ANGULAR)
975 C
60SEC
Q (ANGULAR)
0.20
0.16
0.12
0.08
0.04
0.00
975C
110 SEC
Q (ANGULAR)

PATEL FIG. 2

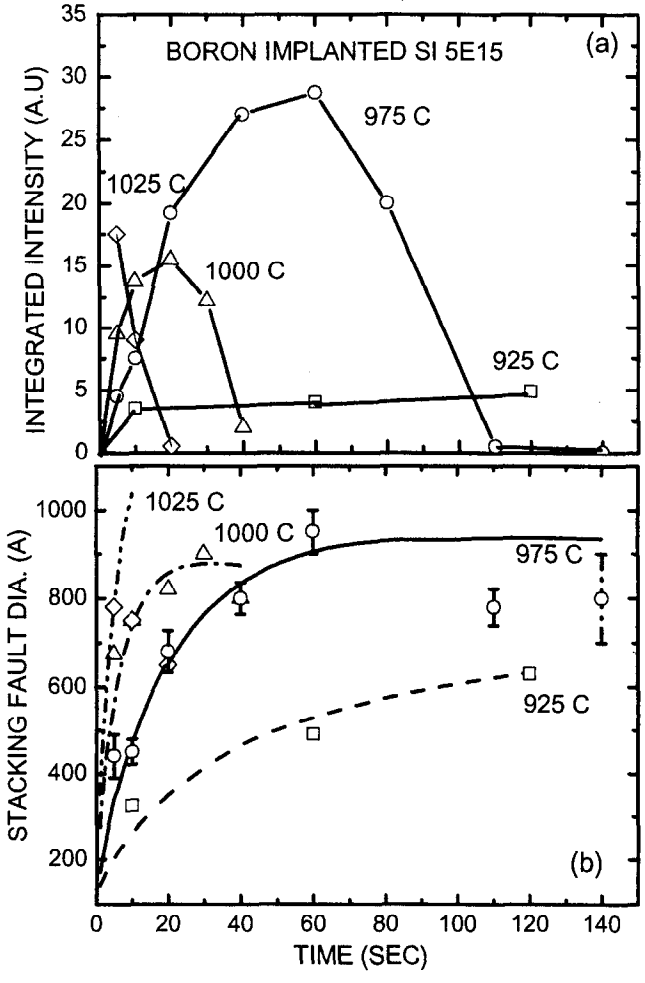


FIG. 3

PATEL FIG. .3