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The publication of the ICFA Instrumentation Bulletin is an activity of the Panel on Future Innovation and Development of ICFA (International Committee for Future Accelerators). The Bulletin reports on research and progress in the field of instrumentation with emphasis on application in the field of high-energy physics. It encourages issues of generic instrumentation.

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Cover: The illustration depicts L. J. Waghenaer's marine atlas, "The Mariner's Mirror," published in 1588. Lucas Janszoon Waghenaer was born in Holland in the 1530s. He became a famous ship pilot in his time. In 1584, he published the atlas ("Spieghel der Zeevaerdt") which was greatly valued among mariners for centuries. This was not due only to the map content, but also to the detailed knowledge of navigation techniques of that time. The atlas, as it appears on our page, is the same one used for the Dutch to English translation.

1997-1998 Conference List

- 7th International Workshop on Low Temperature Detectors (LTD 7)
  28 Jul. - 1 Aug. 1997 , Munich, Germany

- 7th International Workshop on Polarized Gas Targets and Polarized Beams
  18-22 Aug. 1997 , Urbana, IL

- 6th International Workshop on Vertex Detectors (VERTEX 97)
  31 Aug. - 5 Sep. 1997 , Mangaratiba, Brazil

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Radiation Damage in CCDs used as Particle Detectors

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February 1997

Introduction

CCDs sensitive to minimum-ionizing particles (hereafter referred to as min-I particles) have found a niche as very high precision tracking devices, used as vertex detectors for the detection of short-lived heavy flavor quarks or τ leptons, in high energy physics experiments [1-3]. As such, they must be located as close as possible to the interaction point (usually starting within 10 or 20 mm). In this environment the capability of these pixel-based devices to tolerate very high hit densities (typically $\sim 1 / \mathrm{mm}^2$) is an important attribute. However, this environment may be quite demanding as regards radiation hardness, a situation also encountered by users of imaging CCDs in industry (nuclear, X-ray and electron microscopy, for example), for space-based optical and X-ray telescopes, etc. Radiation damage in these complex silicon devices is therefore relevant to numerous application areas and has been studied for many years [4-16]. Reference [11] provides a particularly valuable review. Despite being 17 years old, it remains the most comprehensive general paper on this subject.

Despite this extensive bibliography, there is no simple picture that summarizes radiation effects of concern to all CCD users, for two reasons. Firstly the uses made of these devices are highly variable. To a particle physicist (who is interested in the tracking precision given by the centroid of a min-I cluster) a 10% loss of signal (as long as it is slowly varying across the detector area) would not be serious. To an X-ray astronomer, using the cluster signal amplitude to determine the X-ray energy, such a degradation would be disastrous. Secondly, the radiation sensitivity depends strongly on the operating conditions, such as integration time, readout speed, etc. These conditions may be imposed by external factors peculiar to a specific application. For example, the limitations on operating temperature and power dissipation of space-based systems are likely to be more restrictive than in terrestrial applications.

In this paper an attempt is made to focus on the issues relevant to the particle tracking/vertex detector application, leaving aside issues of great important to other users.

Surface Damage

With regard to surface damage effects due to all forms of ionizing radiation (charged hadronic and electromagnetic) we can be brief. Process improvements over the years have reduced the build-up of

interface charge, and CCDs (having on-chip gain less than unity, unlike microstrip detector readout ICs) are relatively insensitive to such effects. There is a level shift as the signal is transferred from beneath the polysilicon gate structure (uniformly affected by interface charge build-up) onto the output node, whose potential is directly set by the external reset bias V_{RD}. As the radiation dose builds up, it may become necessary to raise V_{RD} to match the shift in buried channel potential. This has a knock-on effect to the drain voltage V_{DD} of the output transistors, in order to maintain the charge-sensing circuit at full gain. This procedure would eventually be limited by the breakdown voltage of the MOSFET to substrate. 'Standard' CCDs show voltage shifts due to trapped charge at the Si / SiO_2 interface of about 1 V/100 kRad, with half this for radiation tolerant devices having thin dielectric gate insulators, and around 0.1 V/100 kRad for experimental devices, soon to become generally available. Thus with modern radiation-hard dielectric, the practical limit can be >1 Mrad of ionizing radiation, which is entirely adequate for all CCD vertex detector applications in the past or contemplated to date. Incidentally, these voltage shifts are much smaller if the CCDs are powered off during irradiation (giving enhanced electron-hole recombination in the dielectric) but this option is not generally applicable in HEP applications, apart from beam-tuning periods. As well as causing flat-band voltage shifts, the interface states produced by ionizing radiation act as sources of electron-hole generation, i.e., increased dark current. In HEP applications, there is no reason not to design the tracking detector for operation at cryogenic temperature, so reducing the dark current to completely negligible levels.

Bulk Damage

Regarding bulk damage, we need to consider the effects on dark current, charge collection efficiency and charge transfer efficiency. Even in heavily irradiated CCDs, the excess dark current can normally be dealt with by modest cooling. Given the thin epitaxial layer (~20μm) from which the min-I signal is collected, the requirements made on minority carrier lifetime are not severe, and there is essentially no problem with charge collection into the potential wells. However, once the electron charge packet starts its long journey to the output node (possibly several centimeters, ~2000 pixels), the situation is far more dangerous. At every location where the charge packet is momentarily stored (and there are three such locations for every pixel of a 3-phase CCD) there is a finite probability that some of the signal charge may be trapped, leading to less-than-unity charge transfer efficiency CTE. Use is also made of the quantity CTI (=1-CTE), the charge transfer inefficiency. In order not to seriously degrade the signal-to-noise performance, the average CTI of a tracking detector in a large instrument should typically not exceed $\sim 10^{-4}$.

The *n*-channel being relatively highly doped, the generation of bulk defects is considerably simpler than for the high resistivity material required for microstrip detectors, being closely similar to that encountered in electronic devices. The primary products of bulk damage are vacancy/interstitial pairs. Indeed, in the case of electromagnetic irradiation, these pairs (in the form of point defects) represent the

complete picture. For hadronic interactions, the large energy transfer to the silicon atom results in damage clusters (local regions of the crystal having dimensions typically hundreds of Angstroms in longitudinal and transverse dimensions). These clusters constitute highly disordered regions within the crystal, and may be a source of mobile vacancies, di-vacancies etc. In the heavily doped CCD *n*-channel, the majority of active defects are formed from the capture of mobile vacancies by phosphorus dopant atoms (the Si-E center). These form positively charged donor-like defects when empty, with an energy level E_{tr} of 0.44 eV below E_c, the edge of the conduction band. In the case of electromagnetic irradiation, the Si-E center is probably the only significant defect generated. These defects have a high probability of capturing signal electrons which come within their electrical sphere of influence. Let us consider this case, a single type of bulk trap which is randomly distributed within the *n*-channel. This situation is described by a restricted case of the general Shockley-Hall-Read theory of carrier capture and emission from traps, in which only capture and emission of electrons from/to the conduction band plays a part. Hole capture and emission are irrelevant since we are concerned with donor-like traps in depleted material. This situation has been considered by various authors [4, 7, 12, 14].

Let us first take a qualitative look at the situation. As the charge packet is transported from gate to gate (within a pixel or between neighboring pixels) *vacant* traps that lie within the storage volume of the charge packet will tend to capture electrons. If the traps are already filled (either fortuitously, due to the passage of an earlier signal packet, or deliberately for this purpose by the injection of an earlier 'sacrificial' charge packet) they will permit the signal electrons to pass undisturbed. Also, if the signal packet is transported at a sufficiently high clock rate that the dwell time τ_g under any gate is small compared to the trapping time constant τ_c, the signal electrons will pass. Also, if the trap emission time constant τ_e is small compared with the clock pulse rise/fall time τ_r, the trapped electrons will be re-emitted in time to rejoin their parent charge packet. Only if electrons are *trapped and held long enough* to be re-deposited in the next or later potential well, does the process contribute to a loss of CTE. This is evidently a multi-parameter problem with some room for maneuver.

Let us now look at the process quantitatively.

Assuming all traps initially empty, the CTI is given by

$$\mathrm{CTI} = \sum_{j=1}^{N_F} F_j \times \frac{N_{tr}}{N_s}\left[1-\exp\left(\frac{\tau_r}{\tau_e}\right)\right];$$

N_F is the number of phases per pixel (3 for a 3-phase structure).

F_j is the fill-factor for phase j, i.e., the probability that a trap in the charge packet storage volume will become filled during the dwell time.

$$F_j = 1-\exp(-\tau_g / \tau_c).$$

For most cases of practical interest τ_c is of order of magnitude 10 ns and F_j may be taken to be unity. N_{tr} is the trap density and N_S, the signal charge density, is a function of the signal size, but is effectively constant (and approximately equal to the *n*-dopant concentration) for charge packets larger than approximately 1000 e^- [14]. For smaller charge packets, the effective signal density is reduced, and the CTI is correspondingly degraded. For very small charge packets of N_e electrons, one expects $N_S \propto 1/N_e$ since the signal electrons will occupy a constant volume determined by their thermal energy and the 3-dimensional potential well in which they are stored.

Now

$$\tau_e = \frac{\exp[(E_c - E_{tr})/kT]}{\sigma_n X_n \nu_n N_c}.$$

The terms in the denominator are in turn the electron capture cross-section for that trap type, an entropy factor, the electron thermal velocity and the effective density of states in the conduction band. The numerator tells us that for shallow traps (or high temperature) τ_e is likely to be short, and conversely for deep traps and/or low temperatures, τ_e is likely to be long. In fact, for deep traps and appropriate clock times, by reducing the temperature, one can sweep the CTI through its full range from approximately zero (since the charge is re-emitted into the parent pixel during the drive pulse risetime) to $3N_{tr}/N_S$ (for a 3-phase CCD) and back to zero, as all traps are filled by some long preceding deliberate or accidental charge packets to have been clocked out of the device. Figure 1 nicely illustrates this point.

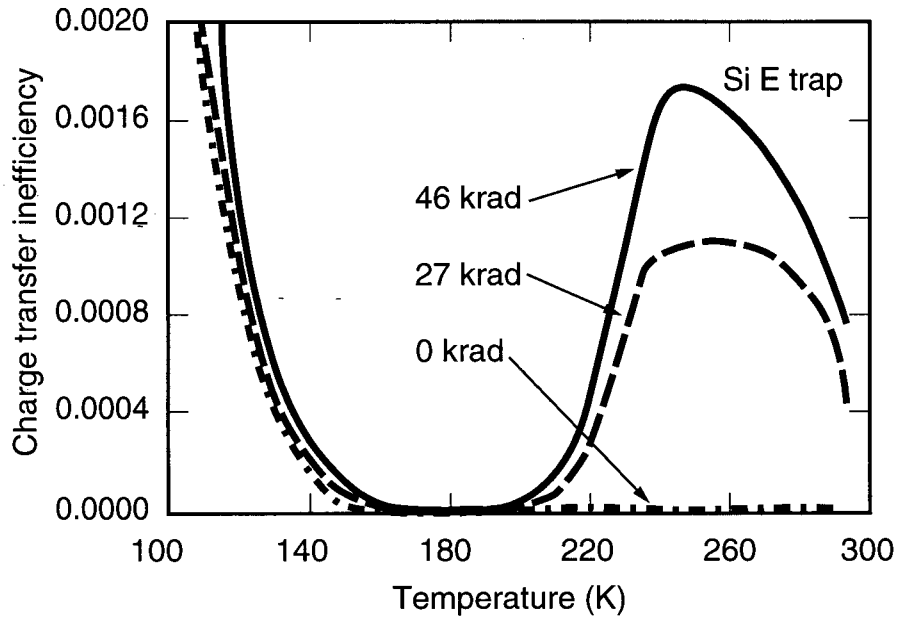

Fig. 1 From reference [14], effect of ionizing radiation damage on CTI, as function of operating temperature. (^{90}Sr β source)

This demonstrates the growth in CTI due to irradiation of a CCD with a radioactive β source. The density of Si-E centers increases, but the effect on CTI can be minimized by operating at or below 190 K, where the trap emission time becomes adequately long. The degradation in CTI below 160 K (even before irradiation) is not seen in later CCDs from the same manufacturer. It probably represents an artifact of the register design or processing of this particular device. In practice, one can normally reduce the operating temperature to ~85 K before the CTI rises to $\sim 10^{-4}$ at the onset of carrier freeze-out, the trapping of signal electrons by the phosphorus donor ions [12]. This sets an effective lower limit to the useful operating temperature of *n*-channel CCDs.

For hadronic irradiation of CCDs, because of the much greater non-ionizing energy loss or NIEL factor, the damage rates are greatly increased. In addition, several donor-like defect levels have been identified. The Si-E center (VP) still forms the predominant and deepest trap, though 15% of this deep trap is believed due to the di-vacancy (VV) [16]. Shallower traps at $E_c - 0.30$ and $E_c - 0.12$ eV are also observed [8, 16]. Protons are particularly damaging (due to the large p-Si Coulomb scattering cross-section) and Fig. 2 shows the CTI resulting from an irradiation with the very modest dose of 3.6×10^9 10 MeV proton/cm^2.

While these proton damage results are of great importance for their particular application area (space-based X-ray cameras) they probably give a pessimistic impression for the conditions relevant to particle detection systems, for two main reasons. Firstly, these results refer to very low signal densities, so the benefits of the long trap emission times at low temperature are not exploited to the extent possible in a particle physics experiment. Secondly, the only hadronic background likely to be significant at an e^+e^- collider are neutrons leaking through shielding. There is evidence that neutrons may be much less harmful than would be inferred from these proton data.

Taking the standard NIEL factor, the data of Fig. 2 correspond to an equivalent dose of 1 MeV neutrons of 3×10^{10} n / cm^2. Yet there are measurements on *n*-channel CCDs (buried channel) [5, 6], which demonstrate CTI $< 10^{-4}$ for 10^{12} n / cm^2 at room temperature. Most significantly [6], at a temperature of 84 K and 30 ms between bursts of charge injection, the CTI of 10^{-4} is achieved for 10^{13} n / cm^2 (1 MeV equivalent). The clocking conditions between these experiments are quite different (protons in parallel register clocked very slowly, neutrons in linear register clocked at 500 kHz) but this should not be critical. The low temperature performance should be driven by the time between charge injections, and 30 ms would be quite realistic for an HEP experiment. There is the further difference that the neutron studies have all been made with large signal packets, but as already discussed, this should become an issue only if the packet size falls below ~1000 e^-, where the signal charge density falls significantly below the dopant level in the *n*-channel.

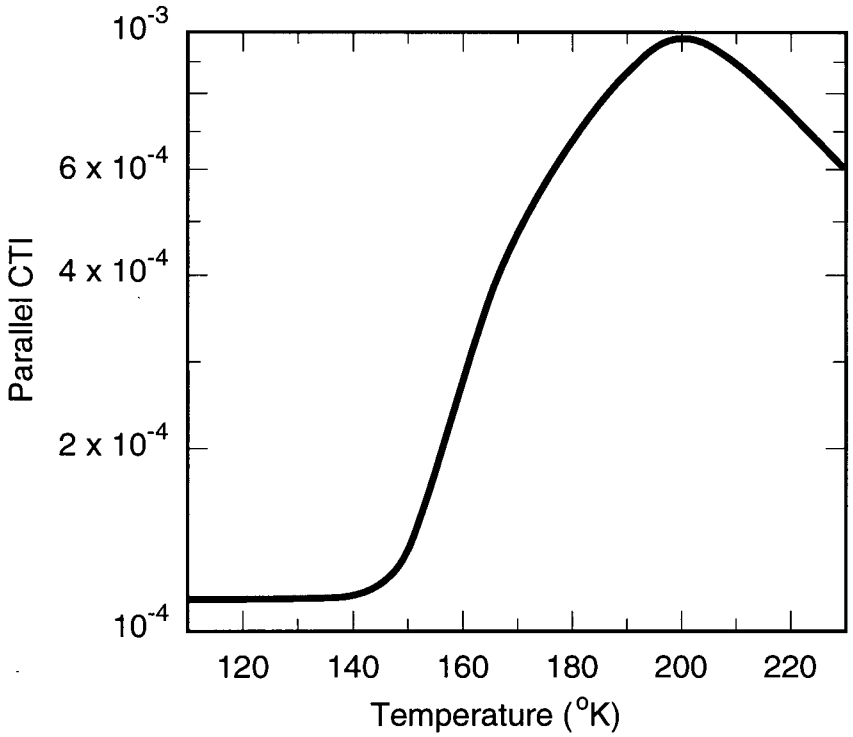

Fig. 2 From reference [16], effect of hadronic radiation damage on CTI, as function of operating temperature. (10 MeV protons)

Conclusions

Due to their long readout time, CCDs are not applicable as vertex detectors in continuous high flux environments such as LHC. They have a proven record in fixed target experiments (where the incident beam can be interrupted during the readout) and in the e^+e^- linear collider environment, where the interval between bunches (or between bunch trains) allows time for readout. In both these environments, radiation damage effects have so far been modest. In the fixed target environment, given the small number of CCDs required, they can simply be exchanged at intervals of 6 months or so. For the e^+e^- collider, with reasonable care over beam conditions, the detector lifetime can be many years.

For the future e^+e^- linear collider, the backgrounds may be substantially higher. The dumps for secondary e^+e^- pairs, for beamstrahlung and for the residual main beam, are all significant sources of neutrons. At this stage, it is not clear if any of these could cause problems for a CCD vertex detector. As we have seen, there is a possible discrepancy between the radiation damage data with neutrons and with protons, as regards charge transfer efficiency, so the actual performance limits for a CCD detector are far from clear.

What is long overdue is a comprehensive study of the radiation effects in one CCD design, comparing electromagnetic, neutron and charged hadron irradiation, with particular attention to the

operating conditions (clocking, charge injection interval and temperature), covering the region of interest for particle detection. It should be noted that very high clocking rates for the readout register (~50 MHz) are envisaged for this environment. This will provide a significant suppression of CTI in this register due to the fact that τ_g will no longer be much larger than τ_c, so the above-mentioned fill factor can be far from unity. Equally important as these systematic studies of radiation effects is a serious evaluation of neutron background conditions likely to be encountered at the future e^+e^- linear collider (the next likely application area for a large scale CCD vertex detector). This work will reveal if there are any problems with the continued use of currently available CCDs in our field. Should there be difficulties with the anticipated neutron fluxes, there may be considerable room for improvements in the CCD design. The most obvious step (analogous to the use of hetero-structures in radiation hard GaAs electronics) would be to reduce the storage volume for the charge packets. This is possible in both dimensions orthogonal to the transfer direction, by the techniques of a narrow channel, and a highly doped shallow channel. It should be remembered that for min-I detection, a pixel well capacity of 10^4 e^- would be entirely adequate; on current CCDs the signal charge floats around in a vastly excessive storage volume. Another option would be to consider *p*-channel devices, for which the Si-E center would be avoided. There is some evidence [10] that such CCDs do have enhanced radiation hardness, though this has not been studied with neutrons.

In short, there is currently a need for background simulations and for measurements with neutron irradiation of modern CCDs, to determine if the future linear collider presents significant radiation damage problems for a CCD-based vertex detector. Should there be such problems, the CCD designer has a variety of tools at his disposal with which to improve the radiation hardness of his designs. Many of these ideas will in any case be developed for non-HEP applications in radiation environments, but the conditions specific to a particle tracking detector do present opportunities that would not be universally available.

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Silicon Microstrip Detectors in High Luminosity Application

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Abstract

The development of silicon microstrip detectors for high luminosity application at the Large Hadron Collider (LHC) is described. The technical choices are most severely restricted by the anticipated radiation damage. The arguments are presented which led to the selection of the base line detectors for the silicon tracker of the LHC detector ATLAS: sandwiches of single-sided detectors of n-strips in n-type bulk.

1. INTRODUCTION

The advent of high luminosity colliders requires special instrumentation in High Energy Physics [L1-L3]. High rates can lead to a pile-up of events and increased dead time. For the readout electronics, this means the use of much shorter shaping times than one would use to optimize the power consumption and the signal-to-noise ratio. In addition, most detectors have been subdivided into many more channels to reduce the confusion of signals. A new problem at the hadron colliders is the increased radiation levels. Already at the Main injector upgrade at FNAL and even more so at the Large Hadron Collider, radiation damage dictates compromises in many detector subsystems. This applies especially to semiconductor detectors, which, due to their relatively high cost and extremely good position resolution are commonly employed close to the interaction region where the radiation levels are highest.

As described below in detail, the layout of tracking devices based on silicon detectors is severely constrained: they have to be located such that they can survive the radiation for the life time of the experiment [T1, T2]. In the same context, a silicon tracking detector which is more radiation hard allows the detectors to be moved closer to the interaction region, improving the performance in vertexing and momentum resolution and reducing the area of the tracker, and therefore the cost. Thus it is not surprising that the silicon strip detectors developed for ATLAS SemiConductor Tracker (SCT) [T2] are different than the ones developed for low-luminosity applications such as LEP [T4] or even BaBar [T5], where only ionizing radiation is present.

In this report, the basic functioning of silicon microstrips will be explained first, followed by discussion of radiation damage in silicon detectors. The layout of the ATLAS SCT will be

presented, and design features of the detectors highlighted which are specific to the operating conditions at the LHC. The projected performance of both irradiated and non-irradiated detectors will be detailed, based on beam test measurements.

2. BASICS of SILICON MICROSTRIP DETECTORS [Refs. D1-D3]

Silicon detectors are made from near intrinsic bulk having both low-ohmic donor implants (the n-side), collecting electrons, and low-ohmic acceptor implants (the p-side), collecting holes. The n-side signal is mainly due to drifting electrons collected in ~8ns, (for the usual 300 μm thickness and with bias above the depletion voltage). The p-side signal is mainly due to drifting holes with a three times longer collection time, due to the larger mobility. One side has a junction, the other is ohmic. The location of the junction depends on the type of the bulk: it is on the p-side in n-bulk and the n-side in p-bulk. Charge is collected only from the depleted region, which starts at the junction side when the bias voltage is raised from zero, and reaches the full thickness of the detector at the depletion voltage. Single-sided detectors have only one side divided into strips which are read out, double-sided detectors have both sides divided into read-out strips. Most (all?) silicon detectors are made of high-ohmic n-bulk with resistivity of about 5 kΩ-cm, determined by a small fraction (10^{12} per cm^3) of donor atoms. The distance between strip centers, the pitch, is of the order of 50 μm, and thus of the same order of magnitude as the feature size of VLSI chips. This has facilitated the development of read-out electronics which is directly wire-bonded to the strips and helps in the data compression of the large number of channels [E1-E9].

The original single-sided detectors had the p strips implanted in n-bulk and coupled directly to the read-out electronics. Later, AC-coupling was developed which decoupled the DC current and the biasing potential from the front-end electronics. This made the use of double-sided detectors feasible, which are an economical and low-mass technical choice [D2]. Yet, the LHC experiment ATLAS has chosen as the baseline a sandwich of single-sided detectors with n-implants in n-bulk, glued back-to-back. The reason is the expectation that they will present better performance after severe radiation damage predicted for LHC operations.

3. RADIATION DAMAGE in SILICON STRIP DETECTORS [Refs. R1-R8]

3.1 Surface Damage [Refs. S1-S6]

Ionizing radiation deposits charges on the surface of silicon strip detectors, which change their electrical properties. The processing of the surface, and the existence of oxides or nitrides can be a factor in the extent and consequences of the damage. When exceedingly large dose rates were used, increased leakage currents were observed due to charge-up of the surface, which annealed out in less than an hour at room temperature [E3, R7]. These effects are difficult to

quantify and we have dealt with them by performing a beam test at particle fluxes and operating temperatures anticipated for the LHC (see Sec. 5).

A more lasting damage to the surface is due to the accumulation of charges in the interface between the silicon oxides and the silicon bulk, where there is a lattice mismatch. The interface states are filled in ionizing radiation and saturate after a total dose of the order of 100 kRad [S1]. The important detector parameters which can be influenced by the existence of these oxide charges are bias resistance, inter-strip resistance and inter-strip capacitance.

Polysilicon bias resistors are radiation hard [S1], while those using an accumulation layer or the punch-through effect are changed drastically with radiation [S3, S6]. Moreover, the punch-through resistors introduce excess noise [S6, R7].

The inter-strip resistance is crucial for the isolation of the strips, and has to be much larger than the biasing resistor. The isolation is a problem on the n-side (ohmic side) before radiation due to the existence of a conducting accumulation layer of electrons below the normal oxide charges, but can be cured by implanting p-material as isolation ("p-stops") [D2]. After irradiation, when the bulk inverts [see below] and the junction is on the n-side, this problem vanishes. The p-side in turn does not have the accumulation layer after inversion and has good isolation.

The inter-strip capacitance is important because it tends to be the largest contributor to the parasitic capacitance responsible for amplifier noise. In the absence of free charges, it can be estimated fairly reliably from the geometry of the strip detector and is a function of the ratio strip width over strip pitch [C1-C4]. The existence of free charges on the n-side before inversion causes the capacitance to depend on the bias voltage and one reaches the minimum "geometrical" value only with large over-voltage.

Surface currents due to the oxide charges have been observed, but they are much less important than the bulk currents for charged particle radiation [S1, S4, S5].

3.2 Bulk Damage [Refs. I1, A1-A3]

The bulk is damaged mainly by displacement ["Non-ionizing Energy Loss" (NIEL)] [F1]. Hence hadrons and heavy ions damage more than electrons and photons. Two major effects are observed: an increase in leakage current due to the creation of deep acceptor levels and a change in the depletion voltage due to the change in effective doping concentration.

a) Increase in Leakage Current

The leakage current is due to a thermal generation of electron-hole pairs. It varies exponentially with the operating temperature. Due to the creation of deep traps which occupy the middle of the band gap [R8], radiation increases the leakage current i proportionally with the displacing fluence ϕ and the volume Vol

$$i = \alpha \cdot \phi \cdot Vol \quad ,$$

with $\alpha \approx 3*10^{-17}$A/cm after annealing. A large part of the current seems process dependent, but anneals out very fast. The leakage current is the reason why AC coupled detectors are used, which block the current from the amplifier input. But it also causes stochastic noise in the amplifier, proportional to the square root of the product of leakage current and shaping time. The allowable current limit for fast shaping times is about one μA per strip.

b) Change in Depletion Voltage [Ref. I1]

The depletion voltage V_{dep} depends on the effective doping concentration N_{eff} and the square of the detector thickness d:

$$V_{dep} = \frac{e \cdot |N_{eff}| \cdot d^2}{2 \cdot \varepsilon} \quad .$$

Thus a radiation induced change in the doping concentration causes a change in the depletion voltage [I1]. The effective doping concentration is changed in two ways: donor removal and acceptor creation, and both make the bulk more p-type. The donor removal is exponential, while the acceptor creation is linear in the fluence ϕ [Fig. 1].

$$N_{eff} = N_0 e^{-c\phi} + \beta\phi \quad .$$

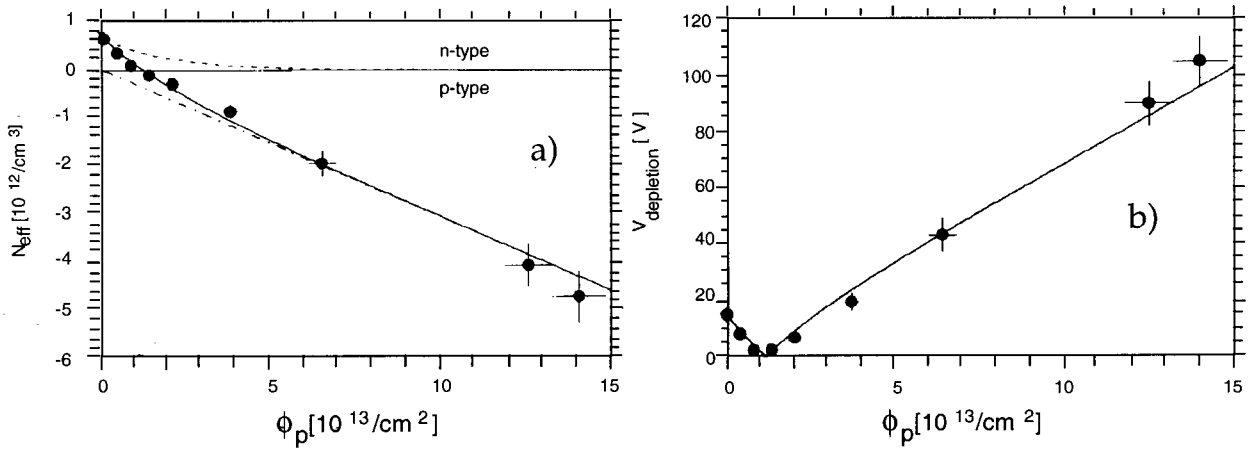

Fig. 1 Radiation damage in a 170μm thick n-bulk photo diode as a function of proton fluence ϕ_p:
a) effective doping density, b) depletion voltage (Ref. I1). For 300 μm thick detectors, the depletion voltages would be about three times as high.

At a certain fluence, about $\phi = 1*10^{13}$p/cm^2 in Fig. 1, the remaining donors are balanced by the newly created acceptors and the detector is intrinsic with zero depletion voltage. For larger fluences, the acceptors dominate and the detector is inverted, *i.e.* p-type, and the detector is said to have undergone "type inversion". For large fluences, the depletion voltage increases linearly with fluence, and is independent of the pre-rad value.

c) Annealing [Refs. A1-A3]

The radiation induced changes in detector properties are initially not stable, but exhibit strong annealing, which is temperature dependent. This means that the increased leakage currents and the modified doping concentration change even after the irradiation has finished. For example, at room temperature, the leakage currents decrease by about a factor of two in a few weeks. The annealing of the doping concentration is more complicated: there are three different effects with different time constants: there is first a constant term; then a short term annealing governed by τ_S, which is beneficial because it reduces the depletion voltage; and a long-term reverse- ("anti") annealing effect due to the release of meta-stable acceptors, which increases the depletion voltage with a characteristic time τ_L. Fig. 2 shows the depletion voltage both during irradiation and annealing for two different operating temperatures.

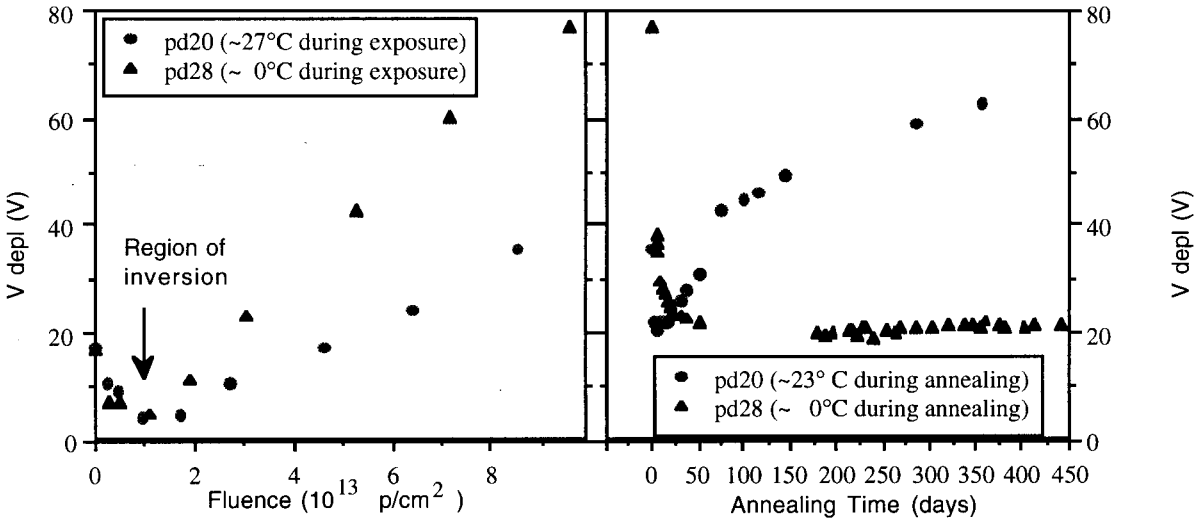

Fig. 2 The depletion voltage of 170 μm thick Hamamatsu photo-diodes as a function of fluence and as a function of annealing time for 0°C and room temperature operation. The last points on the left hand plot correspond to the first points on the right hand plot (Ref. A1).

In good approximation for the fluences at the LHC, the three components, stable, short-term, and long-term annealed, respectively, are proportional to the fluence ϕ

$$V_{dep} = \phi [v_z + v_s e^{-t/\tau_s} + v_s (1 - e^{-t/\tau_L})] \quad .$$

The annealing times are both exponential functions of the temperature and the long annealing time τ_L is about 200 times longer than the short anneal time τ_S. After a fluence of $\phi = 1*10^{14}$p/cm^2, a typical fluence for 10 years of LHC operation, the constant term in the depletion voltage is about 100V, the short-term annealing term is about 300V and the reverse annealing term is also 300V. Thus, depending on the operating temperature, the depletion voltage can vary between 100V and 400V! This is illustrated in Fig. 3, where the depletion voltage for different

detectors irradiated to the same fluence of about $5*10^{13}p/cm^2$, but annealed out at different temperatures is shown: the detectors annealed out at elevated temperatures are reverse-annealed out completely to about 230V, while the detectors operated at 0°C or below are still in the first phase of short-term annealing.

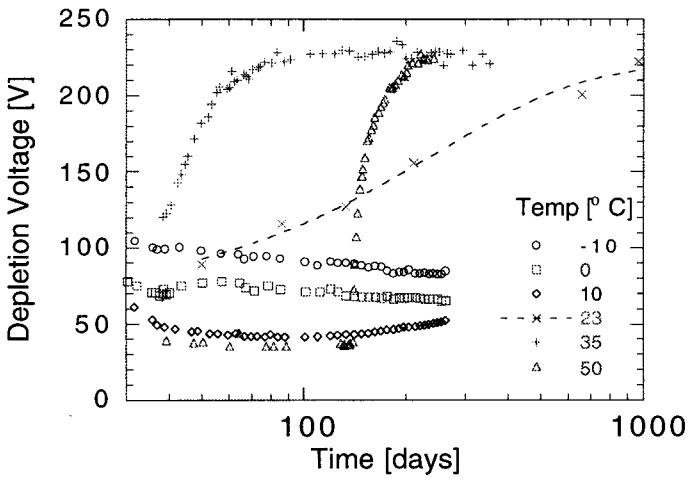

Fig. 3 Temperature dependence of the annealing of the depletion voltage for photo diodes irradiated with about $5*10^{13}$ p/cm^2. The detector at 50 °C was kept at -20°C until day 140. (Ref. A1)

d) Consequences for the Operation of Silicon Detectors

In order to conserve power, and for safe operation, the depletion voltage should be kept as low as possible. Over the lifetime of the detectors at LHC, the detectors will be subjected to fluences in excess of $10^{14}p/cm^2$. The depletion voltage will change from the initial pre-rad value of about 50V to zero to a final value which depends both on the fluence and the operating temperature. Type inversion (see above) occurs at a fluence of about $10^{13}p/cm^2$, i.e., after one year at full LHC luminosity. Given that the damage constants are proportional to the fluence received by the detector, the only additional parameter which controls the depletion voltage is the operating temperature. It has to be kept low to prevent the reverse annealing, but to allow the short-term annealing to take place during the lifetime t of the detector:

$$\tau_S << t << \tau_L \ .$$

For the life time of the LHC detectors of about t = 10 years, this corresponds to an operating temperature between -5 and -10°C [R3]. Access scenarios which result in warm-up of the irradiated detectors have to be evaluated carefully. For example, warming up the detectors every year for 7 days from -10° to +20°C , instead of keeping the operating temperature constant at -10°C, will increase the depletion voltage by 40% .

As mentioned before, the leakage current is a noise source. Short shaping times are required, in addition to the low temperature to minimize the current [E2]. The leakage current produces heat, which has to be removed. Due to the exponential temperature dependence of the leakage current, the self-heating has to be controlled carefully in order to avoid thermal run-away, which puts severe requirements on the cooling system (see below) [H1].

It should be noted that there have been investigations using different bulk materials. One idea was to use p-material, with n-implants. It has the advantage that there is no inversion during the detector life time due to radiation damage: the junction stays on the n-side, and the quality control of the detectors is simplified [Z1]. Unfortunately, there is much less experience with p-bulk processing and more importantly, the radiation damage constants for p-bulk are not much different than for n-bulk [R4, R5]. Another idea was to use lower resistivity n-bulk material for the detector, which increases the initial pre-rad depletion voltage and shifts the inversion point to higher fluences [R1]. Given that the depletion voltage at very large fluences is determined by acceptor creation and not by the removal of donors, the ultimate depletion voltage is the same for both high- and low-ohmic material.

4. DESIGN and LAYOUT of the ATLAS SCT DETECTORS [Refs. T1, T2]

Uncertainties in predicting the dose and operating temperature require that the detectors be designed with "head room", *i.e.*, enough margin in performance to minimize degradation due to unforeseen conditions. Although there have been many years of experience with silicon detectors for example at LEP [T4], detectors have been used in high rate and high radiation environment is only in the SVX at the FNAL Collider [S6] and the LPS at HERA [E3].

The ATLAS SCT chose a sandwich of single-sided n-on-n detectors as the base line, instead of double-sided detectors. Figure 4 shows the main features: two 6 cm x 6 cm detectors are bonded together to make 12 cm read-out strips and are then glued back-to-back with another 12 cm long pair, with a 40 mrad stereo angle. The electronic readout is straddling the center of the module, to minimize the noise contribution from the strip resistance [N2]. The pitch of the detectors is 80 μm, with narrow (≈ 16 μm wide) implants to minimize the inter-strip capacitance [C2, C4].

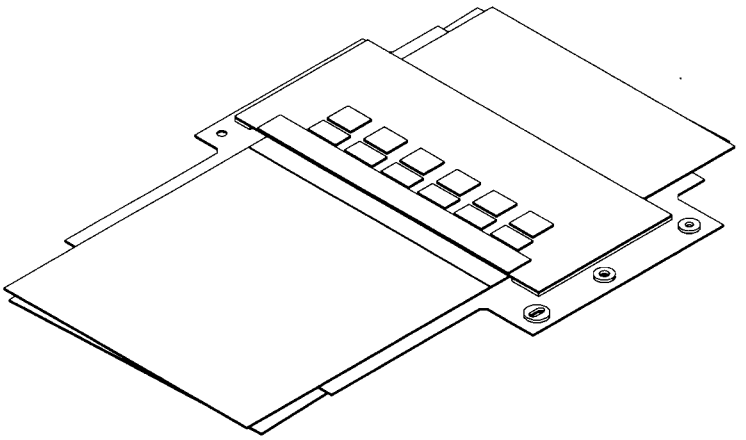

Fig. 4 The ATLAS SCT silicon module consisting of pairs of silicon detectors glued together back-to-back.

A certain amount of conservatism should be applied when extrapolating the finding of short-term R&D to detector designs which will be operated for 10 years in ATLAS. The prediction [Refs. F1-F4] for the depletion voltage for the innermost SCT layer at 30 cm radius varies from 150V to 250V, depending on the assumptions. In the forward region, the expected values are between 300V and 500V. There is considerable uncertainty in the depletion voltage prediction, depending on assumption made for the radiation history and the operating temperature of the detectors. If one requires that the detector be efficient for a depletion voltage after inversion of 300V and that it can function with reduced performance with twice the depletion voltage at the same bias voltage, one is led to using single-sided detectors with n-side read-out. The reasoning is given in detail in the following.

4.1 Charge Collection [Refs. U1-U4, R7]

The signal collection is well understood before irradiation. The signal charge is proportional to the width of the depleted region. Aside from surface effects, the width of the depleted region x depends on the ratio of the bias voltage to the depletion voltage

$$x = d\sqrt{\frac{V_{bias}}{V_{dep}}} \quad \text{for } V_{bias} < V_{dep},$$

$$x = d \quad \text{for } V_{bias} \geq V_{dep}$$

where d is the detector thickness. Biased above depletion, the only difference between the p- and n-sides is the longer collection time of the holes, which can cause a ballistic deficit at fast shaping times and small over voltage [E2]. Biased below depletion, the signal collection depends on whether the collection happens on the junction side or on the ohmic side. On the junction side, the signal charge is collected on one or two strips. On the ohmic side, the strips are shorted out and the charge is collected on many strips. Consequently, the efficiency for detecting tracks on

the ohmic side is much reduced if operated below depletion (Fig. 5a). Before irradiation, the depletion voltage is between 50V and 100V and the detectors can easily be biased above depletion. This is the reason why in the past, in low radiation application, p-on-n or double-sided detectors were used almost exclusively and why they constitute the basis of our operating experience.

The signal collection after irradiation is well measured: first there is signal loss due to charge trapping. Measurements have shown that the loss of charge due to trapping is of the order 15% at the highest LHC fluences considered [R6]. At a fluence of about 10^{13}p/cm^2 (~1/10 of the total life time for the ATLAS SCT) the bulk inverts from n-type to p-type. The junction moves to the n-side. As before irradiation, the charge collection on the junction side is efficient even below depletion (Fig. 5b). The p-side becomes the ohmic side, and below depletion, the generated charge is collected on several strips, as before irradiation, although they are not shorted out. Hence, for irradiated detectors, operation close to depletion is required for the p-side, while operation below depletion is possible for the n-side. The n-side exhibits good efficiency >95% when biased at 50% of depletion voltage, while the p-side shows good efficiency only when biased above depletion voltage (Fig. 5b).

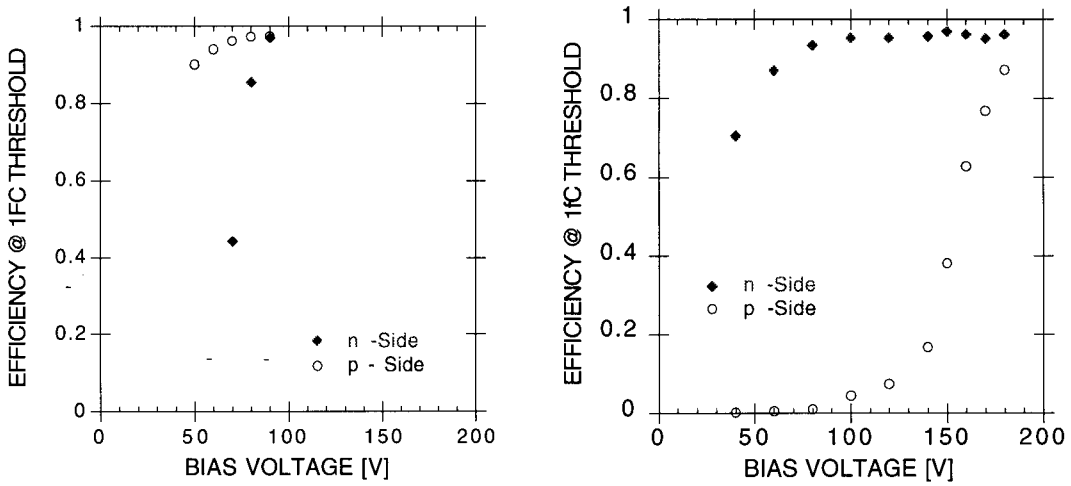

Fig. 5 Efficiency at threshold of 1 fC of a double-sided detector with 50 µm pitch
a) non-irradiated with a depletion voltage of 77V, b) irradiated with depletion voltage 190V (Ref. U2).

The charge sharing in irradiated double-sided detectors has been measured below depletion [R7]. The ratio of (3 hit clusters)/(2 hit clusters) R32 is a measure of the cluster size. The cluster size on inverted double-sided detectors below depletion is shown in Fig. 6. The R32 on the n-side is decreasing with decreasing bias because the collected charge is decreasing and

the minimal pulse height considered is fixed at 2σ. On the p-side, R32 is increasing below depletion. This indicates that the charge collected on the p-side is spread over several strips below depletion, and precise localization of the track is not possible.

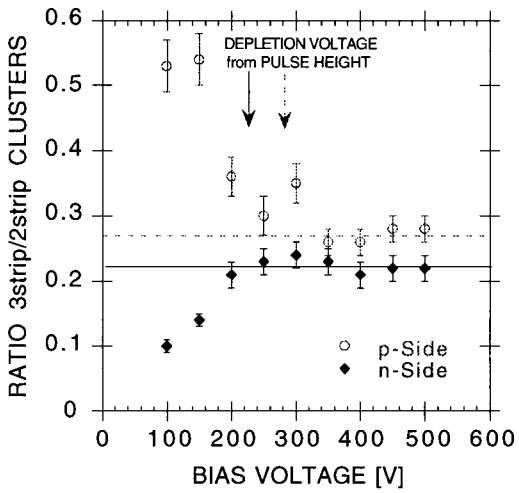

Fig. 6 Ratio of 3 hit clusters to two hit clusters R32 for an irradiated double-sided detector (Ref. R7).

Because read-out on the junction side allows the detector to be operated under-depleted, n-on-n single-sided detectors function, after inversion, almost as well as before radiation up to much larger fluences than originally anticipated. If the system is designed for a maximum bias voltage of 250V-which by now has been routinely used in several beam tests-it will work with 95% efficiency even if the depletion voltage turns out to be 500V, due to increased luminosity, radiation accidents or possible warm-up. If p-side detectors are used in high radiation conditions, the entire SCT system, power supplies, data transmission, bypassing, cables etc., has to be designed to the largest depletion voltage foreseeable, because changes in the conditions which increase the maximum depletion voltage beyond the anticipated goal strongly reduce the p-side performance.

The fact that n-on-n detectors can be operated under-depleted can be exploited in pixel detectors, which could be operated at a reasonably low bias even in the case of a large depletion voltage [V1-V3]. We have irradiated a single-sided n-on-n detector to 10^{15} p/cm^2, where the depletion voltage is about 2000V, and extracted at 180V bias the pulse height, amounting to 20% of the pre-rad value (Fig. 7). With the very low pixel capacitance, this small a signal charge gives sufficient signal-to-noise for efficient track detection very close to the interaction point.

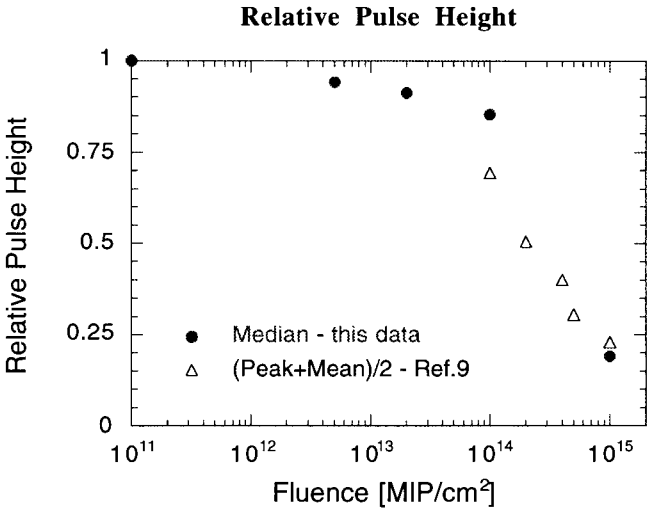

Fig. 7 Relative pulse height of n n-on-n detector at 180 V bias (from Ref. V2. Ref. 9 refers to Ref. V3).

4.2 Noise [Refs. N1, N2]

There is no long-term experience operating heavily irradiated detectors with short shaping times. In laboratory and beam tests, the n-side on irradiated detectors have shown somewhat reduced capacitance and noise with fast shaping front-end electronics (FEE) due to the fact that they have become the junction side (Fig. 8). Laboratory measurements on p-side detectors have shown increased inter strip capacitance and increased noise after radiation [C4].

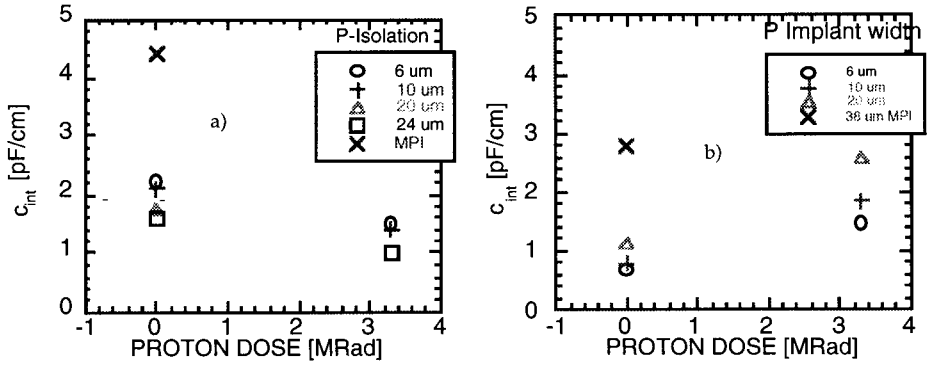

Fig. 8 Inter strip capacitance measurements before and after proton irradiation:
a) n-side, b) p-side (Ref. C4).

Because the amplifier noise depends on the parasitic detector capacitance, the noise performance is directly related to the inter-strip capacitance. The noise occupancy (Fig. 9), *i.e.*, the number of hits per channel per clock-cycle of 25 ns, of irradiated and non-irradiated detectors

agree with the observation that the n-side is the preferred side after heavy irradiation: the occupancy on the n-side is decreased, on the p-side increased.

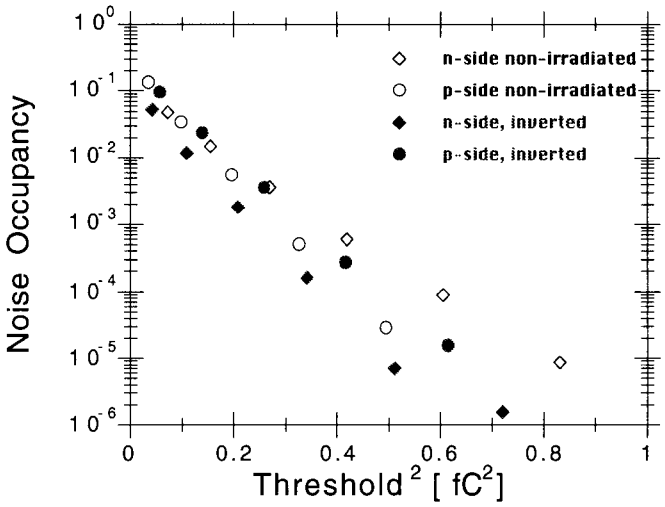

Fig. 9 Noise occupancy as a function of the comparator threshold of non-irradiated and irradiated 6 cm long double-sided detectors (Ref. N2).

4.3 Summary of n- side vs. p-side

The n-on-n detectors have shown good performance with a "head room" of about 20%, when operated close to depletion. This means that the efficiency is almost unchanged when the threshold is increased from 1.0 fC to 1.2 fC. This is due to the high signal-to-noise ratio of about S/N = 15. After radiation damage, the head room can be used to operate under-depleted, if warranted by unforeseen run conditions. At half depletion voltage, the resolution is unchanged and the efficiency is still 95%. The head room is not present for p-side detectors when operated under-depleted: immediately below depletion, the ohmic side looses efficiency and/or resolution. In general, the required bias on the junction side is about half the one needed on the ohmic side.

4.4 Single-sided vs. double-sided detectors

Given that the n-sides have superior radiation resistance, the use of the p-side is less advantageous. Indeed, the ATLAS SCT will build sandwiches of two single-sided n-on-n detectors, glued back-to-back, to make a double-sided module. This way the read-out strips and the front-end electronics are at ground, with many advantages for the operation and safety of the detectors at high depletion voltages and the FEE.

4.5 Effect of Glues [Ref. Z2]

We have built and operated in beam tests modules made out of single-sided n-on-n detectors and have seen no adverse effect due to the gluing onto the detector surfaces, either the

ohmic or the junction side, respectively. We have glued hybrids on the front face of silicon modules, either p- or n-side, and operated successfully without increase of noise. One concern is mechanical stresses due to temperature cycling, but for two years, we have operated the modules cold, and they survived a great deal of temperature cycling during beam and bench tests. We have investigated the noise immunity of the sandwich system and find that a noise voltage of 100 mV on the cooling pipe will contribute less than 1/2 noise sigma [H4].

4.6 Cooling [Refs. H1-H3]

The effects of radiation damage can be mitigated by cooling. Both the leakage current and the reverse annealing in the depletion voltage are reduced at low temperatures. But even at operating temperatures of -10°C, the heat conduction in 300 μm thick wafers are not good enough to prevent local heating of the detectors. This can lead to thermal run-away, in case the radiation damage is worse than anticipated or the cooling system not adequate [H1, H2]. The thermal properties of the silicon modules can be vastly improved with the introduction of a "heat spreader", a thin layer of highly thermally conductive material sandwiched between two single-sided detectors which effectively brings the cooling pipe close to the self-heated detector. The ATLAS SCT will use a plane of pyrolytic graphite (PG) which has a heat conductivity close to CVD diamond. Figure 10 shows the principle of the silicon-PG-silicon sandwich, which has been used to investigate the thermal properties of the PG material [H3]. The cooling pipe attaches to one side of the heat spreader only.

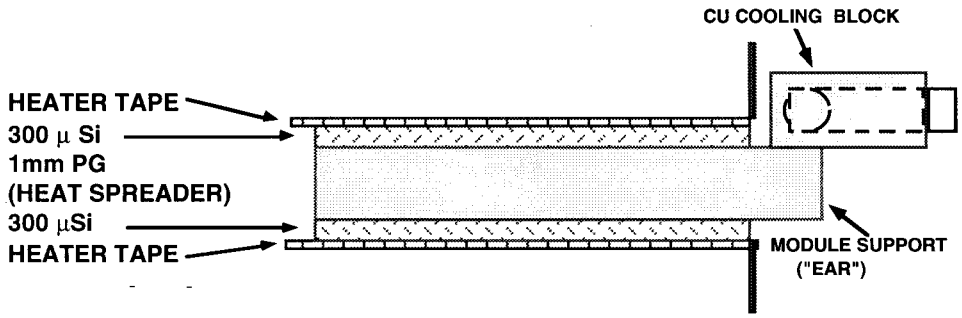

Fig. 10 Cross section through the ATLAS module: a Silicon-PG-Silicon sandwich.

A simulation of the temperature distribution across a 12 cm x 6 cm module was performed as a function of the internal heating for both a single wafer module and the Si-PG sandwich. It shows that the Si-PG sandwich allows a factor of at least 3 in the acceptable internal heating before thermal run-away (Fig. 11).

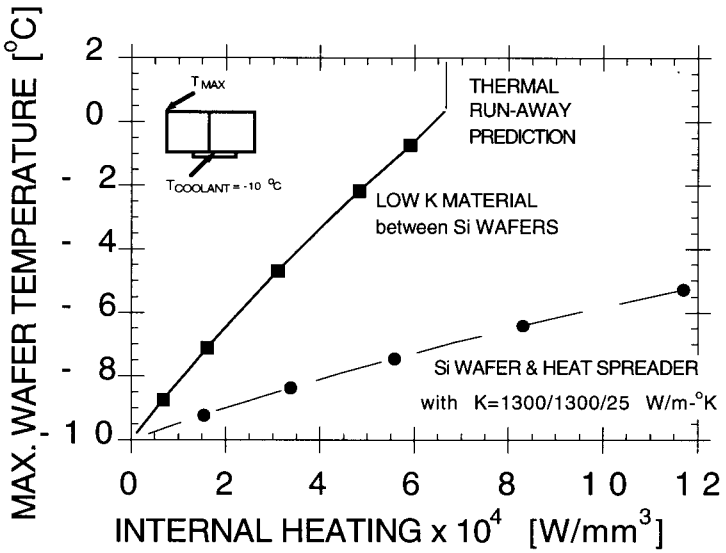

Fig. 11 Simulation of the maximal wafer temperature on a silicon detector with one edge cooled to -10°C as a function of the internal heating. Both a double-sided detector ("Low K") and a Silicon-PG sandwich ("Heat Spreader") are shown (Ref. H3).

The temperature profile across a 6 cm x 12 cm module, both simulated and measured, for a heat input of 3 mW per electronics channel and internal heating of about $2.5*10^{-4}$ W/mm^3 is shown in Fig. 12. The maximum temperature difference on the wafers is of the order of one degree.

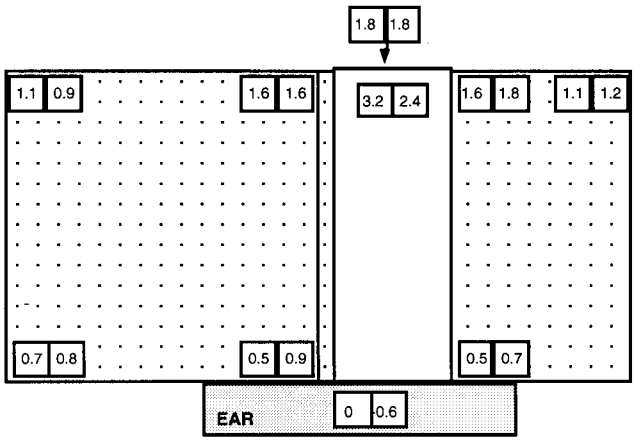

Fig. 12 Measured and simulated temperature profile across a silicon-PG sandwich. Heating occurs both internally and through the FEE (Ref. H3).

5. BEAM TEST RESULTS [Refs. B1-B7]

A series of beam tests have been performed with 12 cm long modules of single-sided n-on-n silicon detectors and fast FEE [B5- B7]. Identical modules were tested in 1996 in the H8 test beam at CERN [B7], with one of them irradiated such that the depletion voltage was 290V,

as determined with C-V measurements (Fig. 13). The detectors were operated cold (at about -10°C) and rotated relative to the beam in a magnetic field of 1.56T to investigate the performance for tracks with crossing angles as expected in the ATLAS detector [T3].

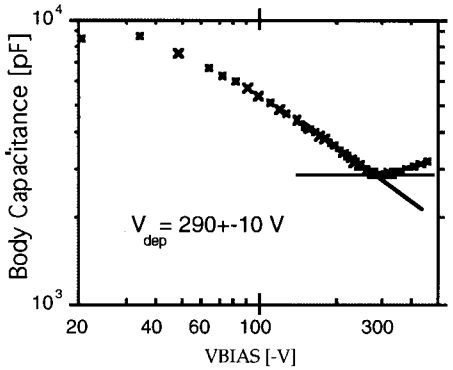

Fig. 13 Determination of the depletion voltage of ATT7, the irradiated 12 cm module, with a C-V curve.

The performance is quantified in efficiency and noise occupancy. The noise occupancy is far below 10^{-3} for 1fC threshold. The median pulse height on a single strip and the efficiency at 1fC threshold of the irradiated detector ATT7 both show the slow decrease below the depletion voltage discussed in Sec. 4 (Fig 14). The efficiency of n-on-n detectors is high in the non-irradiated detector when over-depleted (at bias >100V), and in the irradiated detector at 150V which is one half of the depletion voltage.

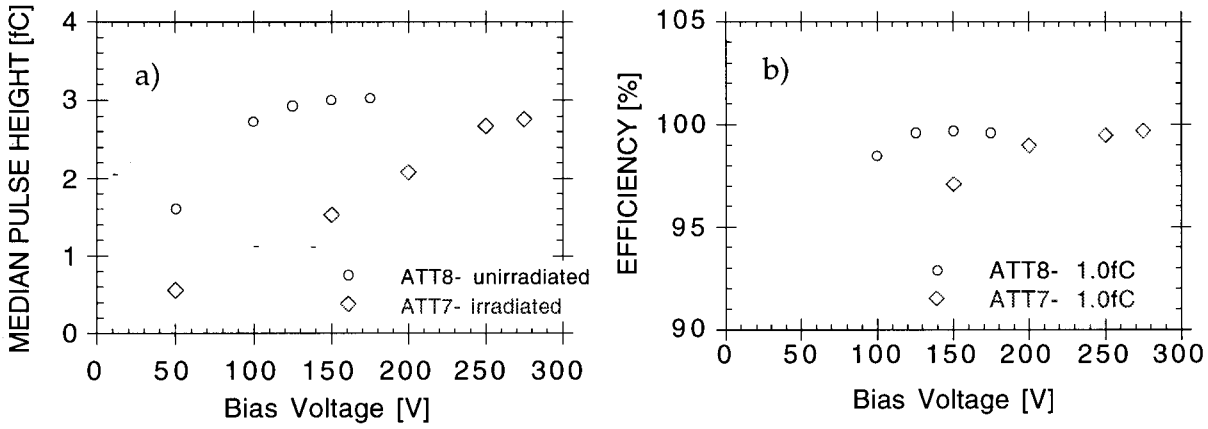

Fig. 14 Bias voltage dependence of 12 cm n-on-n modules for unirradiated ATT8 and irradiated ATT7 detectors (depletion voltage 290V): a) median pulse height, b) efficiency at 1fC threshold (Ref. B7).

For the rotated detectors in a magnetic field, the efficiency is independent of rotation angle for the required range of ±15° relative to the anticipated tilt angle of about +10° (Fig 15a). When biased at half the depletion voltage, the efficiency of the irradiated detector ATT7 is still 95% at 1.0 fC threshold. It turns out that biased at the full depletion voltage, the efficiency is

high even at a threshold of 1.2 fC, is 20% higher than the threshold required for noise suppression [B7]. The position resolution of the irradiated detector identical to the non-irradiated one (Fig. 15b). It is constant as a function of rotation angle and close to the expected value of pitch/$\sqrt{12}$. At 1/2 the depletion voltage, the position resolution for ATT7 is the same as at full depletion.

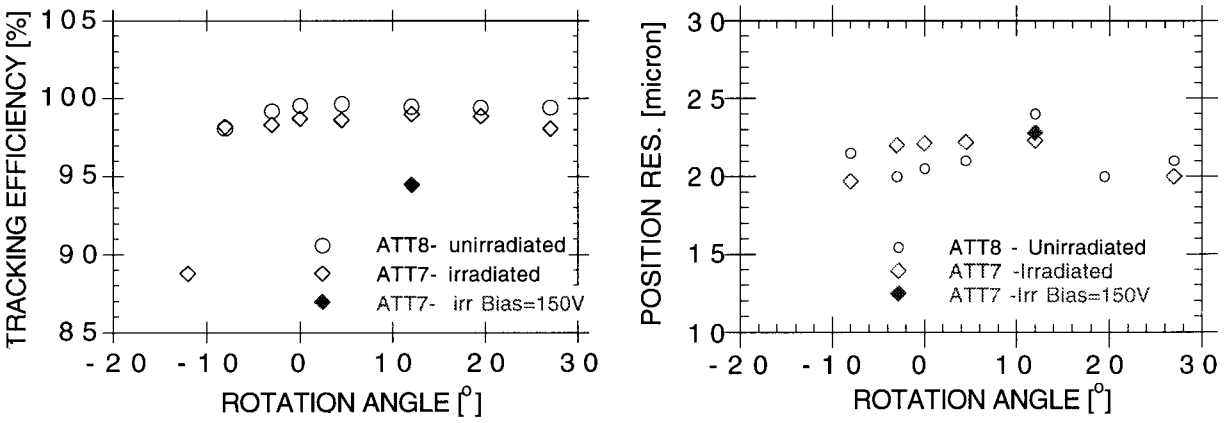

Fig. 15 Rotation angle dependence in a 1.56T magnetic field with bias at 250V (ATT7) and 125V (ATT8): a) efficiency at 1fC threshold, and b) position resolution (Ref. B7).

As mentioned in Sec. 3, short-term radiation effects can effectively be understood only in realistic operating conditions. For part of the runs, the intensity of the test beam was increased to the instantaneous flux expected for operation at the LHC. As mentioned before, the detectors were cooled to -10°C throughout the beam test. No change in efficiency was observed neither for the unirradiated nor the inverted module (Fig. 16).

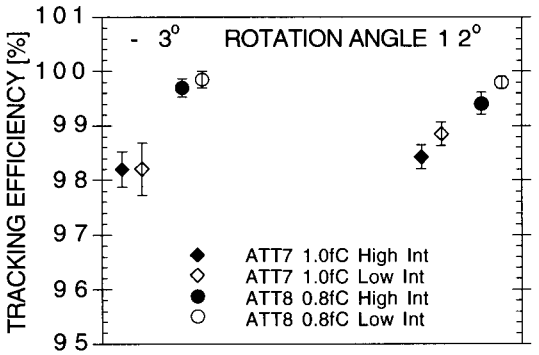

Fig. 16 Efficiency for both irradiated (ATT7) and unirradiated (ATT8) module during high and low intensity running for two rotation angles.

6. CONCLUSIONS

For the ATLAS silicon tracker, a sandwich of single-sided n-on-n detectors was chosen as the base line, because their superior performance after heavy radiation damage has been proven over the last years. They exhibit good signal-to-noise ratio, even when operated under-depleted after radiation induced inversion. The alternative, double-sided detectors, has been shown to require full depletion on the p-side. In several beam tests, fully instrumented modules have been operated, some of them irradiated with realistic LHC fluences. The results confirm that the single-sided n-on-n detector affords the performance headroom required for the high radiation environment of ATLAS and the uncertainty in predicting the operating conditions. With n-on-n detectors, the ATLAS SCT will be able to survive either higher radiation levels than anticipated or unexpected scenario's of warming up of the detectors, and will be able to profit from a more optimistic luminosity scenario.

7. ACKNOWLEDGMENTS

The development of silicon detectors for high luminosity application has been a world-wide effort. I would like to acknowledge the collaboration with many people. I would like to thank the staff of the SCIPP Microelectronics laboratory for their excellent work. This work has been supported by the US Department of Energy.

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3D-A new architecture for solid-state radiation detectors

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Abstract

A proposed new architecture for solid-state radiation detectors using a three-dimensional array of electrodes that penetrate into the detector bulk is described. Proposed fabrication steps are listed. Collection distances and calculated collection times are about one order of magnitude less than those of planar technology strip and pixel detectors with electrodes confined to the detector surface, and depletion voltages are about two orders of magnitude lower. Maximum substrate thickness, often an important consideration for x-ray and gamma-ray detection, is constrained by the electrode length rather than by material purity or depletion-depth limitations due to voltage breakdown. Maximum drift distance should no longer be a significant limitation for GaAs detectors fabricated with this technology, and collection times could be much less than one ns. The ability of silicon detectors to operate in the presence of the severe bulk radiation damage expected at high-intensity colliders should also be greatly increased.

I. Introduction

Since the development of silicon detectors with surface barrier electrodes in the 1960s and ion-implanted ones in the 1980s [1], planar structures on the material surfaces have been used. Voltages that are typically many tens of volts are needed to deplete the detector bulk which is normally hundreds of microns thick. Typical drift paths for ionization charges are at least comparable to that thickness. The structure proposed here uses electrodes with typical pitches of a few tens of microns and which penetrate from one surface through most or all of the bulk (see Figure 1). The resulting short charge collection distances provide fast collection and low depletion voltages. Short collection times will be useful for a proposed quantum mammography system [2] which records individual x-ray hit locations, and the combination will be particularly useful at high-luminosity colliders where detectors face severe problems both from high event rates and from increased depletion voltages due to bulk radiation damage. Use of this technology should

eliminate bulk type-reversals, any need for high depletion voltages, and the need to refrigerate the detector continuously, even during maintenance.

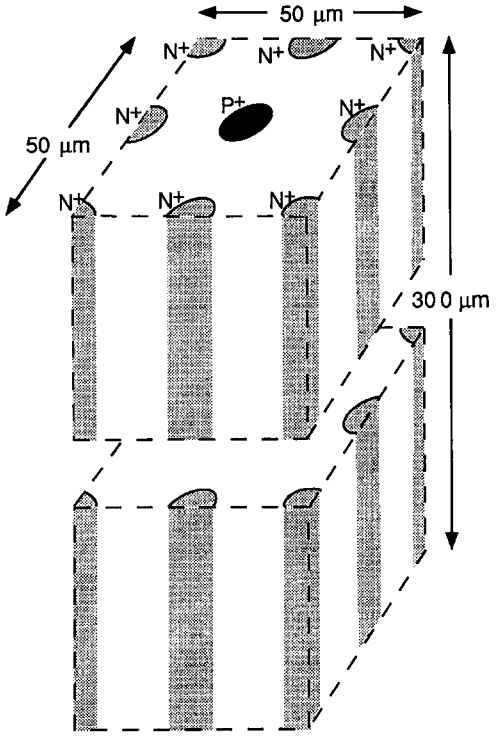


Figure 1 - Three-dimensional view of a typical cell.

The key facts that make this technology possible are:

1. Deep, reactive-ion etching now permits holes to be made with depth-to-width ratios of over 15:1 and with silicon-to-oxide-mask etch rate selectivity of greater than 300:1 or silicon-to-photoresist selectivity of greater than 50:1 [3]. Absolute etch rates (about 5 microns/min) are also high.
2. The holes can then be filled with silicon made by the surface reaction of silane, which will bounce off the silicon surfaces thousands of times before reacting, thus depositing silicon as readily near the bottom as the top [4].
3. Similar behavior by dopant gases such as diborane and phosphine, when added to the silane, allows the fabrication of n^+ and p^+ electrodes. All of the three gases will form conformal coatings without clogging the top of the hole before the bottom can be covered [4,5].
4. The silicon layers deposited simultaneously on the wafer surfaces will have a thickness somewhat greater than the hole radius, and can be readily removed by etching.

The fabrication steps following electrode formation can be varied to produce monolithic pixel detectors [6], bump-bonded pixel detectors [7], and strip detectors with or without on-chip driving electronics associated with the bulk electrodes. Proposed devices of each type will be described,

with the most detail for the simplest ones, which we plan to fabricate first: diodes for DC and capacitance tests and for bump-bonded pixel detectors. Although we are concentrating here on a silicon device, it is possible that the GaAs ones could benefit even more, as large thicknesses could provide good x-ray and gamma-ray detection efficiencies but for their drift-length limitations. Here, it could be possible to provide electrode spacing that is less than those drift length limitations. The short maximum drift distances combined with the high electron mobility of GaAs will also produce an extremely fast detector.

II. A basic detector for initial tests and for bump-bonded pixels

Many different electrode arrangements could be used, depending on the requirements of the test devices and of any experiment using pixel detectors. Figure 1 shows a view of one possible basic PIN diode cell. Some of the architectural principles used in previously fabricated monolithic pixel detectors [6] are also used here:

1. If it is necessary to minimize the maximum electric fields, electrodes forming the diode junctions will have greater total surface area than those forming ohmic ones.
2. N^+ electrodes have phosphorus doping and serve as getters. Their area is kept as large as possible, consistent with other design requirements.
3. Use of p^{--} substrate prevents type change from bulk radiation damage, which while not necessarily lethal in all designs, does mess up principle 1. There is also data, though not at high fluence, indicating that p^{--} silicon is less subject to bulk damage than n^{--} [8].

These three imply that the p electrode should transmit the signal from the entire pixel, while the multiple n electrodes form the diode junctions. Signals could be taken from them also, further subdividing the pixel, and also providing faster signal collection speed, but monolithic technology is likely to be needed for the smallest readout pitches. With fast electronics, improved position and time information could also be provided by comparing the various p and n signal times and pulse heights.

In addition,

4. to reduce the number of bumps required, and to provide redundancy for those that are used, multiple n electrodes are tied together with metal or diffusion conductors, as are the electrodes in many test structures. If the desired amount of electronics in the pixel causes the pixel area to exceed the area of the underlying bulk cell, conductors can also be used to join p electrodes from several cells to the pixel electronics, but with the price of increased capacitance ΣC_i, a reduced signal, $\Sigma q/C_i$, and a reduced signal-to-noise ratio. In this case, one simple front-end circuit per cell with an input signal q/C_i, may be a better choice. The random noise of the sum

then increases, and the signal-to-noise ratio decreases, at most only as the square root of the number of cells. (For example, if one source-follower from each cell is used to drive a common pixel bus, one with a signal will tend to cut off those without, and only the noise on that channel will be present.)

When on-wafer metal lines are used, the electrode tops will be in contact with, and surrounded by, an implanted ring of like-type silicon to make the contacts, as the silicon surface directly above the electrodes may not be fully planar.

5. The silicon surfaces can be inverted by charges in the surface field oxide layers, which could make a continuous n conductor from the n electrodes to the immediate vicinity of the p electrodes. This small gap, which can result in increased electrode capacity and fields, should however be significantly enlarged by the applied depletion voltage. Increased oxide charge due to radiation damage might again reduce the gap. To prevent this, p^+ guard rings around the p electrode or a blanket p implant may be used. Implanted rings may also be used in test devices to monitor surface leakage currents.

III. Fabrication steps for test structures and bump-bonded diodes

One possible sequence of fabrication steps is given below. Routine wafer cleaning and process checking steps are not listed. In addition, most major steps have many substeps which are also not given. For instance, masking steps involve spinning of photoresist, a low temperature bake, exposure in a mask aligner, photoresist development, a high temperature bake, the masked process (such as ion implantation or etching), and photoresist stripping. And even a simple step such as the spinning of the photoresist will have substeps.

1. mask 1: alignment mask and etch
2. mask 2: n electrode mask and wafer etch-through
3. n^+ silicon deposition and hole fill (for example, using a silane/phosphine mixture)
4. etch back deposited silicon on both wafer surfaces
5. mask 3: p electrode mask and wafer etch-through
6. p^+ silicon deposition and hole fill (for example, using a silane/diborane mixture)
7. etch back deposited silicon on both wafer surfaces
8. thermal oxidation (0.6 micron oxide thickness)
9. etch oxide, backside
10. backside blanket p^+ implant (to prevent oxide charges from inverting the adjacent silicon; this step might not be needed or might be changed to a masked one with p^+ rings to increase the n^+/p^+ separation)

11. thermal oxidation (0.6 micron oxide thickness). (If step 10 isn't needed, steps 9 and 11 will also be omitted.)
12. mask 4: front side n^+ mask and implant (to provide a planar ohmic contact to the n^+ electrodes--the silicon fill at the electrode surfaces will not be necessarily flat)
13. mask 5: front side p^+ mask and implant (to provide planar ohmic contact to the p^+ electrodes and guard rings around them if the rings are used to monitor currents)
14. anneal implants
15. low temperature oxide (LTO) deposition
16. mask 6: contact mask and etch
17. aluminum deposition
18. mask 7: metal mask and etch

IV. Epi vs. poly

Two major questions must be answered by experiment: the size of the smallest holes that can be etched through, and whether single-crystal (epi) or poly-crystalline silicon (poly) is used to fill the holes. Holes 15 microns in diameter and 200 microns deep have been made in which the top-to-bottom taper is less than 0.1 microns, and it is believed that 10 micron holes can be readily etched [9]. Epi is generally more difficult to make than poly, and can only be deposited on single crystal silicon, which however, should form the hole surfaces, if they are properly cleaned prior to deposition. It is not clear if the nature of the etched surfaces will present extra difficulties to epi deposition.

Use of epi will provide one major advantage, particularly if it can be combined with a gradually increasing dopant level during deposition. Following the anneal, there should be a radial dopant gradient that will provide a radial built-in electric field which will transport ionization charges in the same direction as the applied field, providing rapid collection of charge from the entire volume of the detector, including the electrodes.

Following the deposition, the silicon is heated so the dopant atoms move to lattice sites and become electrically active. They also diffuse out from the n^+ electrodes into the p^{--} bulk and form p-n junctions in high-quality silicon. However, in poly, diffusion of dopant atoms, following grain boundaries, is far faster than in single crystal silicon. Because of this, a nearly uniform doping density is established in the poly, reducing the size of the built-in field in the electrodes. Diffusion of ionization charge from the track to the start of the applied field several microns away, possibly with a small boost from Coulomb repulsion from the rest of the track, becomes the only method of collection. This is discussed in more detail in section IX. Recombination within the electrodes should not be a problem. Measurements on 20 ohm-cm epi in a CCD vertex detector show diffusion lengths of about 200 microns [10].

V. Calculated performance

Voltage distributions have been calculated both by MEDICI [11] and by the sequential-over-relaxation method [12] (we have coded the latter so its speed and efficiency permit its use in three-dimensional calculations as well as the two-dimensional ones needed for this section). For the latter, symmetric boundary conditions, V(i+1,j,k) = V(i-1,j,k), are used for the (cubic) cells on either side of a boundary at the plane i = constant, where the V's are the voltages at the center of the cells. At silicon-insulator boundaries, the next voltage for any cube is found from the average of the four adjoining ones on the boundary and the adjoining one further into the silicon (plus the usual term from fixed charges). This is a reflection of the fact that, in equilibrium, there is no net charge transport into the cube, and so the sum of the current across the five faces and thus the five voltage differences sum to zero (in this approximation, surface currents are neglected). The effects of induced charges are calculated using Ramo's theorem [13].

At present, of the two, only MEDICI can calculate fields and current flow in the presence of surfaces and undepleted silicon. When both methods could be used for the same problem, results agreed within errors. Coulomb forces within the ionization cloud are included but are generally unimportant, causing only about a 10% decrease in collection times, even when a track was at a zero-drift field location such as the null point between two n^+ - electrodes (the Coulomb forces were approximated by subdividing the 24,000 electron-hole pairs from a typical minimum-ionization track into packets of 40 charges each, which diffused and drifted as a group. Results did not change significantly when the packet size was changed).

Depletion voltages for the sample diode shown in Figure 1 are 1.6, 1.8, 3.8, and 8.8 V for dopant concentrations of 10^{12}, $3x10^{12}$, 10^{13}, and $3x10^{13}$/cc, including a contribution from the built-in voltage at the electrodes that ranges from about 0.7 to 0.8 V. The values are not proportional to the concentrations because in the course of fully depleting the lightly doped silicon, part of the heavily doped region around the electrodes is also depleted. Our first and second generation pixel detectors have a doping concentration of $1.2x10^{12}$/cc. Bulk damage in 10 years for pixel detectors at the LHC would not be expected to increase this doping much beyond 10^{13}/cc.

Figure 2a shows equipotentials for one quarter of the unit cell of the same device with 10^{12} dopant atoms/cc when 5V is applied between the two metal electrodes. The cylindrical electrode doping profile assumed here and throughout this paper is 10^{18} exp-$(r/r_0)^2$, where r_0 is chosen to bring the concentration to 10^{12}/cc at r = 5 microns. This profile will produce n^+ electrodes with a resistance of about 3 ohms/micron and p^+ ones of about 2.5 times that value. The boundaries of the depleted region are indicated by short dashes. Lines with longer dashes, mark p-n junctions. Figures 2b, 2c, and 2d show similar equipotentials for 5V-10^{13}/cc, 10V-10^{12}/cc, and 10V-10^{13}/cc. Figure 3 shows drift lines corresponding to the equipotentials of Figure 2a.

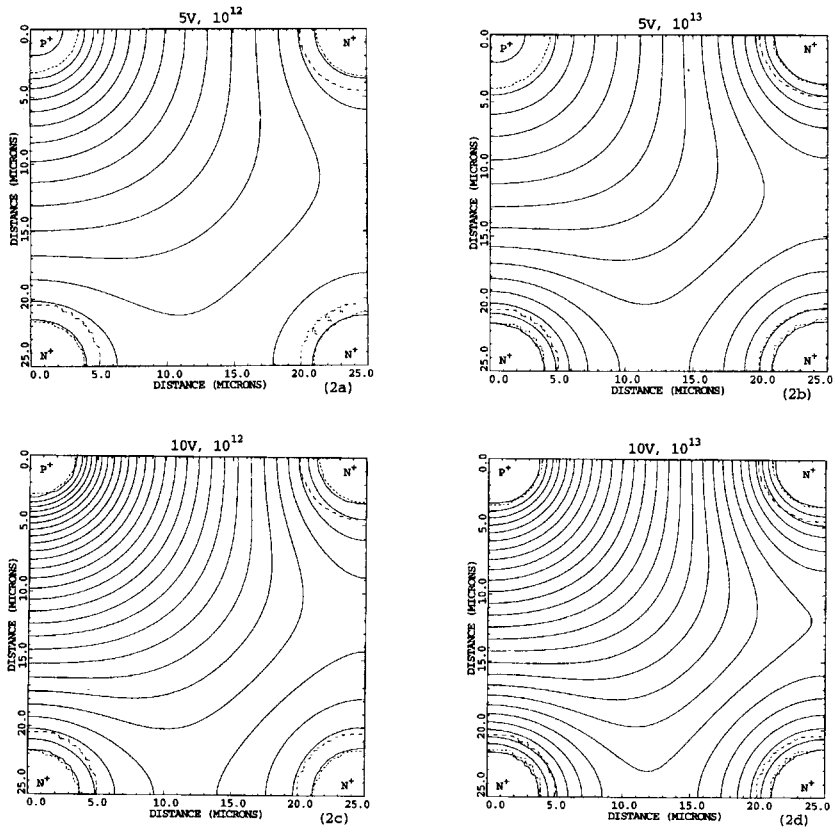


Figure 2 -(a) Equipotentials for one quarter of the unit cell of Fig. 1 with 10^{12} dopant atoms/cc when 5V is applied between the two electrodes. The boundaries of the depleted region are indicated by short dashes. Lines with longer dashes, mark n-p junctions; (b) equipotentials for 10^{13}/cc, 5V; (c) for 10^{12}/cc, 10V; (d) for 10^{13}/cc, 10V. Effects of surface charges are not included. The lack of cylindrical symmetry in the fields and depletion depths into the electrodes, especially of the n^+ ones adjacent to the p^+ electrode, can be seen as can the decrease in low-field volume for the heavier (10^{13}/cc) substrate doping.

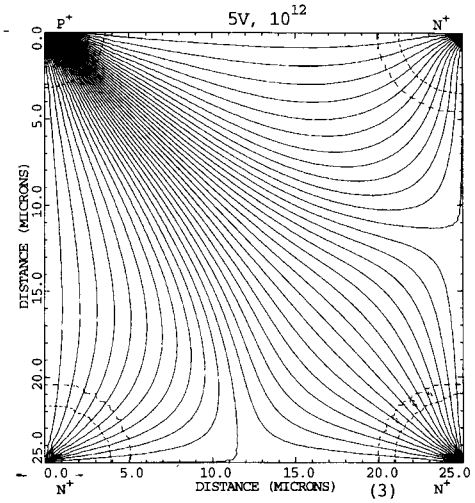


Figure 3 - Drift lines for Figure 2a: 10^{12} dopant atoms/cc and 5V.

Figures 4a, b, and c show the magnitude of the electric field of Figure 2a along three electrode-to-electrode lines for 10^{12} dopant atoms/cc. For 5V (the next-to-bottom line), more than enough for full depletion, the peak fields are more than an order of magnitude below avalanche fields which are over 100,000 V/cm. Figure 5 shows peak fields actually decrease when the substrate doping increases by a factor of 10.

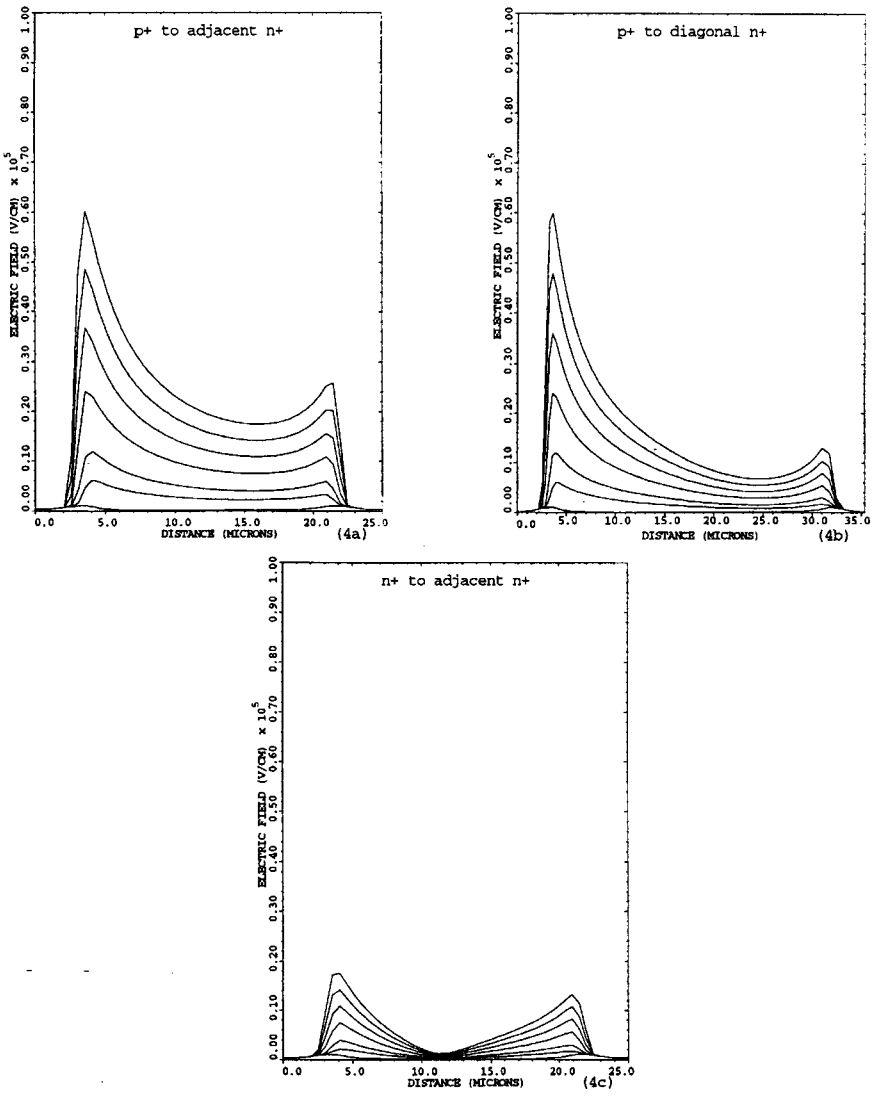


Figure 4 - Electric field magnitudes for the quarter cell of Fig. 2a, substrate doping of 10^{12}/cc, and applied voltages of 50, 40, 30, 20, 10, 5, and 0 V (top to bottom lines) along lines from (a) the p^+ to the adjacent n^+ electrode, (b) the p^+ to the diagonally opposite n^+ electrode, and (c) the n^+ to the adjacent n^+ electrode.

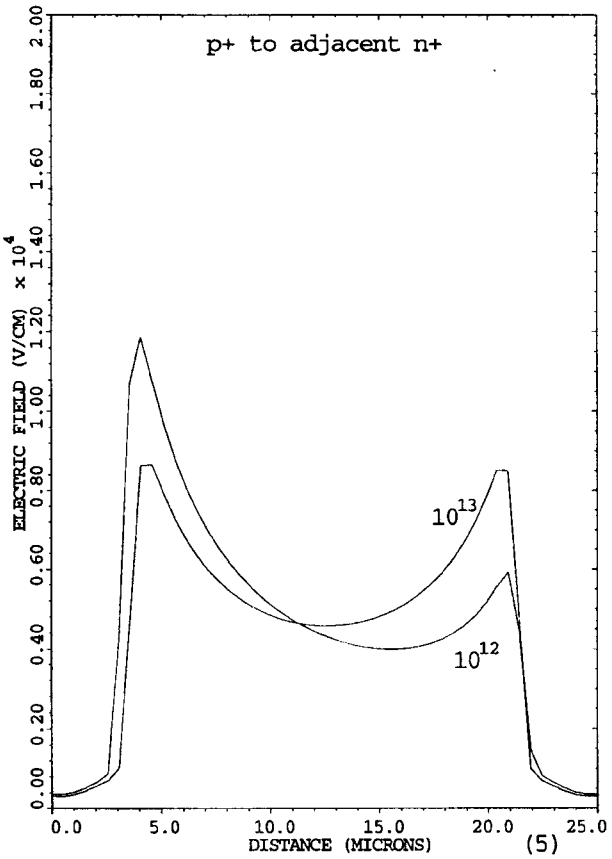


Figure 5 - Comparison of electric field magnitudes for the quarter cell of Fig. 2, 10 V applied voltage, along the line from the p^+ to the adjacent n^+ electrode for substrate doping of 10^{12}/cc and 10^{13}/cc. With higher substrate dopant levels, as can occur with radiation damage, the peak fields, located where the depletion volume meets the electrodes, actually decrease due to the increase in voltage dropped across the lightly doped (compared to the electrodes) substrate. The small, but non-zero values of the electric field at the ends of the plot (corresponding to the electrode centers) are due to approximations in the finite element calculations.

Figure 6 shows lines of equal drift time corresponding to the equipotentials of Figure 2c, 10 Volts and 10^{12}/cc. The drift time from the center of the cell is less than 1 ns, and the times from the other electrodes ranges from 1 to 4 ns. The time from the far cell borders is infinity as the collection field goes to zero there. To get realistic times for tracks in those regions, one must add diffusion, and for ionization created near or inside electrodes, the built-in fields. This is calculated by MEDICI. Figure 7 shows charge density contours for electrons and holes created by an ionization track of 24,000 pairs parallel to the electrodes and through the middle of the cell of Figure 2c, which should be typical of much of the area, and through the slowest, the null point on the border between two cells.

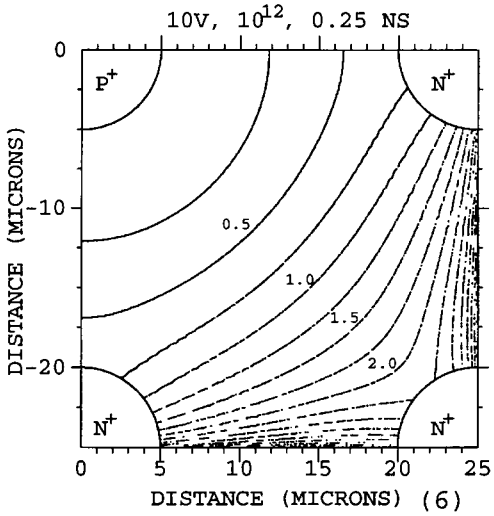


Figure 6 - Lines of equal drift time for potential distributions of Figure 2c (10^{12}/cc and 10V). Zero time is measured from the p^+ electrode (top left corner) at r = 5 microns and charges are traced backwards. Lines in the immediate vicinity of the zero-field points at the bottom center and right center are not reliable: diffusion plays a major role there. In addition, few of the tracks being traced backwards go there.

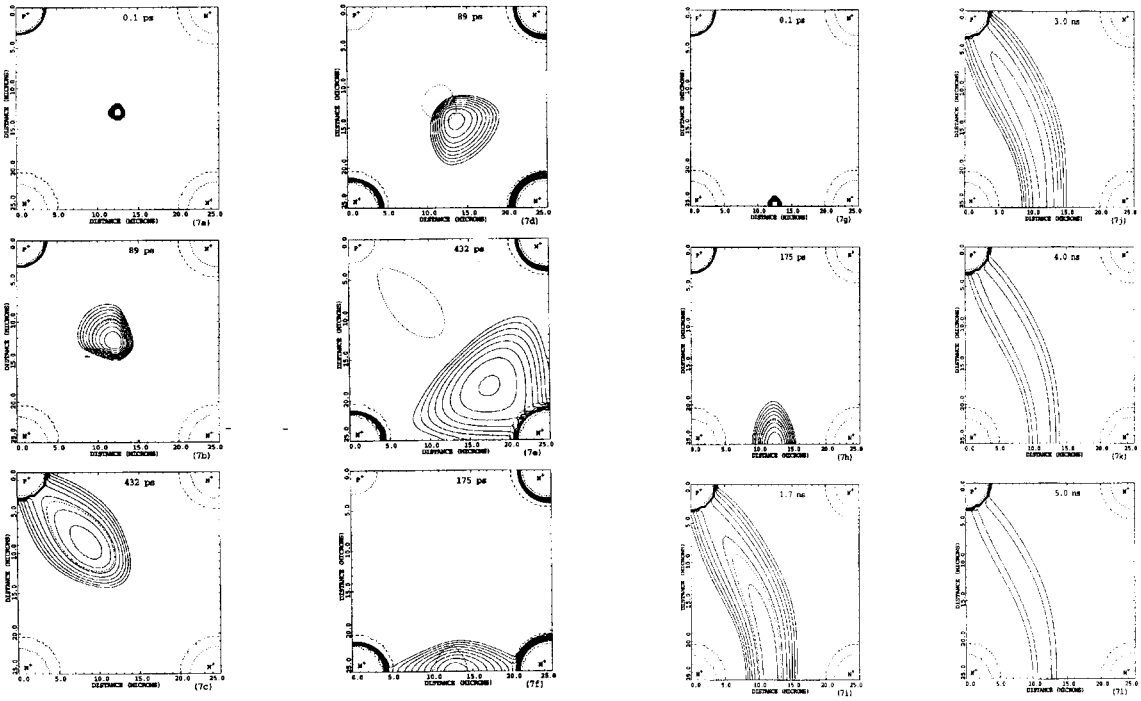
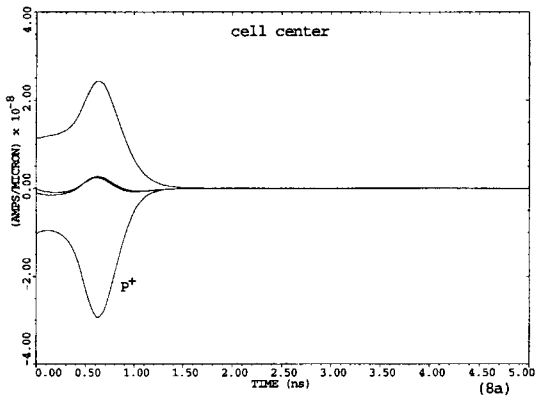


Figure 7 - Charge density contours (2 per decade) for electron-hole pairs. (a)-(c) holes starting from the cell center at 0.1, 89, and 432 ps, (d)-(e) electrons from the cell center at 89 and 432 ps, (f) electrons from the null point at 175 ps, and (g)-(l) holes from the null point at 0.1, 175 ps, 1.7, 3, 4, and 5 ns. The fields are those of Figure 2c, 10^{12}/cc, 10V.

Figure 8 shows the current pulses on the electrodes for those two starting points. The small difference in Figure 8a (the midpoint start) between the pulses on the two n^+ electrodes adjacent to the p^+ electrode are due to small but non-zero grid size effects. Effects of induced pulses from moving charges can be seen. The signal peaks at 0.5 ns and returns to the base line at 1.5 ns. Signals on strip detectors with 2D electrodes take about 25 ns to return to the baseline, neglecting amplifier delays [14]. (The return-to-baseline time can be important for pile-up considerations, especially since Landau fluctuation effects can be present until all the charge is collected.) The pulse on the p^+ electrode for the null point track (Figure 8b) peaks at 2.4 ns, and returns to the baseline at about 6 ns. These times, while significantly shorter than typical times for detectors with 2D planar electrodes, are, at the same time, for 3D devices with far lower maximum fields.



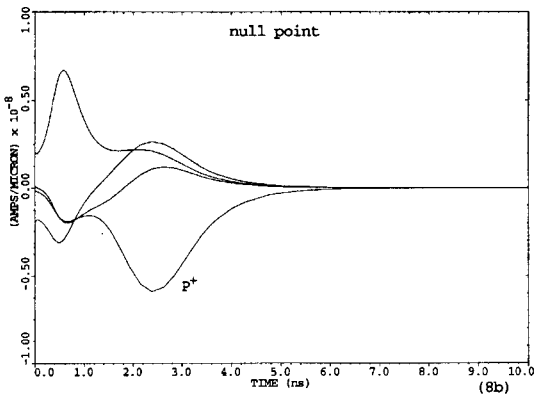


Figure 8 - Current pulses on the electrodes from a track parallel to the electrodes, (a) through the cell center, and (b) through the null point between two n^+ electrodes. The fields are those of Figure 2c, 10^{12}/cc, 10V. Effects of induced pulses from moving charges and diffusion are included, but not Landau fluctuations or Coulomb forces from the other charges along the track.

VI. Choice of electrode diameter and wafer thickness

Factors entering into the choice of hole diameter, in addition to fabrication capabilities, are the electrode capacitance, which is made smaller--improved--for small diameters, and the resistance and maximum electric fields which are increased, and so made worse.

The capacitance, C, of a 300 microns long electrode is about 0.1 pF. The RC products, related to the minimum times pulses take to leave the electrodes, are about 90 and 225 ps for the n^+ and p^+ electrodes. For some (but not all) structures, the value of R may also play a role in the noise performance, but that depends sensitively on the circuit to which the electrode is connected and is beyond the scope of this paper. Other possible fabrication sequences, for instance ones using selective deposition of tungsten in the central core of the holes to reduce the value of R, will not be needed for pixel detectors which are the first planned application of this technology, and will also not be covered here.

The initial signal developed on the electrodes, $q/C_{electrode}$, is, to first order, independent of the wafer thickness for penetrating ionizing particles as $C_{electrode}$ is approximately proportional to the thickness. While, in later stages of some electronic readout systems, thinner wafers may produce smaller signals, the degradation of the signal-to-noise ratio is not likely to be as rapid as it would be with planar, 2D electrode systems. If multiple Coulomb scattering considerations make thinner detectors desirable, it is likely, rather, that fabrication and handling difficulties will set the lower limit. Thinner wafers should actually permit smaller hole diameters to be fabricated, resulting in a decrease in $C_{electrode}$.

VII. Surface effects

All of the preceding calculations are for charge motion in the detector bulk. Close to the top and bottom, the effects of surface charges and structures must be considered. Results of calculations using a simple two-dimensional model in which the n^+ and p^+ electrodes are flat slabs separated by a 15 microns region of silicon with 10^{12} acceptors/cc and covered with an oxide layer having 10^{11} positive interface charges per sq. cm., are shown in Figure 9. A layer of induced electrons can be seen nearly reaching the p^+ electrode. When a bias is applied to the electrodes a gap appears. While this indicates it may not be necessary to use p^+ guard rings around the top of the p^+ electrode, they may be needed for radiation damaged oxides with larger surface charges.

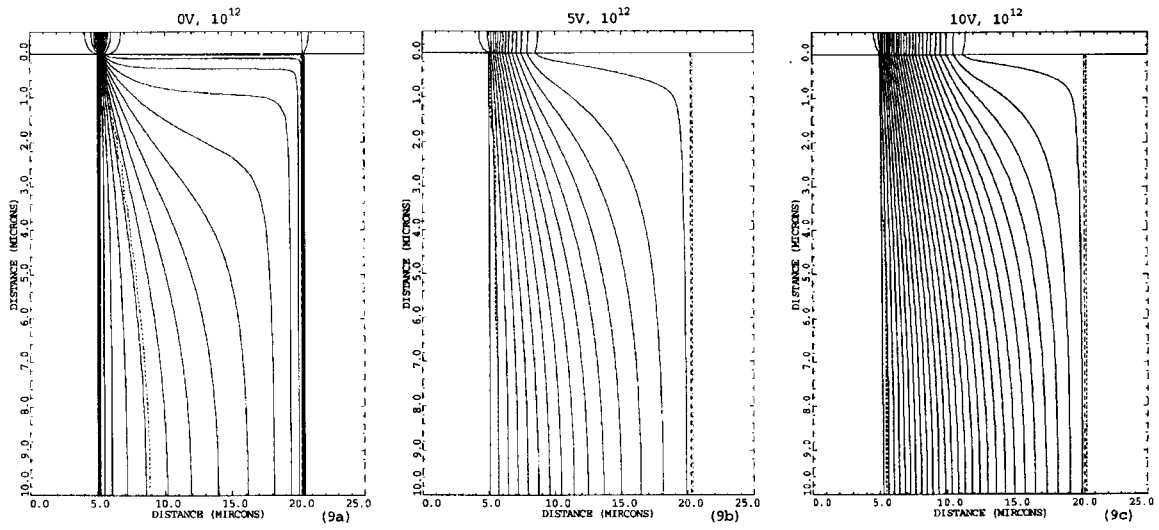


Figure 9 - Effects of an oxide interface charge of $10^{11}/cm^2$. In this two-dimensional example, the p^+ and n^+ electrodes are at 0-5 microns and 20-25 microns, doped throughout at $10^{18}/cc$, and the charges are along the top between them. The substrate doping $10^{12}/cc$. (a) Applied voltage = 0V. The effect of negative charge induced by the oxide charge can be seen with the closest equipotential almost parallel to the surface. The contact of the induced charge with the n^+ electrode on the right forces the equipotentials from the built-in field into a bundle next to the p^+ electrode. The capacitance between the two electrodes will be relatively high. (b) Similar equipotentials for 5V and, (c) 10V. An increasingly wider depletion zone at the surface can be seen. (d)-(e) Electron density contours for 0 and 10V. (f) Net carrier concentration 0.1 microns below the surface for 0, 5, 10, and 20V.

VIII. Other configurations

Figure 10 shows several additional configurations using 3D technology. Figures 10a and 10b show top views of alternating rows of n and p electrodes and 10c of one with hexagonal cells. Figure 10d shows a side view with an implanted n well on the top and an n^+ layer on the bottom. The n^+ layer would be made by driving phosphorus into single crystal silicon from a poly layer, providing gettering from both phosphorus and poly [15]. Figures 10e-10h show additional side views with various combinations of wells, n^+ layers, and oxide layers with and without p^+ rings. Figures 10d and 10e require back-side lithography. This should not be too difficult using steps already developed to protect the wafer bottom side during lithography [6], since the structures are relatively crude and the holes provide alignment marks. Figures 10g and 10h show electrodes that stop short of the bottom. This will permit a (conducting) n^+ layer to be implanted without the need for double-sided patterning. In general, cells with n^+ layers are the easiest to deplete, and those with p^+ rings the most difficult. On the other hand, the n^+ layer, forming an equipotential,

normally at the same voltage as the n electrodes, will make regions with relatively slow drift velocities, as would any top wells in monolithic devices. These should not affect the main part of a pulse from an ionizing particle, but could add somewhat to the tail.

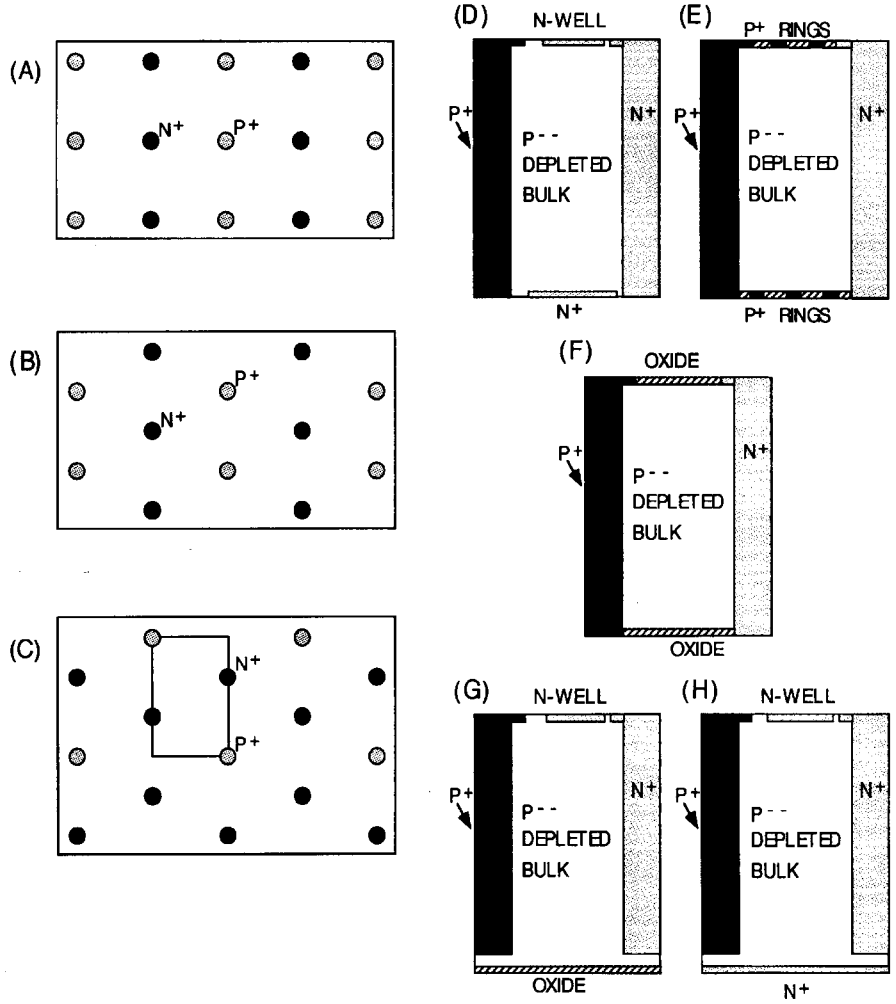


Figure 10 - Top views (a)-(c), and side views (d)-(h) of several possible structures.

Figure 11 shows equipotentials for one cell of Figure 10a, for 10^{12} net dopant atoms/cc, and 10V applied bias. Figures 12a and 12b show the electric field magnitudes for Figure 10a along a line connecting an n^+ electrode with a p^+ one directly opposite, and along a parallel line through the middle of the cell. Figure 13 shows a potential distribution for the cell of Figure 10c. Should poly electrodes be used, ones that penetrate only part way might be useful, if charge collection speed or efficiency for the small number of tracks that are fully contained in the electrodes prove to be lower than needed. All tracks will then make signals in the section of silicon below the electrodes (another way, of course, would be to glue two etched-through detectors together with an offset).

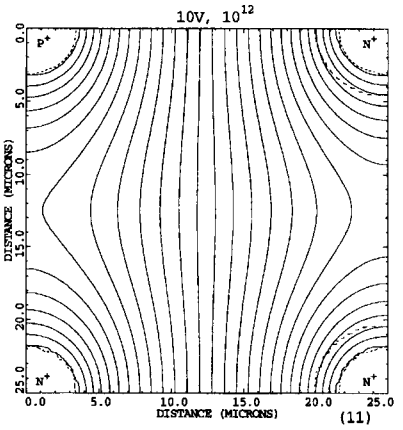


Figure 11 - Equipotentials for a cell of Fig. 10a, 10^{12}/cc doping, 10V.

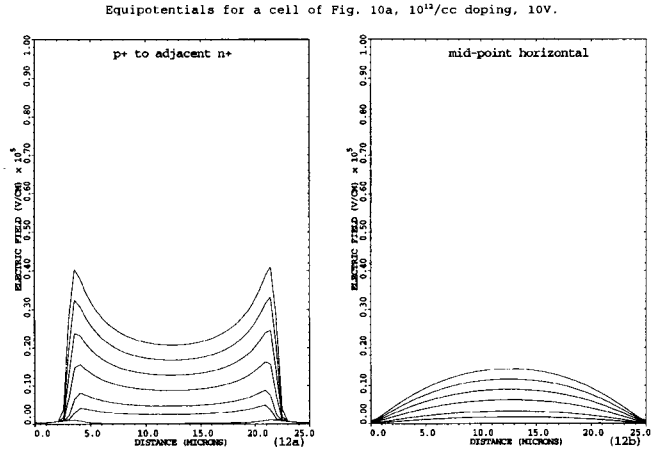


Figure 12 - Electric field magnitudes for 50, 40, 30, 20, 10, 5V (top to bottom) of Fig. 10a for (a) along a line connecting a p^+ and an adjacent n^+ electrode, and (b) along a horizontal line through the middle of Figure 11.

Small wells, covering only part of the top, could be used to hold simple driving electronics for a strip readout, such as is planned for a possible mammography detector [2]. Electronics that places differential signals on twin x and twin u or y lines that drive differential receivers, would permit two-dimensional readout using single-sided technology. There would be negligible danger of interference between crossing signals, given the double subtraction at the crossing and at the receiver. The signal height would be nearly independent of the strip length, and incoherent noise would grow no faster than the square root of the length. For small-angle stereo, it would allow readout from the ends only, since u lines reaching one edge could be crossed over the x lines and brought to the other edge from which they would continue at their stereo angle.

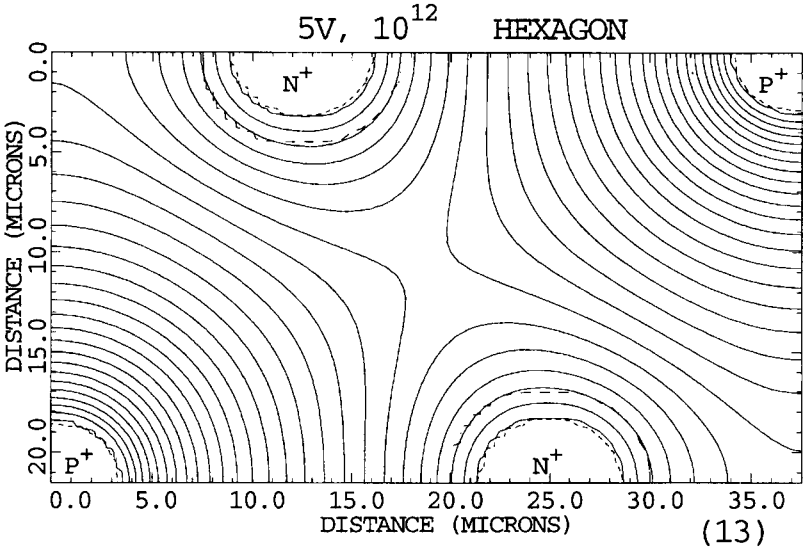


Figure 13 - Equipotentials for a cell of Fig. 10c, 10^{12}/cc doping, 10V.

IX. Charge collection from electrodes

Charge from tracks contained within the electrodes will leave them by diffusion and, for epi electrodes, from electric forces due to the built-in fields. Coulomb forces within the ionization charge cloud itself can either hinder or help charge collection once part of the charge has been collected. For example, in the case of floating n^+ electrodes, once some holes have diffused out to the collection field and have been removed, the net negative charge will tend to attract the remaining holes, slowing their diffusion out of the electrode. If, however, the electrons have been collected by electronics connected to the n^+ electrode, there will be a net repulsion that will speed up hole collection.

The fraction of tracks contained entirely within an electrode depends on their angular distribution as well as the electrode cross-sectional area. Table 1 shows, for an n^+ electrode on the diagonal between two p^+ ones of Figure 2c, and for several radial bands, the percentage of a 50 microns x 50 microns square cell occupied by the band. The next row shows the probability for the track to remain inside the band outer radius, for a beam distributed uniformly over π steradians centered around the normal to the detector. The probability for the entire track to stay within r_{max} is the product of the band area and solid angle factors. For a more tightly aligned beam, the product increases to that of the area fraction alone, although for very tightly aligned beams, the detector can be tilted, reducing the fully contained fraction to zero. The next two rows show the times to the pulse peak and to the 50% charge collection time for an applied voltage of 10V and epi electrodes. The next two rows show similar times for poly electrodes without built-in fields, and with the electrons collected by the attached electronics. The final two rows are for floating poly electrodes with the electrons left in the electrode.

Tracks will also be contained within the p^+ electrode and the two n^+ electrodes adjacent to it, roughly tripling the table area fractions. The times for these electrodes will be shorter than for the n^+ one given in the table.

track	r	1.0	2.0	3.0	4.0	5.0	microns
band	r_{min}	0.0	1.5	2.5	3.5	4.5	microns
	r_{max}	1.5	2.5	3.5	4.5	5.0	microns
band area / cell area		0.283	0.503	0.754	1.005	0.597	%
solid angle / π		0.0025	0.0069	0.014	0.023	0.028	%
time - epi	peak	2.9	2.7	2.3	2.2	2.1	ns
	.5 Σq	3.1	2.7	2.3	2.1	2.0	ns
time - poly, e- out	peak	4.5	4.1	3.5	2.4	1.9	ns
	.5 Σq	6.6	5.8	4.3	2.8	1.9	ns
time - poly, e- in	peak	5.1	4.7	3.5	2.5	2.0	ns
	.5 Σq	8.3	6.8	4.7	3.1	1.9	ns

Table 1. Pulse times for tracks at a radius r within an n^+ electrode centered in a 50 microns x 50 microns cell. The electric field within the poly is assumed to come only from other holes (e- out) (electrode connected to electronics which collects the electrons) or both holes and electrons (e- in). Estimated errors in the times range from 5% to 10%. For poly electrodes, the time to collect 90% of the charge is about three times that to collect 50%.

X. Gallium arsenide

Similar deep holes can be etched in gallium arsenide [9] and filled using metal-organic chemical vapor deposition, for example with trimethyl gallium and arsine [16]. Such a detector would circumvent the present limitations on maximum drift distances and make an efficient x-ray detector. With its low depletion voltages, it should be possible to keep the electric field near values that give high drift velocities, producing sub-nanosecond collection times. Combining this with the parallel processing capabilities of a pixel readout [17] would produce a detector capable of handling very high rates.

XI. Initial etching tests

The STS etcher [18], which is to be used for the deep holes, was new and had not been characterized. To measure its capabilities and determine the proper settings, we first etched arrays of holes and trenches of varying sizes. Optical microscopes with through-the-lens light systems, have convergence angles that are too large to illuminate most of the sides, let alone the bottom of the holes, and a depth of field that is too small. Scanning electron microscopes have an adequate depth of filed, but still have illumination and angle-of-view problems.

Sawing through the etched wafer (and some of the holes) provided the needed side views. Chipping along the hole edges produced several-micron irregularities which did not seriously degrade the diameter measurements. They did, however, leave some uncertainty in our knowledge of the smoothness of the hole walls.

The test structures shown in Fig. 14, cylindrical pillars centered in 290 micron deep holes and connected to the wall by thin webs, solved that problem, since some saw cuts completely missed the pillars, which can be seen to have smooth, vertical side walls. After etching, but before sawing, the structures shown were coated with a 2 micron thick layer of poly.

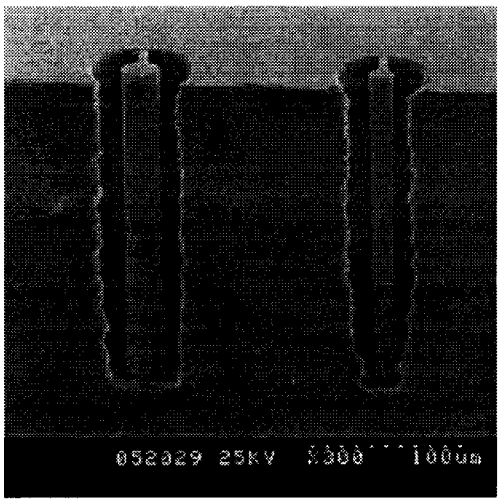


Figure 14 - Scanning electron microscope view of etched, poly-coated, 290 micron - high test structure. The scale at the lower right only applies to horizontal dimensions. Vertical ones are compressed by a factor of about 0.7.

Fig. 15 shows (a) the top, and (b), the bottom of the right column of Fig. 14. Both have radii of 7.9 microns. The lip at the top protrudes an additional 0.44 microns, while the radius halfway down is 1.2 microns less. Fig. 15c shows the bottom of a similar column without the poly. The poly is not only highly conformal, but also has a smooth surface.

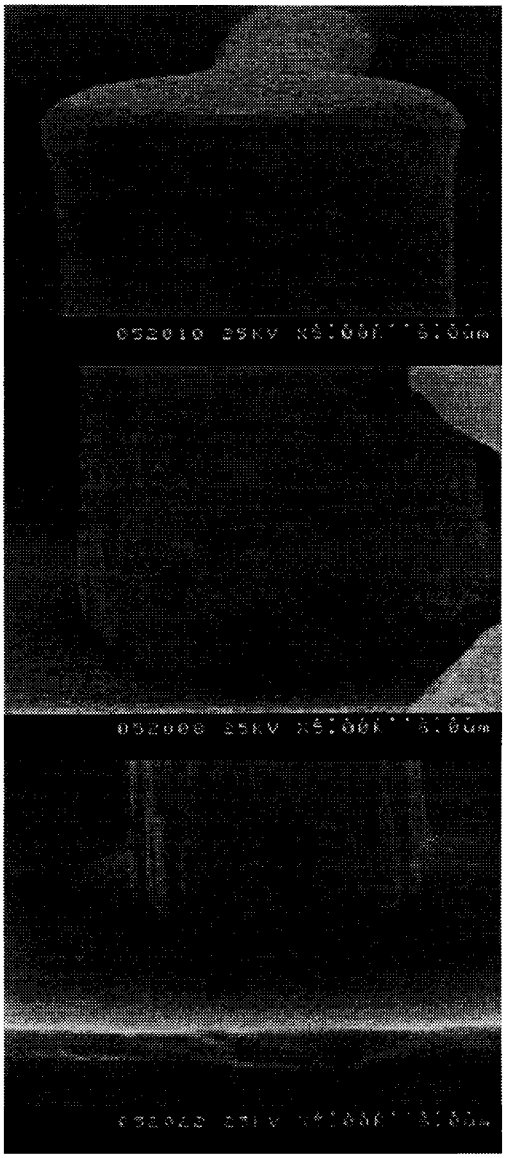


Figure 15 - (a) High-magnification view of the top of the right column of Fig. 14; (b) view, at the same scale, of the bottom of the same column; (c) view, at the same scale, of a similar column without the poly coating.

Acknowledgments

Since commercial ion-implanters have penetration ranges of only a few microns, the development of deep etching has been crucial for this technology. Many people have worked on it, particularly for micromachining applications. We would especially like to thank Kurt Petersen, Nadim Maluf, Christopher Storment, and Gregory Kovacs. Jim McVittie first let one of us know about the low sticking probability of silane, which was one of the key pieces of knowledge that led

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