SLAC–PUB–6414
December 1993

A 700 MHz Switched Capacitor Analog Waveform Sampling Circuit

Gunther M. Haller

[1]Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309

Bruce A. Wooley

Center for Integrated Systems, Stanford University, Stanford, CA 94305

Journal of Solid State Circuits

Work supported in part by Department of Energy contract DE-AC03-76SF00515

A 700 MHz Switched Capacitor Analog Waveform Sampling Circuit*

Gunther M. Haller
Stanford Linear Accelerator Center
Bruce A. Wooley
Center for Integrated Systems
Stanford University
Stanford, Ca 94305

Correspondence Address:
Gunther M. Haller
Stanford Linear Accelerator Center
P.O. Box 4349, MS 96
Stanford, California 94309
Phone: (415) 926-4257
FAX: (415) 926-2923

I. INTRODUCTION

Many modern data acquisition systems require the recording of analog signals as a function of time over a wide dynamic range. Most commonly, the analog information is digitized at the required acquisition rate using an analog-to-digital converter (ADC). However, in a number of applications analog waveforms need only be captured as snap shots; continuous digitization is not necessary. Examples of such applications include pulse echo phenomena (RADAR, LIDAR, ultrasonics, and non-destructive material and medical testing), pulse shape recording (high energy physics experiments, accelerator diagnostics), and laboratory instrumentation (oscilloscopes, transient digitizers). In such cases an input waveform can be sampled at a high rate for a limited period of time, and the samples stored in an analog memory. The analog samples are then retrieved at a lower rate and digitized with a slow ADC before a new waveform is acquired. Many

* This research was supported by the Department of Energy under Contract No. DE-AC03-76SF00515.

channels may be multiplexed onto one converter when readout speed and latency are not crucial. Advantages of using an analog memory include low overall power dissipation and cost, high density, and potentially superior dynamic range at high sampling rates.

Two main technologies are available for the realization of an integrated analog memory: charge-coupled devices (CCD's) and switched-capacitor circuits. Integrated circuits based on switched-capacitor techniques are inherently capable of higher accuracy and sampling rates than CCD devices. Furthermore, CCD's require elaborate clocking circuitry that generally dissipates considerable power.

Strong cost and performance incentives especially encourage the use of analog switched-capacitor memories in high energy physics experiments [1]. Fast analog waveform capture for thousands of channels must be provided with a minimum of power dissipation. The design challenge is to produce a uniform and linear response in a large number of memory cells at a level of performance comparable to the high accuracy inherent in the technology. Principal performance issues are cell-to-cell offset and gain variations within a memory channel, which are governed by the circuit architecture and its sensitivity to the matching properties of its constituent transistors and capacitors [2]-[5]. In high-precision applications, the lowest achievable cell non-uniformities may not be acceptable and therefore must be eliminated by correcting the data. In large systems, it is essential that the number of correction constants and the computational effort be minimized.

Early analog memory circuits based on a sample-and-hold topology contain a sampling switch, a storage capacitor, and a readout buffer in each memory cell [6]-[9]. In order to meet the need for lower power and higher density, architectures based on switched-capacitor circuits were introduced [10]-[14]. In these circuits, each channel comprises a bank of capacitors that is switched to a single operational amplifier for readout. Architectures in which the sampling transistors are placed in the signal path [6]-[13] exhibit signal-dependent charge injection in each cell. Cell pedestals are therefore a function of the input signal and may require individual offset and gain corrections. In addition, a serious drawback of these implementations in high-speed applications is the dependence of the sampling transistor turn-off time on the signal level [7]. In circuits

based on traditional charge redistribution switched-capacitor techniques [14], sampling-switch charge injection can be made independent of the signal level, but the cell gain is a linear function of the size of the storage capacitor. Cell-to-cell gain matching of better than 0.5 % across an entire channel is therefore difficult to achieve, and both offset and gain corrections are commonly needed for each cell. The sampling speed of published analog memory circuits is presently limited to less than 150 MHz.

This work presents a circuit that enables sampling rates as high as 700 MHz while sustaining a dynamic range of more than 12 bits. In addition, cell pedestals are independent of the signal amplitude, cell gains are insensitive to component sizes, and the sampling time is independent of the input level. This allows a straightforward improvement in performance by means of a simple offset subtraction. Cell-to-cell gain corrections are not needed.

A specific application for the proposed memory is high energy physics accelerators and colliders, where bunches of particles are transported at close to the speed of light inside beam pipes several miles long [15]-[17]. In order to control the operation of the particle beam with sufficient accuracy, its transverse position must be measured at as many as a thousand locations with a precision of better than 1 μm across a range of 5 mm. The complexity and cost of such a measurement system can be significantly reduced through use of high-speed, high dynamic range analog memories.

The proposed analog memory circuit is described in detail in Section II of this paper. In Section III, the design of the on-chip write and read control circuitry is explained. Experimental results characterizing the performance of the memory are presented in Section IV.

II. ANALOG MEMORY DESCRIPTION

Shown in Fig. 1 is a block diagram of an analog waveform recorder with m memory channels. The analog waveforms applied at the m inputs are sampled and stored in the main analog memory core. The write and read addresses for the core are generated in the write and read control blocks,

respectively. Since all memory channels are written and read simultaneously, the addresses are common to all channels. In applications where the readout time permits the serial readout of the channels, the m outputs can be read out on a single common output line by including an on-chip analog multiplexer.

A simplified schematic of one channel of the proposed analog memory, comprising n memory cells, is shown in Fig. 2. Each memory cell consists of a large write (sampling) transistor, M_{wi}, a minimum-size read transistor, M_{ri}, and a storage capacitor, C_i. The cells are addressed via write lines ϕ_{w1} through ϕ_{wn} and read lines ϕ_{r1} through ϕ_{rn}. The top plates of the storage capacitors are interconnected and can be shorted to the channel input or output by means of switches M_{in} and M_{out}. Voltage V_C is a dc reference common to the sources of all write transistors, M_{wi}. Transistor M_{rst} serves to configure the operational amplifier as a voltage follower in order to force the nodes at the amplifier input and output to the dc bias level V_B during reset.

The operation of the circuit can be described by dividing the data acquisition process into write and read cycles. In the write phase, analog signals applied at the channel input, V_{in}, are sampled and stored in the memory cells at a high rate. The stored analog information is subsequently read out serially at the channel output, V_o, at a lower speed.

During the write phase, switch M_{in} is turned on, connecting the signal V_{in} to the input bus, while switch M_{out} and the read switches M_{r1} through M_{rn} are all off, isolating the input bus from the read bus. Switch M_{rst} is on to keep the read bus at a defined potential, V_B, during the entire write phase. An analog signal applied at the circuit's input is sampled onto the cell capacitors C_i by sequentially turning transistors M_{w1} through M_{wn} on and off as illustrated in Fig. 3(a). Samples of the input waveform at n discrete times are thereby stored in the memory channel.

The voltage ΔV_{si}, stored across capacitor C_i in memory cell i, $1 \le i \le n$, after sampling is

$$\Delta V_{si} = V_{in} - V_C - \Delta V_{pwi} \tag{1}$$

where ΔV_{pwi} is the voltage error due to charge injection in switch M_{wi} during turn-off [18]-[21].

The source and drain terminals of the write transistor are at the reference voltage V_C at turn-off. If the cell capacitance C_i is much larger than the parasitic capacitances associated with the read and write transistors, then ΔV_{pwi} can be written as [18]

$$\Delta V_{pwi} = -\frac{\frac{C_{ox}W_{wi}L_{wi}}{2} + C_{wi}}{C_i}\sqrt{\frac{\pi UC_i}{2\beta}}erf\left(\sqrt{\frac{\beta}{2UC_i}}(V_H - V_T - V_C)\right)$$

$$-\frac{C_{wi}}{C_{wi}+C_i}(V_C + V_T - V_L) \tag{2}$$

where C_{wi} is the write-transistor gate overlap capacitance, C_i is the sampling capacitance, V_T is the threshold voltage, V_L and V_H are the low and high levels of the write-transistor gate voltage, C_{ox} is the oxide capacitance per unit area, W_{wi} and L_{wi} are the width and length of the write transistor, U is the slew rate of the gate voltage, $\beta = \mu_n C_{ox} W_{wi}/L_{wi}$, and μ_n is the electron mobility in the channel. The equation must be modified [19] if the associated parasitic capacitances and the oxide capacitance are not negligible compared to C_i, but the important fact for this investigation is that in either case ΔV_{pwi} remains independent of the input voltage, V_{in}.

After the write phase has been completed and the input waveform is stored in the analog memory, the read cycle is initiated. During readout, the switch M_{in} is turned off while M_{out} and M_{rst} are turned on, forcing the input and read bus to V_B. M_{rst} is then turned off and the voltage stored in the first cell is read out by turning transistor M_{r1} on as illustrated in Fig. 3(b). After the output has settled, the signal may be digitized with an external low-speed, low-power A/D converter. Following digitization, M_{rst} is again turned on and M_{r1} is turned off, which forces the input bus back to V_B in preparation for the readout of the next cell. This cycle is repeated for all cells. It is essential that the input bus always be forced back to V_B before a new cell is read out; otherwise, charge sharing and parasitic capacitance effects will seriously degrade the performance of the memory. By turning the cell read switches off after the reset switch is turned on, the potential

across the capacitors is initialized to a defined state for the next write phase. The minimum readout time depends on the number of cells to be read out and the performance of the amplifier.

Once the write switch is turned off, the cell capacitor nodes connected to the cell transistors are left in a high-impedance state for the remainder of the write phase and the entire read phase. The charge at these nodes is thus conserved and, with the input and output bus forced to V_B between the readout of adjacent memory cells, only three parasitic capacitances influence the dc transfer function of a memory cell. One is the capacitance C_{pi} associated with the cell sampling capacitor terminal that is connected to the write switch M_{wi}. C_{pi} comprises the parasitic capacitance of the sampling capacitor together with the drain-substrate capacitance of the read switch and the drain-substrate and gate overlap capacitances of the write switch. The second parasitic capacitance is the gate overlap capacitance of the read switch, C_{ri}, and the third parasitic to be considered is the capacitance, C_{pp}, between the input bus and the read bus. C_{pp} consists of the capacitance between the inverting input and output of the amplifier (a fraction of the gate-drain capacitance of the amplifier input transistor) together with capacitances associated with interconnections on the chip.

In the proposed memory the voltage across the cell capacitor, rather than the charge stored on that capacitor, is sensed during readout. When memory cell i is selected for readout, the voltage at the output of the amplifier, V_{oi}, can be described as a function of the input voltage, V_{in}, in the form [19]

$$V_{oi} = A_i V_{in} + V_{offi} . \tag{3}$$

The gain factor A_i is given by

$$A_i = \frac{1}{1 + \frac{C_{pp}}{C_i} + \frac{1}{G}\left(1 + \frac{C_{pi} + C_{pp}}{C_i}\right)} \approx \frac{1}{1 + \frac{C_{pp}}{C_i}} \tag{4}$$

where G is the open-loop gain of the operational amplifier. From a technical standpoint, the sampling capacitance C_i can be made large compared to C_{pp}, which, because of careful circuit layout,

is dominated by the input-to-output capacitance of the amplifier. The open-loop gain G of the amplifier should exceed 60 dB for practical CMOS circuits, so that A_i is close to one.

The offset voltage, V_{offi}, in (3) is given by

$$V_{offi} = V_B - A_i V_C + A_i \frac{C_{pi}}{C_i}(V_B - V_C) + A_i V_{poi} + V_{ch} . \tag{5}$$

V_{ch} is an offset voltage term common to all cells in one channel and includes both the charge injected at the turn-off of reset switch M_{rst} and the amplifier input offset voltage. The cell-specific parasitic offset voltage, V_{poi}, is

$$V_{poi} = \frac{2C_{ri}}{C_i}(V_L - V_H) - \frac{C_{ox}W_{ri}L_{ri}}{C_i}(V_H - V_B - V_T) - \Delta V_{pwi}\left(1 + \frac{C_{pi}}{C_i}\right) \tag{6}$$

where W_{ri} and L_{ri} are the width and the length of the read transistor.

Because, as indicated by (4)–(6), both A_i and V_{offi} are independent of the input voltage, V_{in}, it follows that the output voltage of the analog memory channel, V_o, is a linear function of V_{in}.

For applications where a high input bandwidth is required, the write transistor must be made large because the cell bandwidth, B, is determined by the size of the sampling capacitor and the resistance of the write transistor:

$$B \propto \frac{\mu_n C_{ox}\frac{W_{wi}}{L_{wi}}(V_H - V_C + V_T)}{C_i} . \tag{7}$$

The bandwidth of a memory cell and the size of the error voltage ΔV_{pwi} are therefore correlated.

In order to simplify the calibration and correction procedure, the uniformity of the sampling cell transfer characteristics must be considered. In the architecture presented here, memory cell response variations across a channel are governed by switch charge injection mismatch of the large write transistors. With the reference voltage V_C set to the bias voltage V_B, and W_w much larger than W_r (width of the minimum size read switch), the output voltage is approximately

$$V_{oi} = V_{in} - \Delta V_{pwi}\left(1 + \frac{C_{pi}}{C_i}\right). \tag{8}$$

In fast turn-off conditions the variation in channel charge dominates the charge injection mismatch [3] and can be modeled as part of the mismatch of two geometric parameters, the channel width and length. Smaller switches yield smaller pedestal mismatches but limit the signal bandwidth of the sampling cell. The size of the write transistor is thus a trade-off between input bandwidth and pedestal mismatch for a given sampling capacitor value, which in turn is chosen on the basis of thermal noise considerations and the need to make relevant parasitics negligible.

A single NMOS transistor is used as a write switch to avoid the need for complementary control signals, which impose a burden on high speed designs. Complementary cell switches would reduce the overall cell pedestal sizes, but would not improve and might even worsen the cell pedestal uniformity across a channel. Since the pedestals can be accurately determined and then subtracted from the output by either analog or digital methods, their mean value is not of great concern. The pedestals are measured by applying a dc reference level at the channel input, recording the responses of the cells, and then subtracting the results during readout. In this context it is important that the charge injected by transistors M_{w1} through M_{wn} not depend on the signal level, as is the case in [6]-[13]. Note that in the analyses presented in some of these references the error voltages from the sampling switches are neglected, which is not a valid assumption for a high input-bandwidth analog memory.

The influence of the size of the sampling cell capacitance on the memory cell gain can be derived from (4), and the gain variation across a channel as a function of capacitor mismatch is

$$\frac{dA}{A} = \frac{C_{pp}}{C_i + C_{pp}}\left(\frac{dC_i}{C_i}\right). \tag{9}$$

The parasitic capacitance C_{pp} is small compared to practical values for the cell sampling capacitance C_i. As a result, it is expected that the gain will be insensitive to the capacitance mismatch and thus uniform across a memory channel.

Since the cell capacitor nodes connected to the cell transistors remain floating after the write switch is turned off, care must be taken to ensure that no leakage occurs at those nodes, for all possible ac and dc input signals, during the entire write and read phases. To avoid subthreshold leakage, the maximum input voltage swing, ΔV_{in}, in the write phase is limited to

$$\Delta V_{in} \leq V_C - V_L \,. \tag{10}$$

For the same reason, the maximum voltage swing ΔV_{oi} at the output of the amplifier must be less than $V_B - V_L$ during the read phase. The corresponding limit for the input voltage swing during the write phase is then

$$\Delta V_{in} = \frac{\Delta V_{oi}}{A_i} \leq \frac{V_B - V_L}{A_i} \,. \tag{11}$$

From (10) it is apparent that the maximum voltage swing is limited by the value of reference input voltage, V_C, which must be chosen such that the sampling switch impedances are small enough to achieve the desired bandwidth, as given by (7). The bias level V_B is set to avoid leakage during the read phase and to ensure that V_o does not exceed the amplifier output voltage range.

A common input switch, M_{in}, could be used in the circuit of Fig. 2 because of the relatively small number of memory cells required in each channel for the intended application. This input switch must be large enough to achieve the desired bandwidth in the presence of the parasitic capacitance of the input bus and the combined capacitance of the addressed memory cells.

Finally, it should be noted that in the design presented herein, the turn-off time of the sampling switches M_{wi} is independent of the signal level, thus eliminating a timing error that would otherwise be present for high-frequency input signals.

III. CONTROL CIRCUIT DESCRIPTION

Traditionally, shift-registers have been used for write address control in analog memory circuits. At sampling rates above 100 MHz this approach is difficult to implement, and in the present

design a starved inverter delay chain, illustrated in Fig. 4, is used instead. Such inverter chains have been employed previously in digital applications [22]. Each delay element in the chain consists of five MOS transistors, as indicated by the shaded box in Fig. 4. A write pulse applied at input A_{in} propagates through the delay elements, thereby producing the write address signals ϕ_{w1} through ϕ_{wn} for the analog memory core. The delay of the write pulse through the chain is set by control voltage V_{ctr}, which thus determines the write sample frequency. The minimum width of the write pulse A_{in} (minimum acquisition time of the memory cell) is constrained by the accuracy with which the analog signal is to be acquired and the input time constant of the sampling cell.

In order to ensure a delay, and thus sampling frequency, that is independent of variations in the fabrication process, a servo feedback circuit, also shown in Fig. 4, is used. The leading edge of a reference input signal A_{ref} is compared to the trailing edge of the last write sample clock ϕ_{wn}. When the delay is less than the intended value, logic gate U_1 turns transistor M_1 on, which in turn connects current source I_1 to capacitor C_s. The voltage across C_s is increased, thereby slowing the inverter chain via the control voltage V_{ctr} . Likewise, V_{ctr} is reduced via current source I_2 should the inverter chain delay increase above the ideal value. The time difference $t_{ref} - t_{in}$ between input signals A_{in} and A_{ref} thus determines the resulting write sample frequency, $f_s = n/(t_{ref} - t_{in})$. This feedback circuit eliminates the sensitivity of the delay chain to process parameters and compensates for the effects of temperature and supply variations.

The speed with which V_{ctr}, and thus the sampling frequency, can be adjusted, is governed by the magnitudes of currents I_1 and I_2 and the size of capacitor C_s, which is selected to avoid perturbations from leakage currents of switches S_1 and S_2 between acquisition cycles. The net leakage current is given by the sum of the currents flowing through the four reverse-biased source/drain pn-junctions of S_1 and S_2 in Fig. 4. Switch S_1 is included so that the voltage across C_s is modified only while the delays are being compared during the write phase. Switch S_2 is added to ensure that V_{ctr} is remains constant during the write phase. S_2 is turned on during the read phase in order to update V_{ctr} in preparation for the next write cycle. The start-up time of the circuit is determined by the sizes of I_1, I_2, and C_s.

The readout of a memory channel is implemented with an on-chip two phase shift-register together with the logic used to generate the read control signals ϕ_{r1} through ϕ_{rn}, as illustrated in Fig. 5. The serial input signal ϕ_{in} is shifted through a dynamic register by non-overlapping clocks ϕ_{sr1} and ϕ_{sr2}. The enable signal ϕ_{en} is used to disable the read addresses while the device is reset between readout of two successive memory cells, as shown in Fig. 3.

IV. EXPERIMENTAL RESULTS

The analog memory circuit has been fabricated in a 2-μm CMOS technology with poly-poly capacitors. Fig. 6 is a die photo of the prototype. Two channels with 32 memory cells in each were integrated in the experimental device. The area of a memory cell is 40 x 40 μm^2 and is dominated by the 0.5 pF capacitor and the sampling switch (W/L=50 μm/2 μm) in each cell. The dc power dissipated from a single 5-V supply by each 32-cell channel was measured to be 2 mW and is dominated by the folded-cascode amplifier. The output voltage range of such an amplifier [23] is a good match to the limited input signal range of the analog memory, as indicated by (10) and (11). This type of amplifier also provides sufficient gain, speed, and noise performance.

The performance of the analog memory was evaluated by driving the input with high-quality pulse, dc, and sinusoidal signal sources, digitizing the data read out from the memory with a commercial 16-b ADC, and transferring the acquired data to a workstation for processing.

The response of one channel to a 2-V input voltage step with a 3-ns rise time is shown in Fig. 7(a) and illustrates the operation of the device with V_C and V_B set to 2.5 V. The output signal alternates between the output levels of the 32 cells and the amplifier reset level V_B as illustrated in Fig. 3. The delay feedback control signal A_{ref} was adjusted to establish a sampling rate of 700 MHz (1.42 ns between the turn-off of adjacent sampling transistors). The readout time for each cell was set at 11 μs, which is the conversion time of the 16-b ADC used in the test setup. The settling time of the analog memory output to 0.1% is 1 μs. In Fig. 7(b) the output pulse is plotted as a function of input time, and the results agree with the input pulse monitored on an

oscilloscope with respect to rise and fall time, pulse width, and the signal undershoot. The input time constant of the memory, defined as the product of the on-resistance of the write transistor and the capacitance C_i, was designed to be less than 0.5 ns for $V_C = 2.5$ V.

The nonlinearity of the experimental circuit was measured by applying 38 equally spaced input voltages and fitting the output levels to a straight line using the least-squares method. Fig. 8(a) shows the output of a typical cell plotted as a function of input voltage over a range of 3 V, and in Fig. 8(b) the deviations are shown for the chosen input voltage range of 2.5 V. The maximum deviation is 0.7 mV, or 0.03 % of full scale.

The dynamic range is commonly defined as the maximum recordable signal divided by the baseline noise, which determines the smallest detectable signal. The noise voltage for the analog memory can be expressed as

$$\bar{v}^2 = \frac{kT}{C_i} + \left(\frac{C_i + C_{op}}{C_i}\right)^2 \bar{v}_{eq}^2 \tag{12}$$

where C_{op} is the capacitance at the inverting input node of the amplifier during readout, and v_{eq} is the input-referred noise voltage of the amplifier. The baseline noise of the analog memory was determined by recording the device response to repeated measurements with a constant input and calculating the mean square error. An RMS of 0.3 mV was obtained from sets of 100 repeated measurements, independent of the input signal level. The dynamic range of the device is therefore better than 8,000/1, or 13 bits.

The cell-to-cell pedestal variations result in a RMS deviation of 1.8 mV across a channel. This is expected for the selected switch and capacitor sizes and the fabrication process used. In order to investigate whether the cell pedestals depend on the input signal, the responses to various dc input levels were recorded, and the response to one dc reference level was subtracted from these measurements. The differences for all 32 cells are plotted in Fig. 9 as a function of the input voltage. In order to plot the data on the same scale, the nominal input level has been subtracted. Each data point represents the mean value from five measurements so that variations in the result due to

baseline noise can be neglected. The RMS cell response variation after cell pedestal subtraction across the entire input signal range is only 0.3 mV, demonstrating that the sampling switch charge injection is independent of the dc input signal level and can be reduced to the level of the thermal noise by a simple subtraction.

The average gain, $\Delta V_o/\Delta V_{in}$, of a memory channel at low frequencies was measured to be 0.9967, with an RMS gain variation across the channel of 0.0001, as indicated by Fig. 10. Calibration of the channel therefore requires only a simple cell pedestal subtraction in order to achieve a precision of better than 12 bits for dc signals. The measured absolute gain agrees well with estimates based on (4).

The ac performance of the circuit has been quantitatively evaluated by applying free running sine waves of various amplitudes and frequencies at the analog input. Since the phase of the input signal was not synchronized to the sampling process, the results also provide a measure of the ac uniformity of the cells across a channel. The pedestal subtracted responses for 20 separate sets of measurements were fitted to a common frequency, offset, and amplitude of the signal and a free phase for each set of measurements [24], [25]. The signal-to-(noise+distortion) ratio (SNDR) was then calculated based on the residuals from an ideal fit. Errors can be attributed to a variety of sources, including errors in sampling time and amplitude, variations in the ac response of different cells, nonlinearities, and thermal noise.

Fig. 11 shows a 21.4 MHz sine wave fitted to the data and plotted modulo the phase along with the residuals. The fit yields RMS residuals of 0.4 mV. The amplitude and residuals remain stable for various dc input voltage levels, demonstrating the good small-signal ac linearity across the signal range. Shown in Fig. 12 is a plot of the SNDR as a function of the input amplitude, as measured for a 21.4 MHz input frequency. An input level of 0 dB represents a full-scale peak-to-peak amplitude of 2.5 V. The device achieves a peak SNDR of 60 dB and a dynamic range of 74 dB for a 21.4 MHz input.

The performance of the analog memory degrades at large signal amplitudes principally because of harmonic distortion and timing errors. Errors in sampling time can be attributed prima-

rily to two sections of the circuit, the delay chain and the feedback control. The total delay of the inverter chain is regulated by the feedback control circuit. The peak-to-peak timing jitter measured at the end of the 32 stage delay chain is less than 1 ns, which translates into 31 ps per sampling interval or delay element. This jitter corresponds to a sampling frequency error of 2 % at the 700 MHz rate and will decrease linearly with an increase in the number of delay elements. Additional error is introduced by cell-to-cell sampling time, or delay, variations. These variations have been estimated by fitting the sine wave with the individual delays of the elements as a parameter (with the same element delays for each of the 20 measurements sets). The best fit yielded an RMS value of 25 ps for the element delay variations across a channel. This timing error is due to delay element mismatch and is independent of the input signal level. This error can be corrected for if required. The approximate start-up time of the delay chain was measured to be less than ten cycles at a trigger rate of 120 Hz. For the intended application start-up effects are of no concern since the circuit is exercised long before input waveforms need to be acquired.

The performance of the analog memory is summarized in Table 1.

V. CONCLUSION

In analog waveform sampling applications switched-capacitor memories can provide superior performance with respect to cost, space, dynamic range, sampling rate, and power dissipation when compared to flash A/D converters and CCD devices. Present analog memory circuits are generally limited to sampling frequencies of 150 MHz. This paper has described a memory architecture that enables sampling rates from 200 MHz to 700 MHz by utilizing starved inverter delay elements with on-chip delay feedback compensation. In the proposed circuit, memory cell pedestals are independent of the input signal amplitude and can be eliminated by analog or digital subtraction. This is an especially important attribute in applications where digitization and subtraction are to be included on the same chip as the memory.

Analysis and measurements indicate that the gain variation from cell to cell is insensitive to the size of the capacitors, since the voltage across the capacitor, rather than the charge stored on it, is sensed during readout. The sampling time is independent of the input signal level, which is especially important for the acquisition of high-frequency input signals. For applications where sampling frequencies of less than 100 MHz are sufficient, the high-speed inverter delay chain can be replaced by traditional shift registers.

A 2 (channel) x 32 (cell) experimental device was fabricated in a 2-μm CMOS technology with poly-poly capacitors. The measured nonlinearity is 0.03 % for a 2.5 V input range and the cell-to-cell gain matching is 0.01 % RMS. The dynamic range of the device exceeds 12 bits and the peak signal-to-(noise+distortion) ratio for a full-scale 21.4 MHz sine-wave sampled at 700 MHz is 60 dB. The device has been optimized for high energy physics applications where, in general, different classes of signals covering a wide dynamic range must be processed in a channel, but where each class of signals has a limited inherent accuracy. For each class of signals it is thus sufficient to have a peak SNDR that is lower than the dynamic range of the channel. The power dissipation for one channel operated from a single +5 V supply is 2 mW.

The proposed analog memory is a viable alternative to real-time analog-to-digital converters in applications where continuous acquisition is not required. The power dissipation of the device is orders of magnitude below that typical of commercial monolithic converters, which are presently limited to a dynamic range of 8 bits for rates exceeding 100 MHz.

ACKNOWLEDGEMENT

The authors wish to thank Dr. Dietrich Freytag for numerous helpful discussions. They are also grateful for the support provided by Prof. Martin Breidenbach and Prof. David Leith of the research department at SLAC.

REFERENCES

[1] R. Larsen, "Overview of the Data Acquisition Electronics System Design for the SLAC Linear Collider Detector (SLD)," *IEEE Trans. Nucl. Sci.*, NS-33, No. 1, pp. 65-72, Feb. 1986.

[2] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid State Circuits*, vol. SC-24, pp. 1433-1439, Oct. 1989.

[3] K. Lakshmikumar, R. Hadaway, and M. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE J. Solid State Circuits*, vol. SC-21, pp. 1057-1066, Dec. 1986.

[4] J. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors," *IEEE J. Solid State Circuits*, vol. SC-16, pp. 608-616, Dec. 1981.

[5] K. Nagaraj, "Switched-Capacitor Delay Circuit that is Insensitive to Capacitor Mismatch and Stray Capacitance." *Electron. Letters*, vol. 20, pp. 663-664, Aug. 1984.

[6] J. Walker, S. Chae, S. Shapiro, and R. Larsen, "Microstore-The Stanford Analog Memory Unit," *IEEE Trans. Nucl. Sci.*, NS-32, No. 1, pp. 616-621, Feb. 1985.

[7] D. Freytag and J. Walker, "Performance Report for Stanford/SLAC Microstore Analog Memory Unit," *IEEE Trans. Nucl. Sci.*, NS-32, No. 1, pp. 622-625, Feb. 1985.

[8] G. Haller, D. Freytag, J. Walker, and S. Chae, "Performance Report for Stanford/SLAC Multi-Channel Sample and Hold Device," *IEEE Trans. Nucl. Sci.*, NS-33, No. 1, pp. 221-225, Feb. 1986.

[9] E. Franchi, M. Tartagni, R. Guerrieri, and G. Baccaranie, "Random Access Analog Memory for Early Vision," *IEEE J. Solid State Circuits*, vol. 27, pp. 1105-1109, July 1992.

[10] K. Matsui, T. Matsuura, S. Fukasawa, Y. Izawa, Y. Toba, N. Miyake, and K. Nagasawa, "CMOS Video Filters Using Switched Capacitor 14-MHz Circuits," *IEEE J. Solid State Circuits*, vol. SC-20, pp. 1096-1101, Dec. 1985.

[11] S. Kleinfelder, "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit," *IEEE Trans. Nucl. Sci.*, NS-37, pp. 1230-1236, June 1990.

[12] D. Munday, et. al., "A 66 MHz, 32-channel Analog Memory Circuit with Data Selection for Fast Silicon Detectors," *Nucl. Inst. and Meth. in Phys. Research,* A-326, pp. 100-111, 1993.

[13] R. Horisberger and D. Pitzl, "A Novel Readout Chip for Silicon Strip Readout Detectors with Analog Pipeline and Digitally Controlled Analog Signal Processing," *Nucl. Inst. and Meth. in Phys. Research,* A-326, pp. 92-99, 1993.

[14] J. Moeschen, A. Caldwell, L. Hervas, B. Hosticka, U. Koetz, B. Sippach, "High-Speed Analog CMOS Pipeline System," *Nucl. Inst. and Meth. in Phys. Research,* A-288, pp. 180-186, 1990.

[15] J. Pellegrin, M. Ross, B. Scott, and D. Wilson, "Beam Trajectory Acquisition System for the Arcs of the Stanford Linear Collider," *Proc. IEEE Particle Accelerator Conference,* vol. 2, pp. 673-675, May 1991.

[16] M. Ross, "Beam Diagnostics and Control of SLC," *Proc. IEEE Particle Accelerator Conference,* vol. 2, pp. 508-511, May 1991.

[17] R. Ruth, "Linear Colliders," SLAC-PUB-5597, July 1993.

[18] B. Sheu and C. Hu, "Switch-Induced Error Voltage on a Switched Capacitor," *IEEE J. Solid State Circuits*, vol. SC-19, pp. 519-525, Aug. 1984.

[19] G. Haller, "High-Speed, High-Resolution Analog Waveform Sampling in VLSI Technology," *Ph.D Thesis*, Stanford University, 1994.

[20] G. Wegeman, E. Vittoz, and F. Rahali, "Charge Injection in Analog MOS Switches," *IEEE J. Solid State Circuits*, vol. SC-22, pp. 1091-1097, Dec. 1987.

[21] J. Shieh, M. Patil, and B. Scheu, "Measurement and Analysis of Charge Injection in MOS Analog Switches," *IEEE J. Solid State Circuits*, vol. SC-22, pp. 277-281, Apr. 1987.

[22] Y. Arai and T. Baba, "A CMOS Time to Digital Converter VLSI for High-Energy Physics," *1992 Symposium on VLSI Circuits Digest of Technical Papers,* pp. 121-122, June 1988.

[23] P. Gray and R. Meyer, "MOS Operational Amplifier Design - A Tutorial Overview," *IEEE J. Solid State Circuits*, vol. SC-17, pp. 969-982, Dec. 1982.

[24] B. Peetz, A. Muto, and J. Neil, "Measuring Waveform Recorder Performance," *Hewlett Packard Journal*, vol. 33, No. 11, pp. 21-29, Nov. 1982.

[25] B. Boser, K. Karman, H. Martin, and B. Wooley, "Simulating and Testing Over-Sampled Analog-to-Digital Converters," *IEEE J. Solid State Circuits*, vol. SC-7, pp. 668-673, June 1988.

FIGURE CAPTIONS

Figure 1 Block diagram of an analog waveform recorder with *m* memory channels.

Figure 2 Simplified schematic of the analog memory circuit.

Figure 3 Timing diagram for the (a) write and (b) read phase.

Figure 4 Write control circuit with starved inverter delay elements and feedback compensation circuit.

Figure 5 Read control circuitry.

Figure 6 Prototype die photo.

Figure 7 Response of one channel to a 2-V input voltage step with a 3-ns rise-time sampled at 700 MHz. Pulse is plotted on an (a) read and (b) write time scale.

Figure 8 (a) Output plotted as a function of input voltage for a 3-V input range. (b) Deviations from a linear fit for the selected 2.5 V input voltage range.

Figure 9 Pedestals of all 32 cells in one channel as a function of input voltage after subtraction of the response to a reference input level. The nominal input value is subtracted. (Several data points are super-imposed).

Figure 10 Gain of all 32 cells in one channel.

Figure 11 Upper: Results of 20 measurement sets fitted to a 21.4 MHz sine wave and plotted on a time scale modulo the period of the sine wave. Lower: Residuals from the fit.

Figure 12 Signal-to-(noise+distortion) ratio as a function of amplitude for a 21.4 MHz sine wave sampled at 700 MHz.

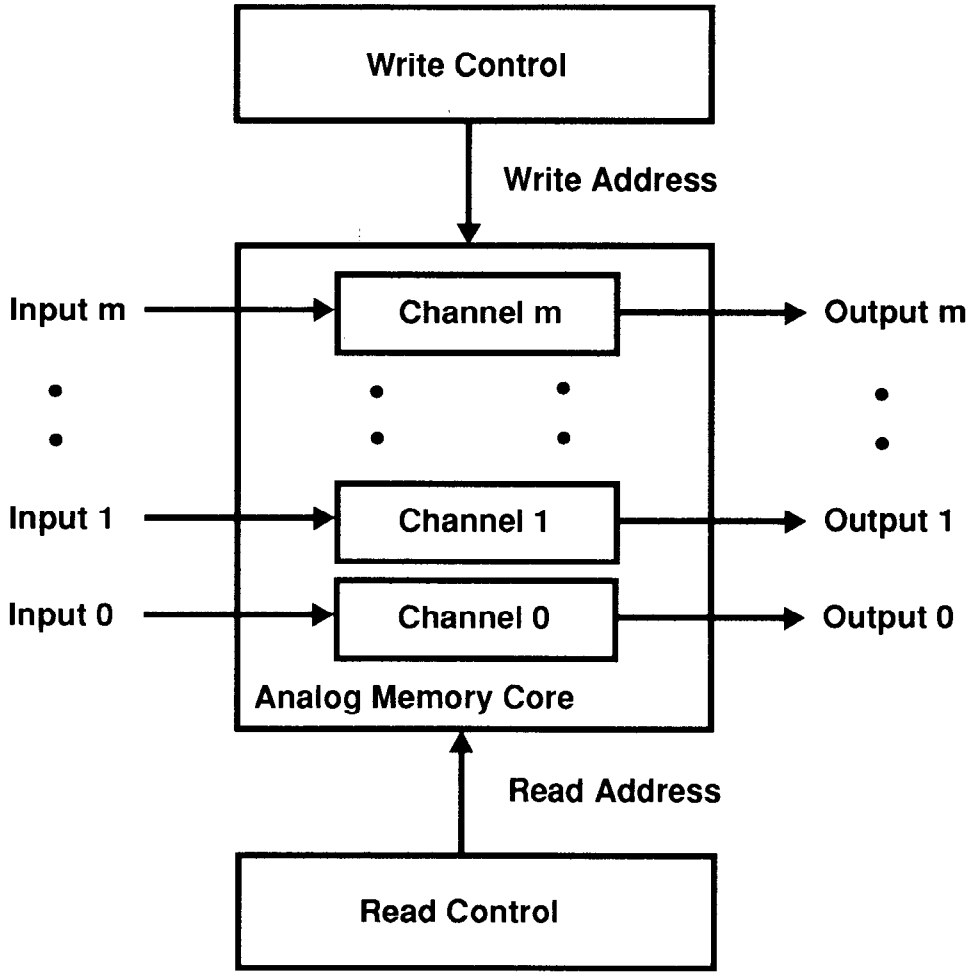

Figure 1: Haller and Wooley

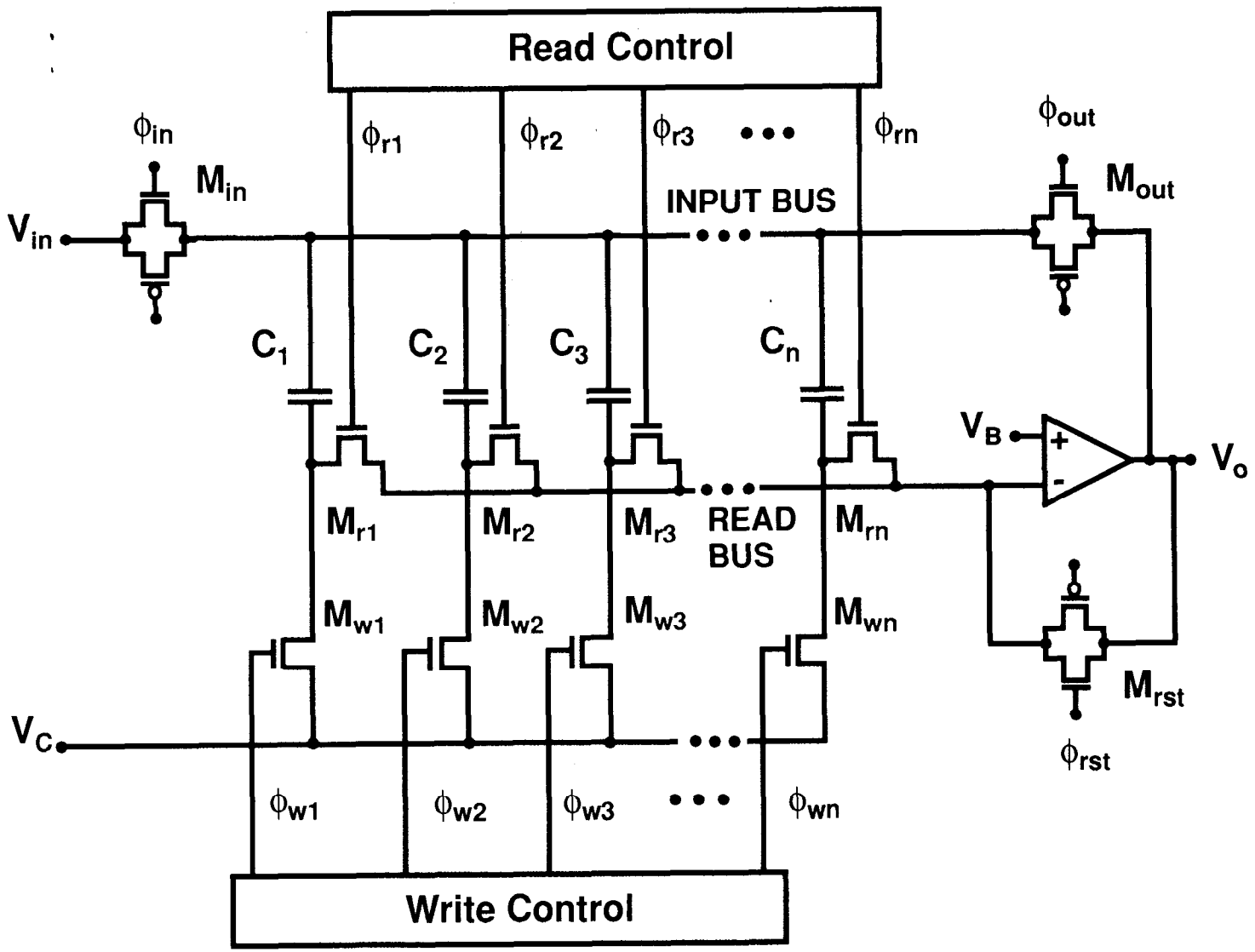

Figure 2: Haller and Wooley

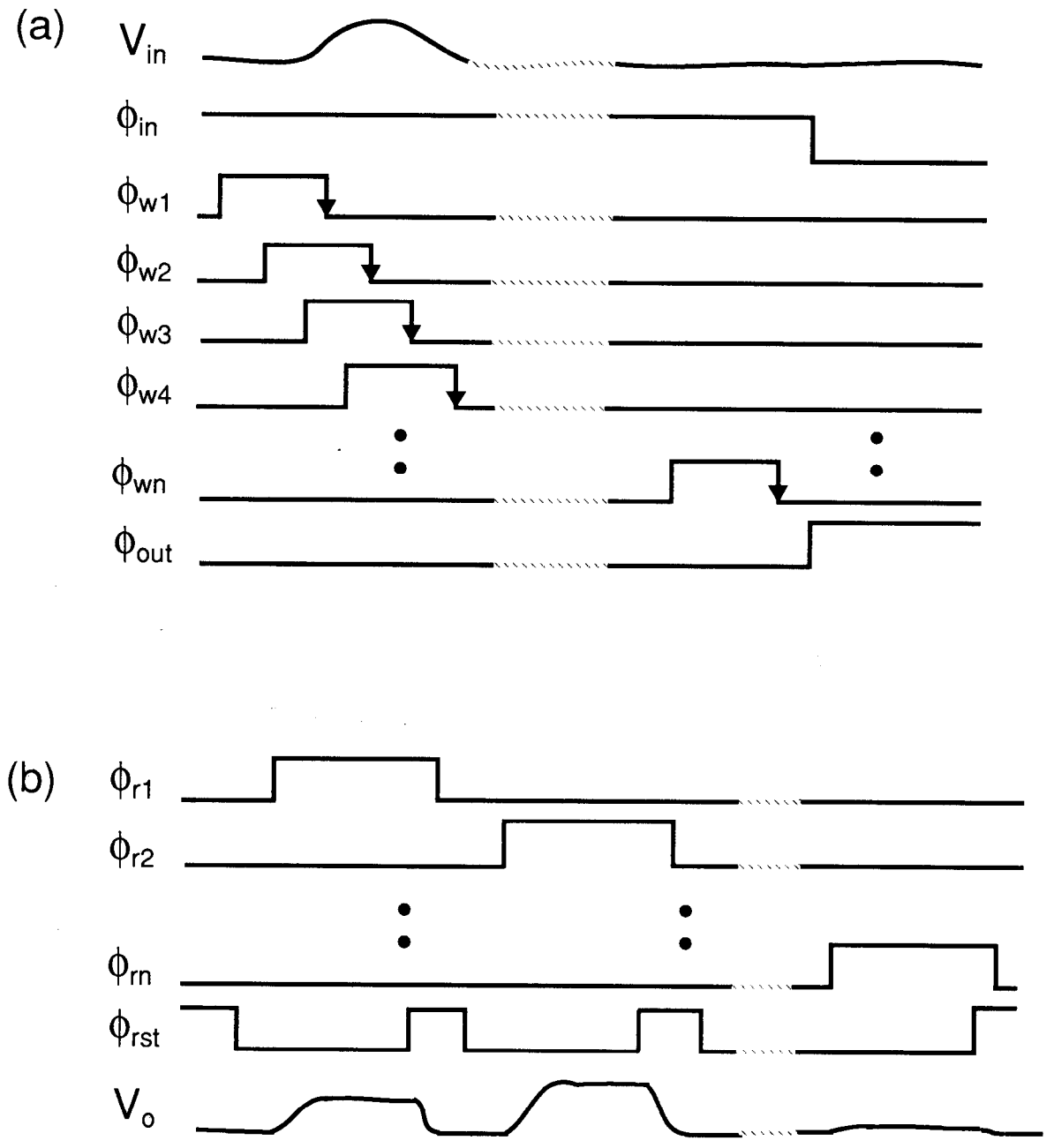

Figure 3: Haller and Wooley

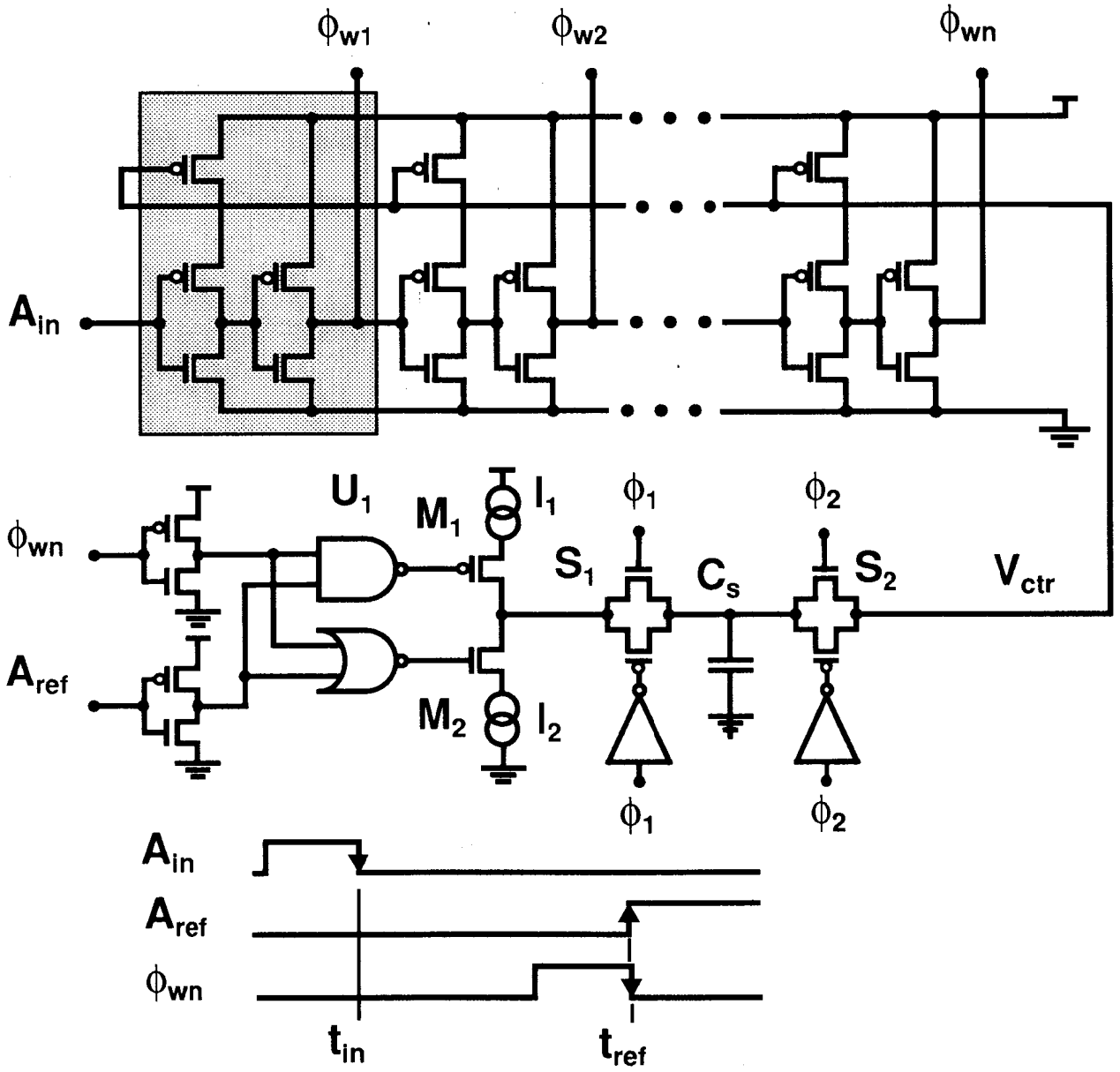

Figure 4: Haller and Wooley

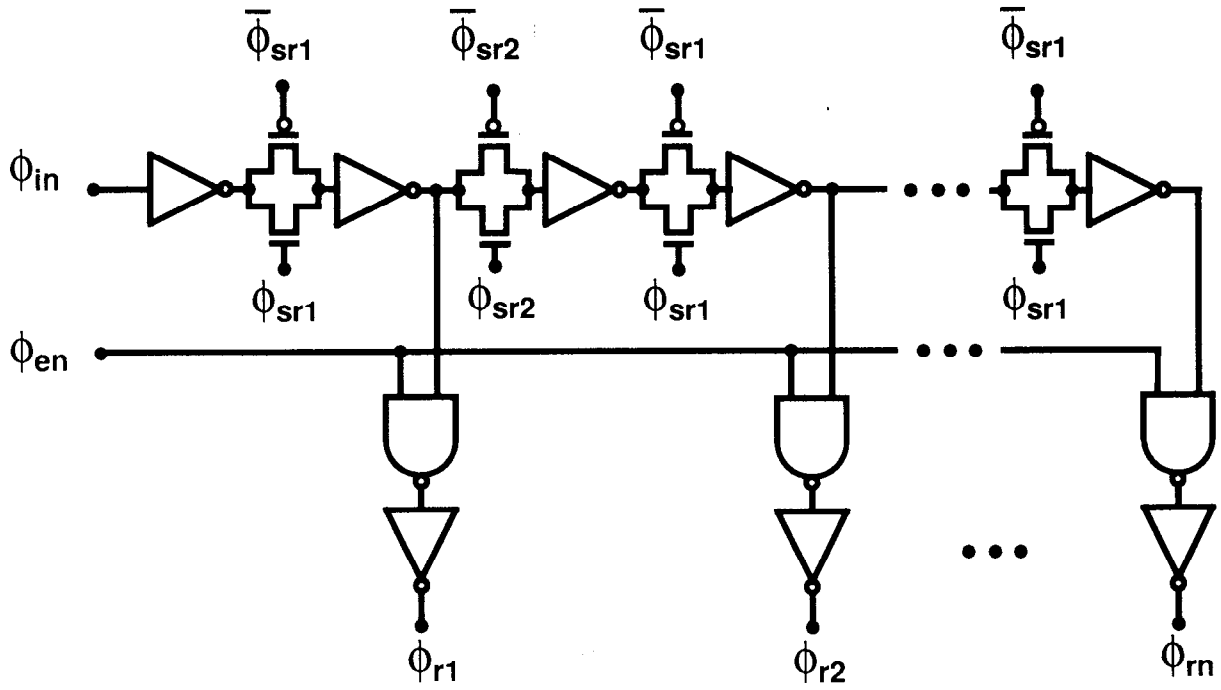

Figure 5: Haller and Wooley

Die Photo

Figure 6: Haller and Wooley

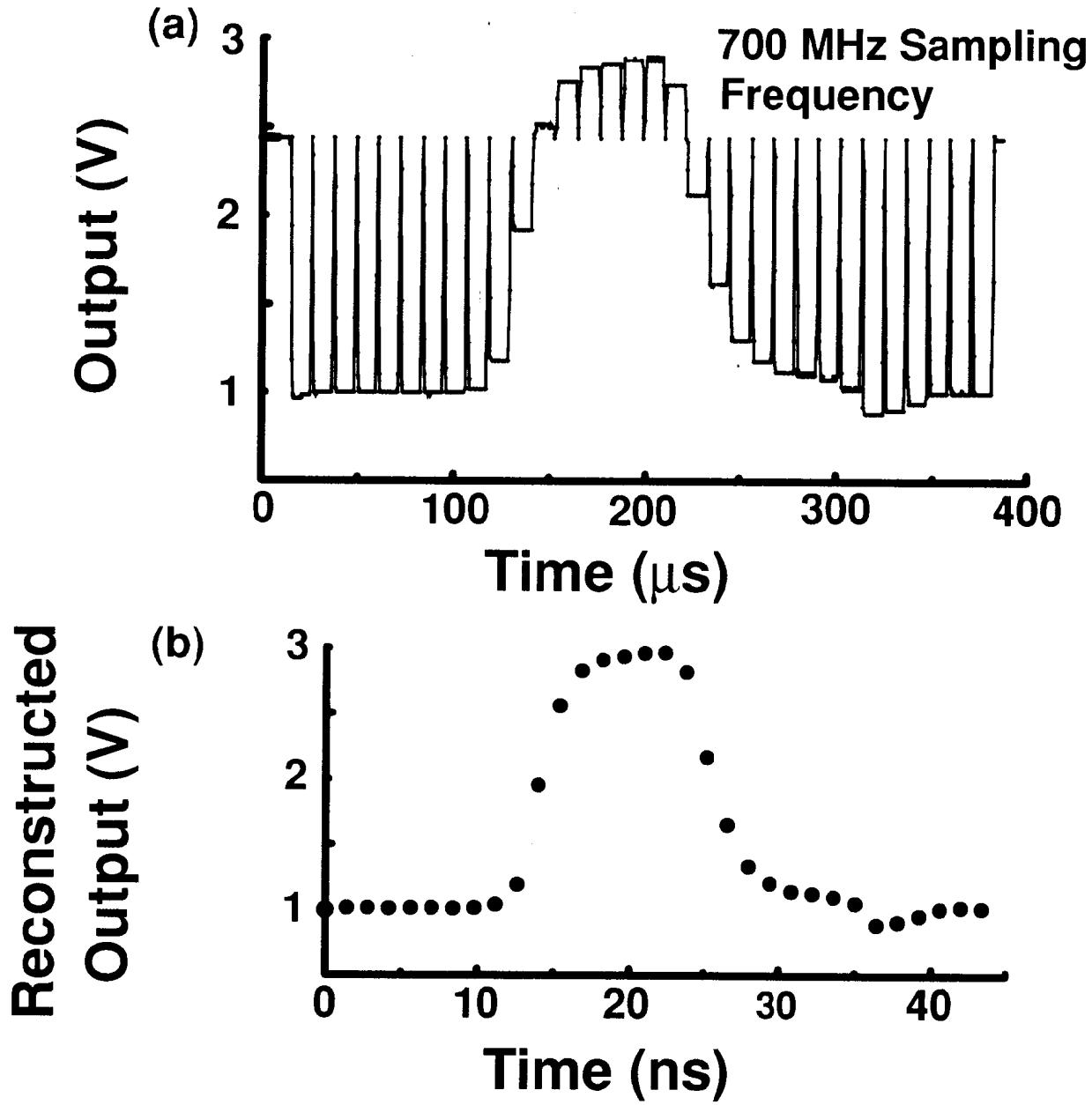

Figure 7: Haller and Wooley

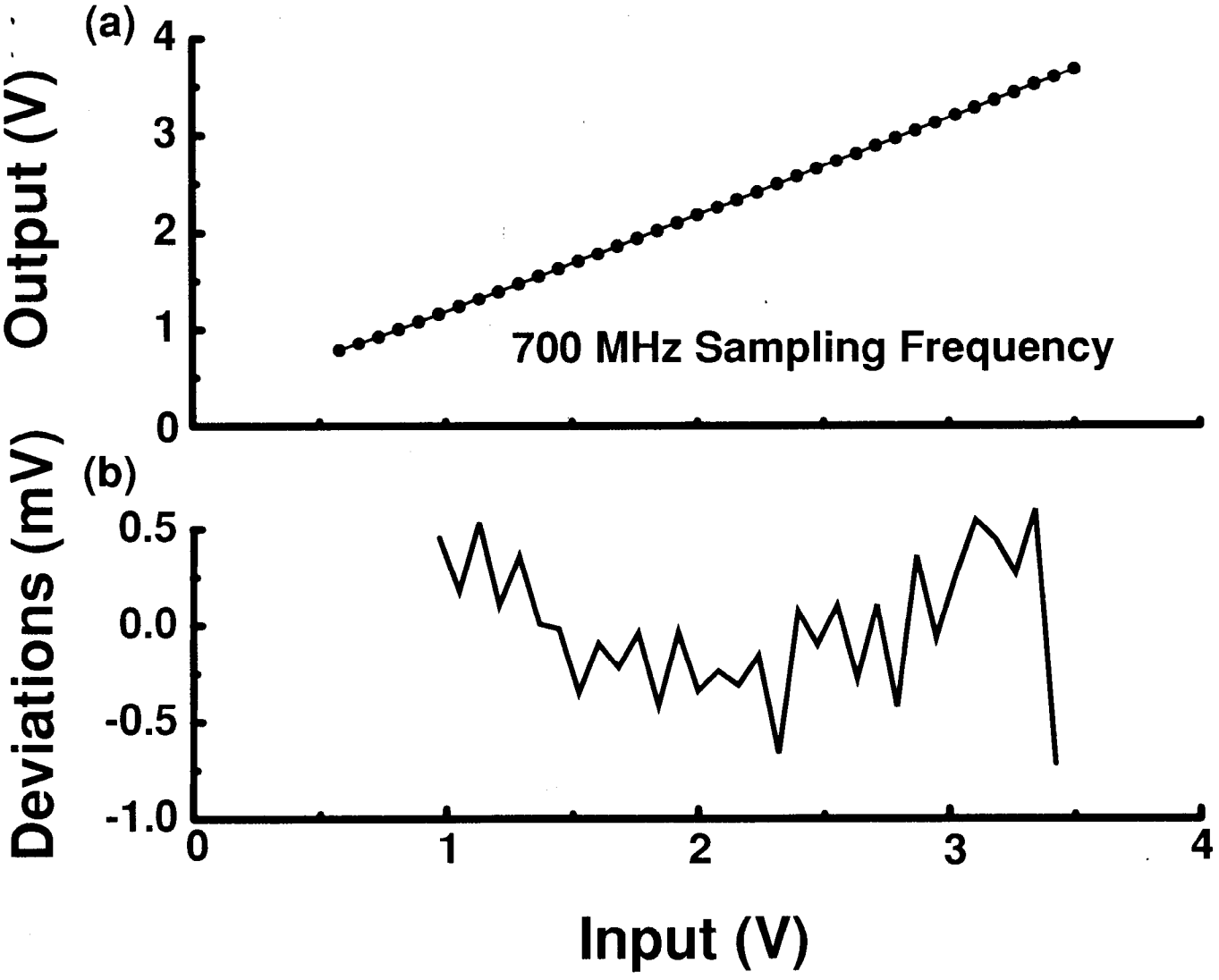

Figure 8: Haller and Wooley

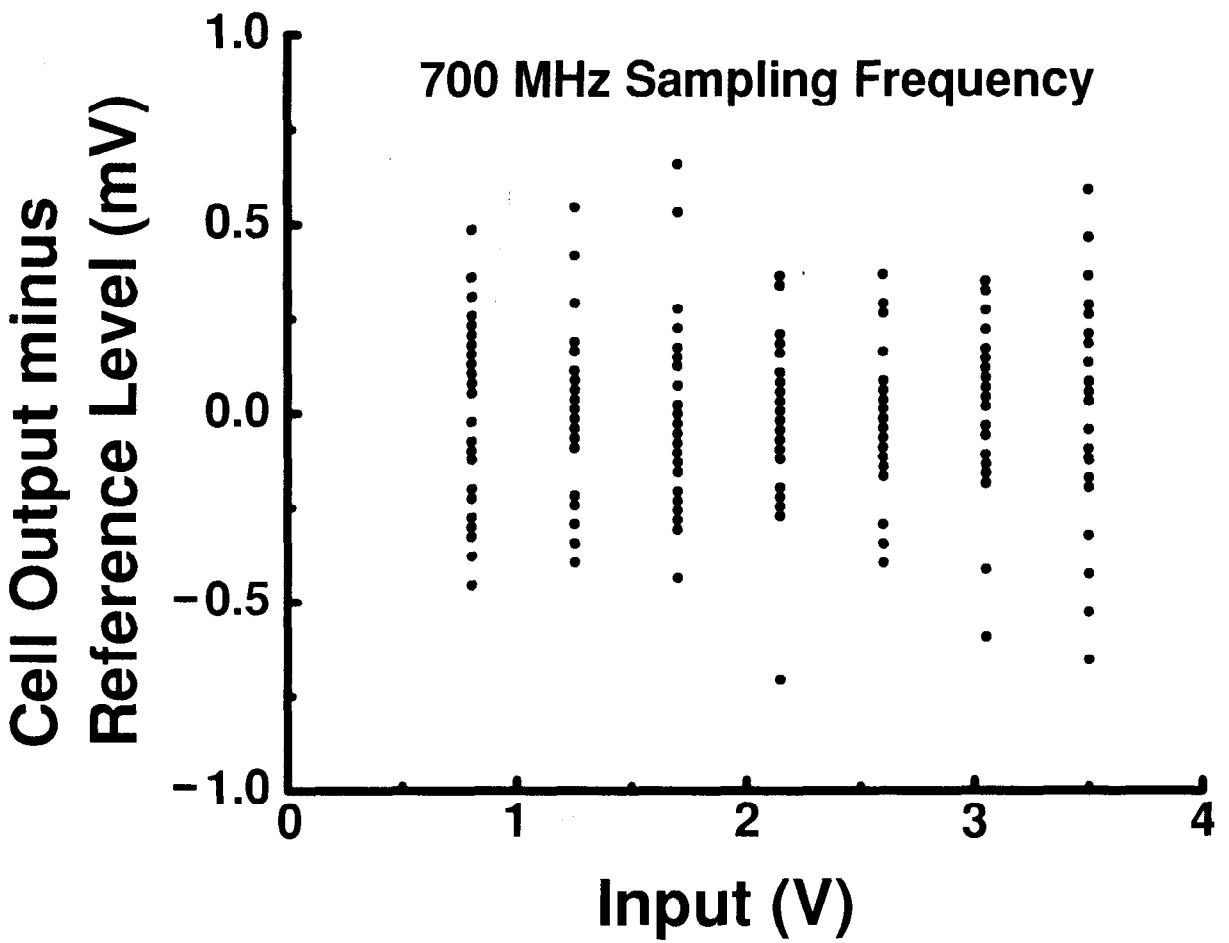

Figure 9: Haller and Wooley

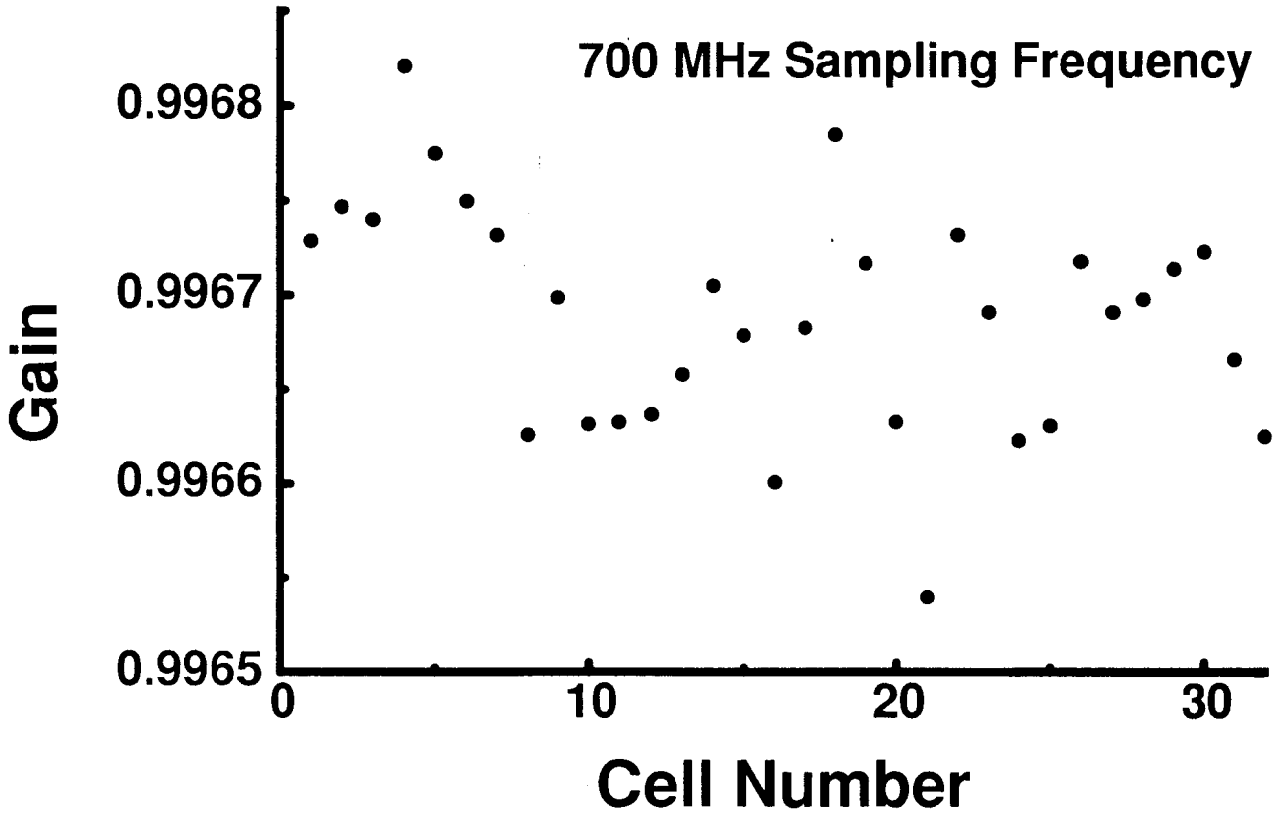

Figure 10: Haller and Wooley

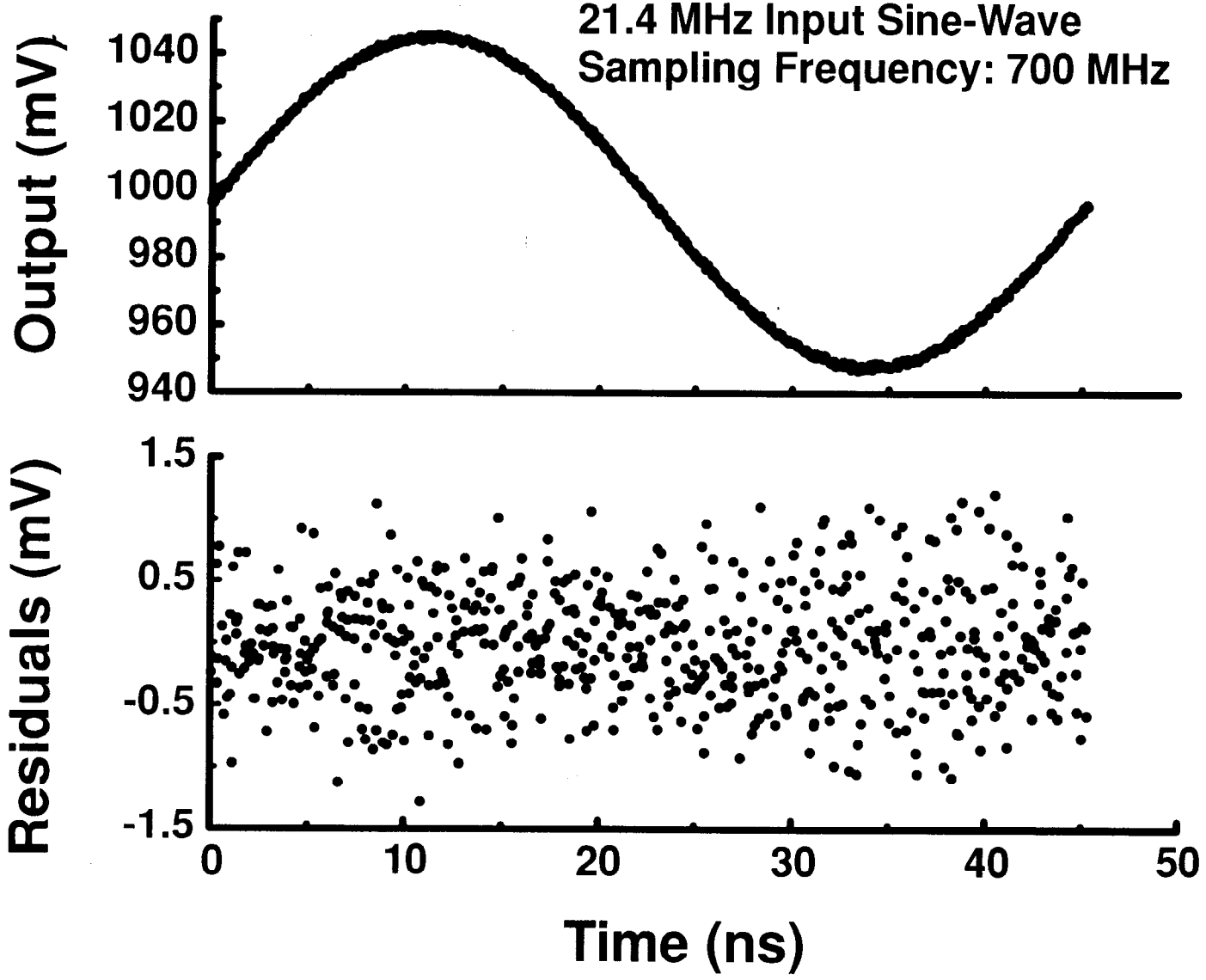

Figure 11: Haller and Wooley

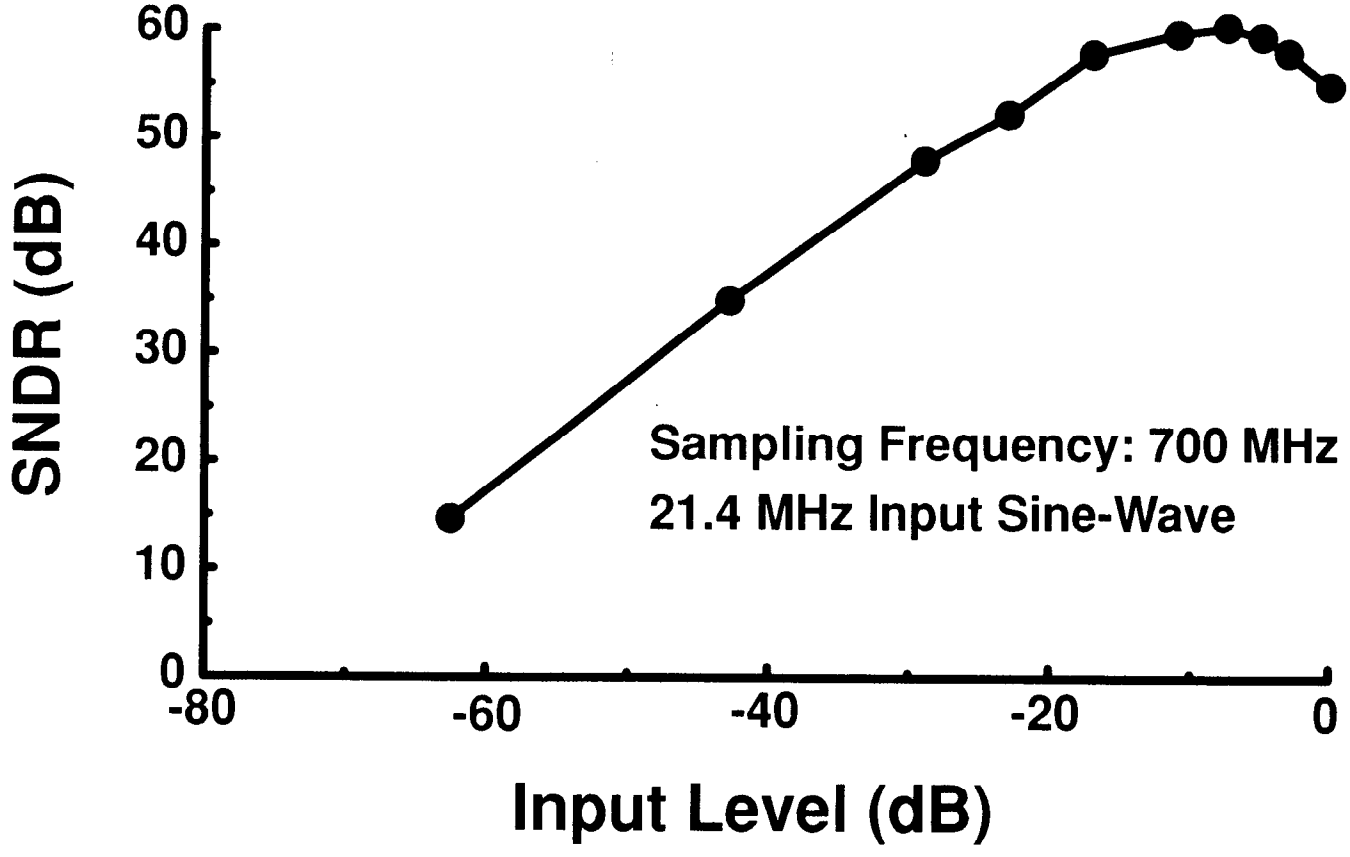

Figure 12: Haller and Wooley

Table 1

Analog Memory Performance Summary

Input time constant	< 1 ns
Minimum sampling frequency	200 MHz
Maximum sampling frequency	700 MHz
RMS cell-to-cell timing accuracy	25 ps
RMS noise floor	0.3 mV
Cell offset variation across full input range	
uncorrected	1.8 mV
reference level response subtracted	0.3 mV
Nonlinearity (for 2.5 V full scale)	0.03%
Cell gain nonuniformity (mean gain: 0.9967)	0.01%
Peak SNDR (21.4 MHz input sine wave, 700 MHz sampling rate)	60 dB
Dynamic range	74 dB
Power consumption of one channel (+5 V)	2 mW

Table 1: Haller and Wooley