SLAC–PUB–6386
November 1993
(E/I)

Design of a Trigger and Data Acquisition System for a Detector at PEP–II *

R. Becker-Szendy, D. Briggs, G. Haller, J. Hoeflich, and W. Innes
Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309

Abstract

This paper proposes a design of a trigger and data acquisition system for a detector at the PEP–II *B* Factory. The system is asynchronous, data-driven, and scalable. Design goals include orthogonal tracking and calorimetric triggers, minimal dead time, graceful degradation, high efficiency, and useful performance in the face of backgrounds so high as to overwhelm reconstruction. Also described are instrumentation of the Drift Chamber, based on 8-bit FADCs, and of the Calorimeter, based on a new custom integrated circuit, the Charge Amplifier with Range Encoding (CARE), and 10-bit ADCs. This design employs commercial embedded CPUs in VME and VXI crates.

I. Introduction

The physics program for the PEP–II *B* Factory, an asymmetric e^+e^- collider [1], requires a detector that emphasizes exclusive state reconstruction with the highest possible resolution and efficiency. The program requires luminosity of $3\times10^{33}/cm^2/s$. It targets *B* physics (especially CP violation), τ physics, and $2-\gamma$ physics.

The high luminosity of PEP–II requires high currents and 1746 bunches in each ring. The bunch-crossing period of 4.2 ns implies that for many purposes, the interactions appear to be continuous. The energy asymmetry boosts the final state in the lab frame for CP violation studies. Thus, the accelerator may present severe background rates in early operation. The trigger and data acquisition system must prove flexible. As discussed in ongoing workshops [2,3], *B* Factory detector subsystems include a Silicon Vertex Detector, Drift Chamber, Particle ID, projective tower CsI Calorimeter, and Instrumented Flux Return; but no Time-of-Flight subsystem. The detector must quickly achieve robust, stable, factory-like performance.

The trigger and data acquisition system should not limit the experiment or accelerator operations by dead time or susceptibility to background. During conditions of intense background rates, system performance should degrade gracefully, still providing useful diagnostic information about detector performance and background sources. Some of the design choices presented serve only as examples for cost estimates, reflecting currently available commercial technology.

II. Implementation Overview

This design departs from existing systems in e^+e^- colliders in several ways. It also differs from designs for other proposed *B* Factories [4]. Separate pipelines carry the early trigger information and data. Trigger decisions and data transfers occur asynchronously. The design requires no dedicated event builder hardware. The system's capacity scales largely with the number of commercial data links and processors installed.

The system comprises three levels; see Fig. 1. Level 1 digitizes and buffers signals, and forms two streams of trigger decisions, based independently on tracking and calorimetry information. Level 2 uses complete detector information in VME processors to verify and refine the trigger decisions of Level 1. Level 3, discussed elsewhere [5], performs full reconstruction on-line, using a farm of workstations.

A. Level 1 Overview

Level 1 comprises front-end digitizer modules and pattern recognition in software. In Level 1, two orthogonal streams of trigger decisions provide independent efficiencies in the detector acceptance for most physics channels. The logical OR of the two streams provides redundancy in the trigger hardware, and control of trigger systematics for physics analysis. The calorimeter stream depends only on information from the CsI calorimeter. The tracking stream depends on the Drift Chamber and possibly the Silicon Vertex Detector. Each stream originates in its front-end digitizer modules, based on one or a few neighboring channels, and flows to a processor group that recognizes tracks (Curvature Engine) or calorimetric patterns (Pattern Engine).

A subsequent processor (Monotonochron) collates the two decision streams (logical OR), merging events that overlap in time. It forms a time window for each event, covering the longest detector resolving time in the system; see Fig. 2.

All subsystems digitize continuously at appropriate submultiples of the bunch crossing rate into the sequential port of Video Random Access Memory (VRAM). New data overwrites old data. The Monotonochron prompts all subsystems, including the nontriggering subsystems, to pass the data in the time window to Level 2. The time window indicates a range of addresses in the random access port of VRAM. Commercially available VRAM readily provides at least 6 ms of buffer depth for the fastest subsystem (Drift Chamber).

The digitizer modules of the Drift Chamber and Calorimeter subsystems require DSP units. These extract signal amplitude and time-of-arrival from sampled waveforms stored in VRAM, for subsequent Level 2 processing.

The Monotonochron can throttle Level 1. In heavy backgrounds or insufficient Level 2 throughput, the Monotonochron can disable the Curvature Engine or the Pattern Engine. Through them, it also can disable the trigger logic of the Drift Chamber and Calorimeter front-end modules.

*Work supported by Department of Energy contract DE–AC03–76SF00515.

Presented at the IEEE 1993 Nuclear Science Symposium and Medical Imaging Conference
San Francisco, CA, October 31–November 6, 1993

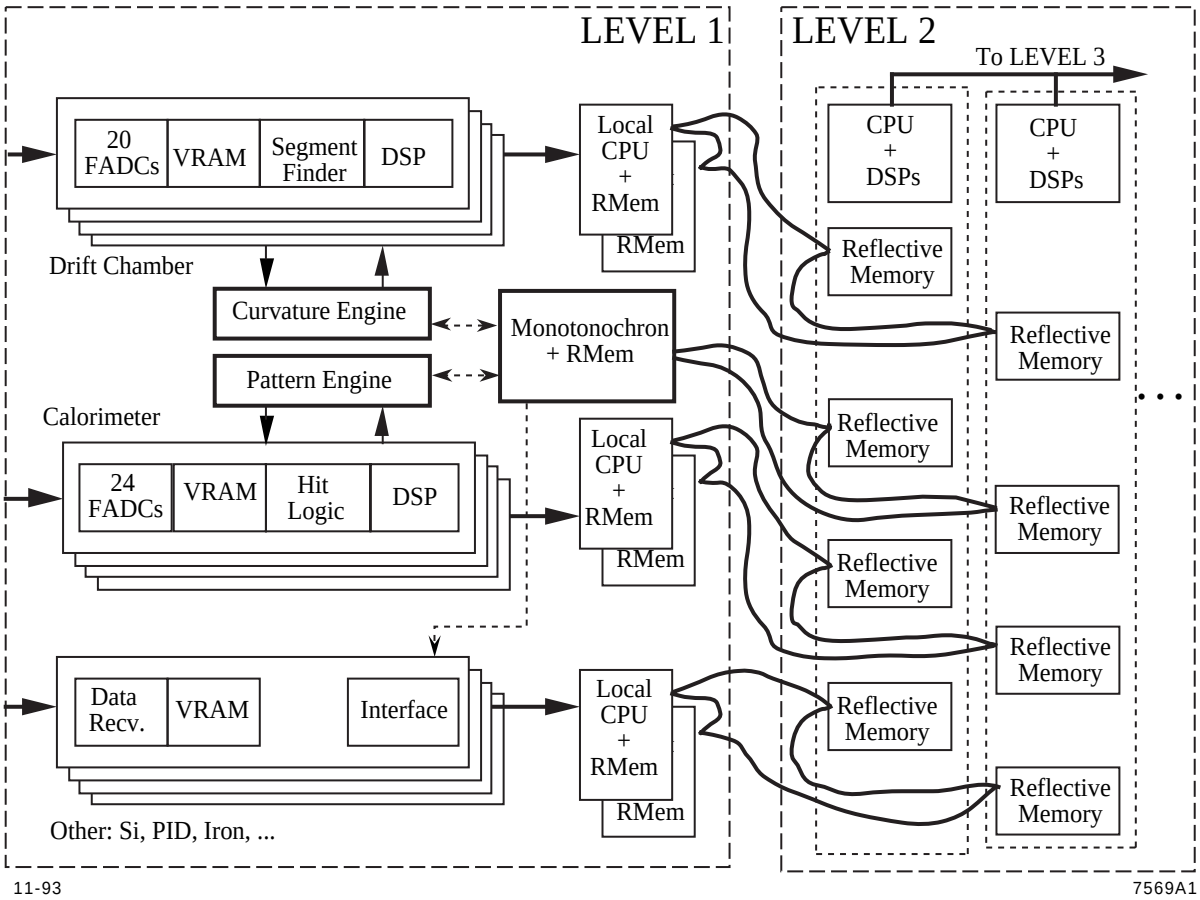

Fig. 1. System overview.

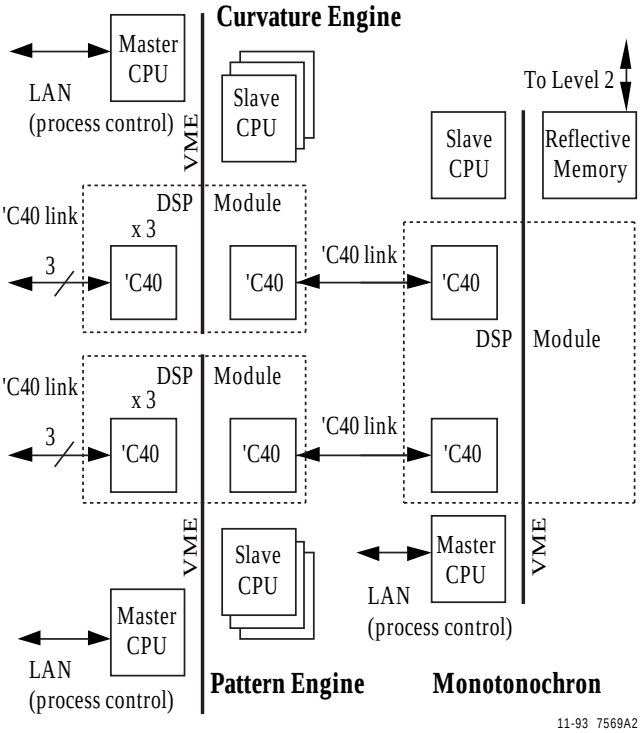

Fig. 2. Level 1 processors.

B. Level 1 Tracking Trigger

The Drift Chamber uses a small-cell stereo and axial design, organized as ten superlayers of four layers each. The tracking trigger criterion requires at least two simultaneous tracks emerging from near the interaction point (IP). One track must reach the outer radius of the drift chamber (>120 MeV/c), and another must reach at least half-way through (>75 MeV/c). The front-end digitizing modules send messages describing track segments to the Curvature Engine, which then assembles the tracks from many such messages.

Each D-size VXI Drift Chamber front-end module serves a block of 20 channels in a superlayer; see Fig. 3. Every two to four bunch crossings (60 to 120 MHz), an 8-bit FADC digitizes a signal from a preamplifier mounted on the chamber, and VRAM captures the data. Studies of tracking resolution in a Drift Chamber prototype will determine the sampling rate. The front-end module also contains logic for finding track segments, and a DSP unit for local data reduction. The module connects to VME, its neighboring modules, and the Curvature Engine.

The Segment Finder logic exploits the superlayer structure of the Drift Chamber. A discriminator on each channel informs the Segment Finder of a hit on a Drift Chamber wire. The Segment Finder uses all 20 hit signals on its own module

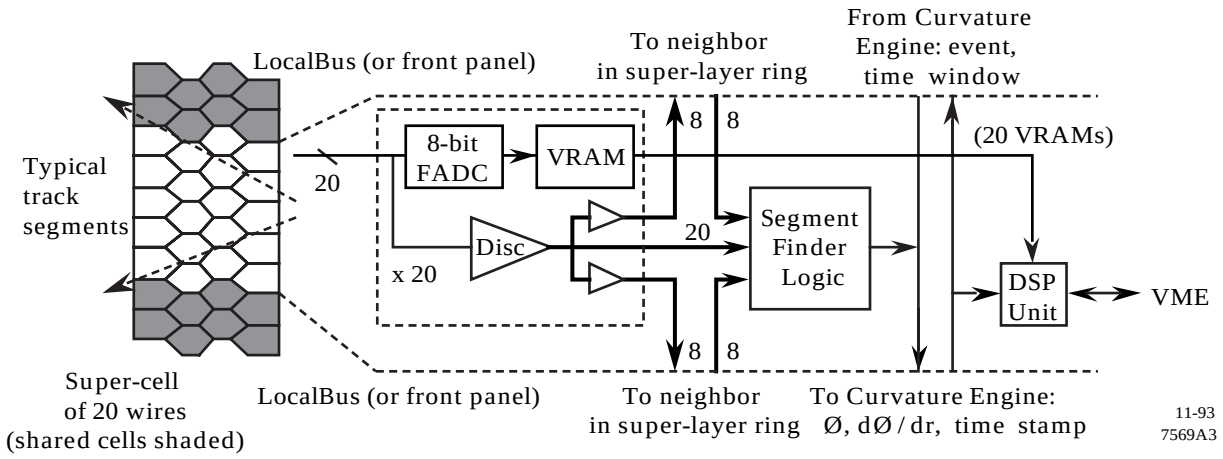

Fig. 3. Block diagram of Drift Chamber front-end module.

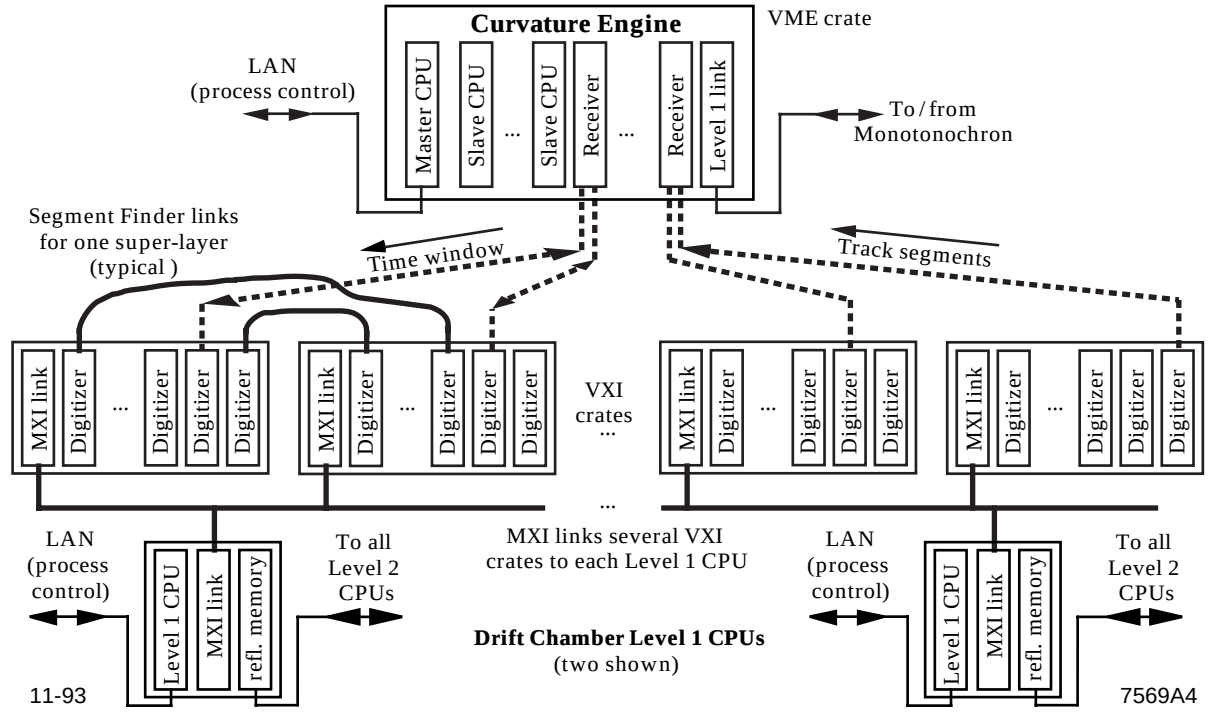

Fig. 4. Drift Chamber Level 1 crates and cabling.

and 16 from neighboring channels in its superlayer ring (8 each from the left and right). Its output is a coarse resolution (about 100 ns) message to the Curvature Engine with the time, location, and slope of each track segment found. The Curvature Engine builds tracks spanning the entire Drift Chamber from these track segment messages, and tests them against the tracking trigger criterion. The Segment Finder suppresses synchrotron radiation backgrounds directly.

The Segment Finder logic depends on a ring of nearest–neighbor connections among the front-end modules supporting each superlayer. Each module also needs a bidirectional link with the Curvature Engine. VXI's LocalBus provides both paths for nearest-neighbors in the same VXI crate. A module uses its front-panel connectors for either path to connect to a nearest-neighbor module in another crate, as shown in Fig. 4.

This scheme allows crates to serve multiple superlayers, or superlayers to span crates, but reduces the cable plant. Initialization software verifies the routing.

When the Drift Chamber suffers high occupancy of low-momentum tracks, the Curvature Engine can suppress transmission of segment messages by superlayer. Finding a candidate track in the outer superlayers, it permits segment messages from inner superlayers in a time window, and

continues its search inward. In response to a decision in the Monotonochron, the Curvature Engine broadcasts a time window message to all the Drift Chamber front-end modules, identifying the data to reduce for Level 2.

C. Level 1 Calorimetric Trigger

In the CsI towers, a criterion near half the energy deposited by a minimum-ionizing particle, i.e., about 0.5×170 MeV, serves to discriminate against background from the beams. The Pattern Engine, again in VME processors, identifies Calorimeter triggers based on the topology and multiplicity of clusters over threshold.

The Calorimeter front-end modules are similar to those of the Drift Chamber. Each D-size VXI module digitizes the waveforms of 24 channels, stores the data in VRAM, forms local trigger decisions, and reduces the data in a DSP unit. The module has a bidirectional link to the Pattern Engine through LocalBus and front-panel connectors.

A custom integrated circuit under development at SLAC, the Charge Amplifier with Range Encoding (CARE), instruments each photodiode of the CsI Calorimeter [6]. Figure 5 shows a simplified block diagram. A charge preamplifier and shaping circuit condition the detector signal. Parallel gain stages G_1 through G_n further amplify the signal and connect to a set of comparators. The gain values approximate an exponential series, A^1 through A^n.

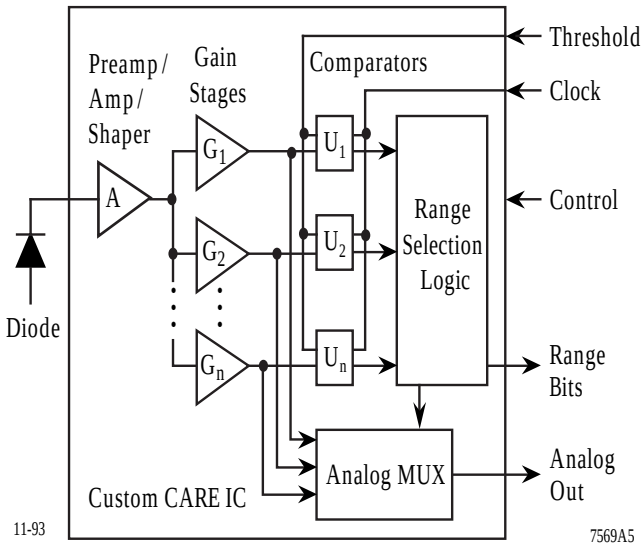

Fig. 5. Simplified block diagram of the Charge Amplifier with Range Encoding (CARE) custom integrated circuit for the CsI (Tl) calorimeter.

Range-selection logic observes the outputs of the comparators, determines the gain stage with the highest nonsaturated output level, and controls an analog multiplexer, which chooses the selected gain stage for the analog output of the chip. This analog level represents the mantissa of a floating point number, and the range bits indicate its exponent. The CARE chip and an appropriate commercial ADC comprise a charge-sensitive preamplifier, shaper, and floating-point ADC. Foster et al. [7] proposed the principle of floating-point digitization for high-energy physics instrumentation at the SSC.

The CARE chip lies on or near the CsI tower and its photodiode, transmitting its analog and digital outputs to a Calorimeter front-end module. Each channel continuously digitizes its analog level to about ten bits of mantissa, writing the mantissa and the exponent into VRAM, at up to 10 MHz.

DSP techniques on the stored waveform can improve the noise and dynamic range of the measurement. The product of the dynamic range of the mantissa (e.g., 2^{10}) times the highest gain (e.g., 2^8) limits the total dynamic range of the device per digitization. The combined impulse response function of the CsI, photodiode, preamplifier, and shaper has rise and fall times much longer than the time between samples. A given energy deposition yields a waveform of many (>10) floating point samples, and provides more information than a single sample at the peak.

Calorimeter front-end modules send messages to the Pattern Engine describing the time, location, and energy of each hit over threshold. The Pattern Engine assembles messages from the entire Calorimeter, forming clusters of hits in time and space. It finds events that match trigger criteria, based on multiplicity and topology. In response to a decision in the Monotonochron, the Pattern Engine broadcasts a time window message to all the Calorimeter front-end modules, identifying the data to reduce for Level 2.

D. Other Level 1 Data Acquisition

The Particle ID and Instrumented Flux Return subsystems employ identical front-end modules. Data-driven logic on the detector generates a message for each hit, and operates without external triggers. These messages contain pulse height, time, and channel number information. Several parallel buses serve each subsystem's digitizers. The front-end module receives the messages and stores them in VRAM, with an address equivalent to a rough time stamp.

The Silicon Vertex Detector will probably use a similar data-driven architecture. Detailed design will determine whether the Silicon Vertex Detector participates in the tracking trigger.

III. Linking Level 1 and Level 2

The front-end modules for all subsystems reside in VXI crates. MXI interface modules and cables link several front–end VXI crates together into groups. Each group has an MXI interface in VME to a CPU and to a commercial reflective memory module. The reflective memory modules of Level 1 link to those of Level 2 as required. Thus, data move from Level 1 to Level 2 through shared memory. Internally, Level 1 relies on message-passing, using the "commports" of Texas Instruments TMS320C40 DSPs or equivalent.

IV. LEVEL 2

Four groups of processors (CPU and/or DSP modules) in two VME crates examine events in detail, using data from the whole detector as required. Upon receipt of a trigger message from the Monotonochron, the next available Level 2 CPU reads data from Level 1 in order of relevance (the relevance depends on the content of the trigger message). For instance, it rejects about 1 kHz of cosmic ray events that deposit threshold energy in the Calorimeter, but have tracks in the Drift Chamber or the Instrumented Flux Return that miss the IP. Level 2 can reject most beam-gas events that pass Level 1, because it resorts to the full tracking resolution, including the Silicon Vertex Detector.

V. RATES

At design luminosity on the $\Upsilon(4S)$, physics rates surpass those of previous e^+e^- colliders; that is the point of a "factory". Studies of background sources at the machine-detector interface have played an important role in the design of the interaction region [8]. Iterations in the design have steadily improved the expected background rates. However, these rates serve only as asymptotes, approached after perhaps a year of operation. Table I presents physics rates and asymptotic background rates that pass the Level 1 trigger criteria, neglecting the Silicon Vertex Detector as a participant. Some background rates are scaled up from measurements by similar detectors at PEP–I.

Table I. Physics and background rates

Source	Tracking	Calorimetric	Both	Comments
Cosmics	40*	1300		
Accelerator backgrounds (asymptotic)				
Hadronic	200 to 500*			Scaled from PEP–I
Electromagnetic	0	400		60 MeV threshold
		30		80 MeV threshold
		7		100 MeV threshold
2-γ background			50	
Bhabha			10	Prescaled from 90 Hz
1/ 2 Bhabha	0	0	0	1 kHz, single tracks, backward
$e^+e^-\gamma$			50	
$\mu^+\mu^-$, $\tau^+\tau^-$			5	
$\Upsilon(4S)$			12	
$e^+e^- \rightarrow 2\gamma$			3	

* Neglecting the Silicon Vertex Detector.

VI. SCALABILITY

The design permits additional hardware data links between the Drift Chamber front-end modules and the Curvature Engine, and between the Calorimeter front-end modules and the Pattern Engine. Increased processing power in the Curvature and Pattern Engines, the Monotonochron, and Level 2 requires only more VME processors. More reflective memory modules and their links can provide additional throughput from Level 1 to Level 2. These elements are commercially available. Their price/performance ratio improves every year.

Initial backgrounds will no doubt prove worse than the asymptotic rates listed in Table I. Scaling these rates up uniformly, the Drift Chamber suffers first. At 30 times the asymptotic rates, the occupancy in the inner layers of the Drift Chamber becomes about 10%, and event reconstruction fails. Above this rate, then, appreciable dead time is permissible.

Initial cost estimates reflect the system as described, roughly scaled for 30 times the asymptotic rates. Level 1 can emit up to 10 kHz of trigger decisions, and Level 2 can emit up to 1 kHz, keeping dead time less than 10%. Detailed discrete-event behavioral simulations (MODSIM II), using physics and background Monte Carlo data, will guide more detailed design.

VII. CONCLUSIONS

The design presented meets the physics goals for a detector at PEP–II. It should prove robust and flexible under possibly severe background conditions in the initial operation of an asymmetric e^+e^- collider. This system is pipelined, asynchronous, and scalable. It requires few custom modules, relying heavily on commercially available parts. Further details of the design depend on behavioral simulations of the system.

VIII. REFERENCES

[1] "PEP–II Asymmetric B Factory: Conceptual Design Report," SLAC-418, 1993.

[2] "Status Report on the Design of a Detector for the Study of CP Violation at PEP–II at SLAC," SLAC–419, 1993.

[3] "*B* Factories: The State of the Art in Accelerators, Detectors, and Physics," SLAC–400, 1992; and *Workshop on Physics and Detector Issues for a High Luminosity Asymmetric B Factory at SLAC*, SLAC–373, 1991.

[4] CLEO Collaboration, "Detector for a B Factory," CLNS–91–1047–Rev, 1993; and *Int. Workshop on B Factories: Accelerators and Experiments*, KEK-Proceedings–93–7, 1992.

[5] Reference [2], Chapter 8 "Computing".

[6] G. Haller, to be published.

[7] R. J. Yarema et al., "A Fast, Wide Range Charge Integrator and Encoder ASIC for Photomultiplier Tubes," *IEEE Trans. Nucl. Sci.*, vol. 40, No. 4, p. 750, 1993.

[8] H. DeStaebler et al., "Machine–Induced Backgrounds at the SLAC *B* Factory," in Ref. [3], pp. 17–54, 1992.