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Bunch-by-Bunch Feedback for PEP II*

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ABSTRACT

The proposed PEP II B factory at SLAC requires a feedback to damp out longitudinal synchrotron oscillations. A time domain, downsampled, bunch-by-bunch feedback system in which each bunch is treated as an oscillator being driven by disturbances from other bunches is presented as we review the evolution of the system design. Results from a synchrotron oscillation damping experiment conducted at the SLAC/SSRL/SPEAR ring are also presented in this paper.

1. INTRODUCTION

The feedback system design incorporates a phase detector to provide a measure of the bunch phase, digital signal processing to compute an error correction signal and a kicker system to correct the energy of the bunches. A downsampling scheme has been implemented to reduce the size of the hardware.

Figure 1 is a conceptual diagram of such a system. The phase of each bunch is detected and a correction kick for each bunch is computed and applied by a kicker. The downsampler allows each digital signal processor (DSP) to handle more bunches and, consequently, reduces the size of the system. The hold buffer holds the last kick value computed for each bunch.

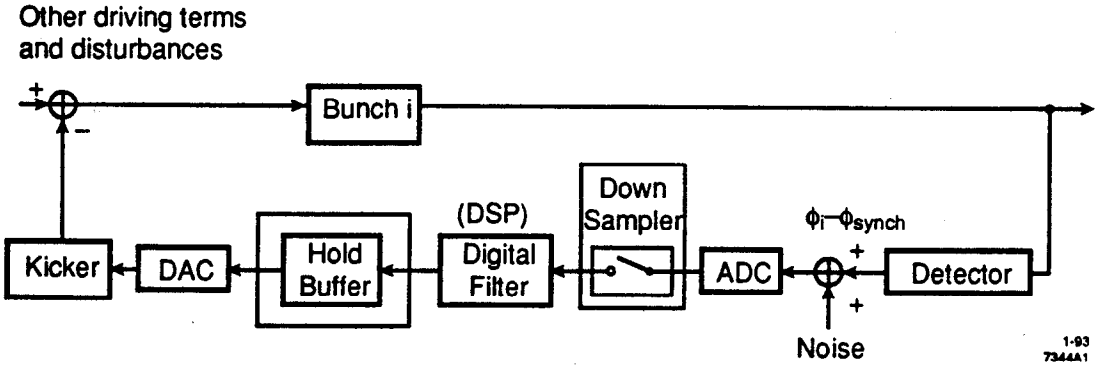

Fig. 1 Conceptual bunch-by-bunch, downsampled feedback system.

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2. SYSTEM REQUIREMENTS

2.1 PEP II Specifications:

- 476 MHz RF frequency
- Every other RF bucket populated
- 4.2 ns inter-bunch period
- Up to 1746 bunches without ion clearing gap
- 1658 populated bunches with gap
- 7.3 μs revolution period
- 140 μs synchrotron period.

2.2 Feedback requirements:

- Detect the bunches' phase oscillation
- Provide a 90° phase shift at the oscillation frequency
- Suppress DC components in the error signal
- Provide a processing gain useful with a noisy front-end
- Provide +/- 15° linear phase range correction
- Provide 0.5°, or better, measurement resolution
- Implement saturated limiting on large oscillations
- Output power 2.5 kW at 1.071 GHz.

2.3 Implementation of the feedback:

The various options to implement an accelerator feedback are discussed in detail in Refs. 1 and 2. Analog and digital approaches are compared, and the approach chosen for the longitudinal feedback systems in PEP II is a digital signal processing technique.

3. DIGITAL SIGNAL PROCESSORS

The commercial activity in DSPs in recent years has lead to a wide choice of devices for audio and speech applications. These devices are also well suited to synchrotron frequencies in the range of 7-10 kHZ. When used to implement an accelerator feedback system, they offer the additional advantage that the filter can be configured via software to match the particular operating characteristics of the machine. Figure 2 is a block diagram of the original PEP II longitudinal feedback system proposal using DSP devices to implement a finite impulse response (FIR) filter

Such a system to control the large number of bunches in the PEP II rings requires many DSPs. It was recommended by a review board that the number of DSPs be reexamined.

4. DOWNSAMPLING

References 3 and 4 present the downsampling approach in detail. Our longitudinal feedback system for PEP II takes advantage of the fact that the revolution frequency at which we sample the phase oscillation is greater than the synchrotron frequency. This inherent oversampling allows use of the downsampling,

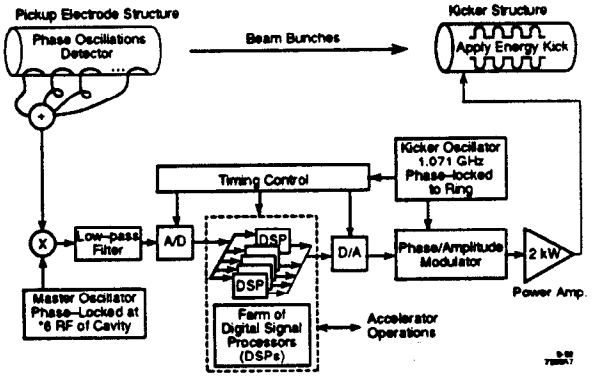

Fig. 2 Longitudinal feedback system without downsampler.

in which information about a particular bunch oscillation is used only every n revolutions, and a new correction signal is updated every n revolutions. This approach allows the processing system to operate closer to the Nyquist limit and reduces the number of multiply accumulate operations in the filter by a factor of $1/n^2$.

The downsampled longitudinal feedback scheme was examined and simulated. The results suggest that it could control the coupled bunch oscillation with dynamics similar to a 20-tap filter. The frequency response of the 20-tap and 5-tap filters are shown in Fig. 3.

A downsampling factor of four was recommended for PEP II. Figure 4 shows that kicker signals applied to the bunch are now a coarser approximation of the ideal feedback kick.

The downsampling reduces the size of the DSP farm considerably, and the bus bandwidth required to move data within the system is reduced by a factor n. However the downsampler and hold buffer need to be implemented with high speed electronic circuitry running at the bunch frequency.

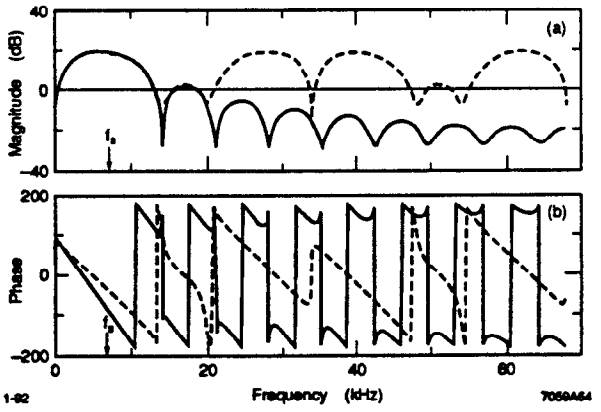

Fig. 3 Frequency response of "n=1" (dashed line) and "n=4."

Figure 5 shows a conceptual block diagram of such a processing farm.

In the spirit of the PEP II technical practice, the downsampled processing scheme was reviewed, approved, and a detailed study of the system architecture recommended.

5. SYSTEM ARCHITECTURE

Multi-processor systems have many applications and are typically based on

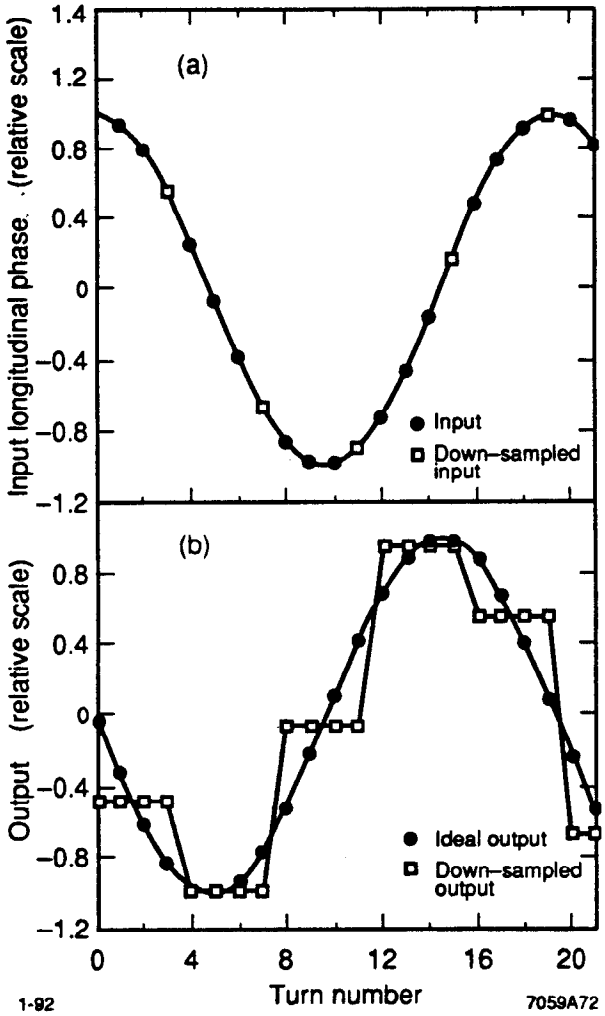

Fig. 4 Response of the downsampled filter with hold buffer. In (a), the squares are sampled values of the oscillation. (b) shows ideal and downsampled outputs to a kicker.

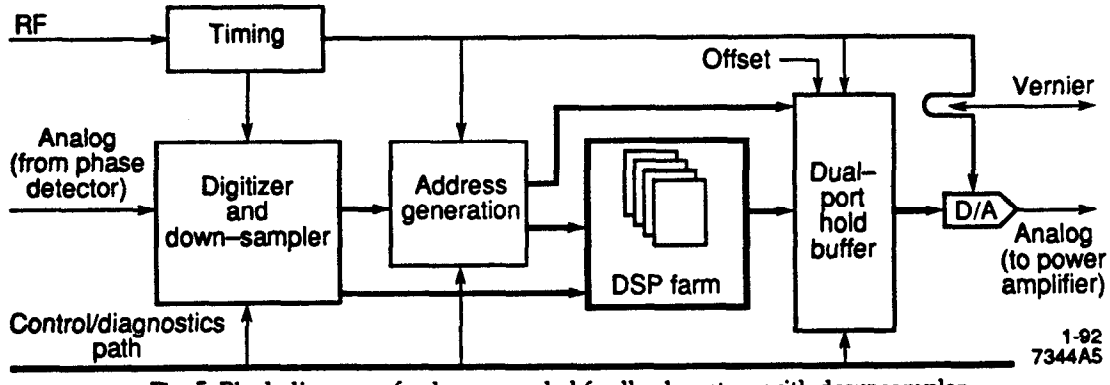

Fig. 5 Block diagram of a downsampled feedback system with downsampler.

standard parallel buses such as VME, Multibus II or a new comer in the field, Futurebus+. The longitudinal feedback for PEP II being a multi-processor system, we chose to use a bus with a well defined protocol to distribute the data. The VMEbus was selected because of its architecture, the availability of assembled chassis with power, cooling and various sizes of backplanes. Interface chip-sets are available to help the designer adhere to the protocol and several side buses, such as VMX, VMS and VSB are specified.

The VMEbus is a computer architecture with 32 bit data and 24 bit wide address buses. It can also be used as a 64-bit-wide multiplexed address and data bus under revision D. There is a proliferation of commercially available VME based board products, many of them with DSPs. However, most of the DSP boards commercially available have floating point devices and large on-board memory. They are designed to accept large blocks of data on which they effect some complicated, slow computation. These subsystems are typically used for speech recognition, image reconstruction and the like. They are not well suited to an accelerator feedback application which is I/O bound and has a short filter code which requires little memory. The design of our DSP boards will have four DSP integrated circuits per 6 U VME board. Since the ADC and DAC are eight bits wide, the data from four bunches and four bunch kicks will each form a 32 bit word. The 32 bit wide VMEbus protocol was recommended. This permits us to address the DSP boards with each transfer and perform a read-modify-write cycle rather than doing block transfers which require duplication of addressing circuitry on the downsampler-hold buffer and the DSP boards. It also guarantees data integrity.

The longitudinal feedback for PEP II presents a particular challenge to meeting the data distribution bandwidth. Even with downsampling by four, the amount of data sent from the downsampler to the DSPs and from the DSPs to the hold buffer is overwhelming. The data to and from a DSP is one byte wide. The aggregate data rate to maintain is therefore one byte every 16.8 ns, or 119 MBytes per second. Of course, the VMEbus cannot sustain such a data rate. Faced with this restriction we are compelled to distribute the data over two or more VMEbuses.

A review was conducted to critique the proposed VME based architecture. Very strong warnings were expressed, one to avoid pushing the bus technology and the other to expand the control interface definition.

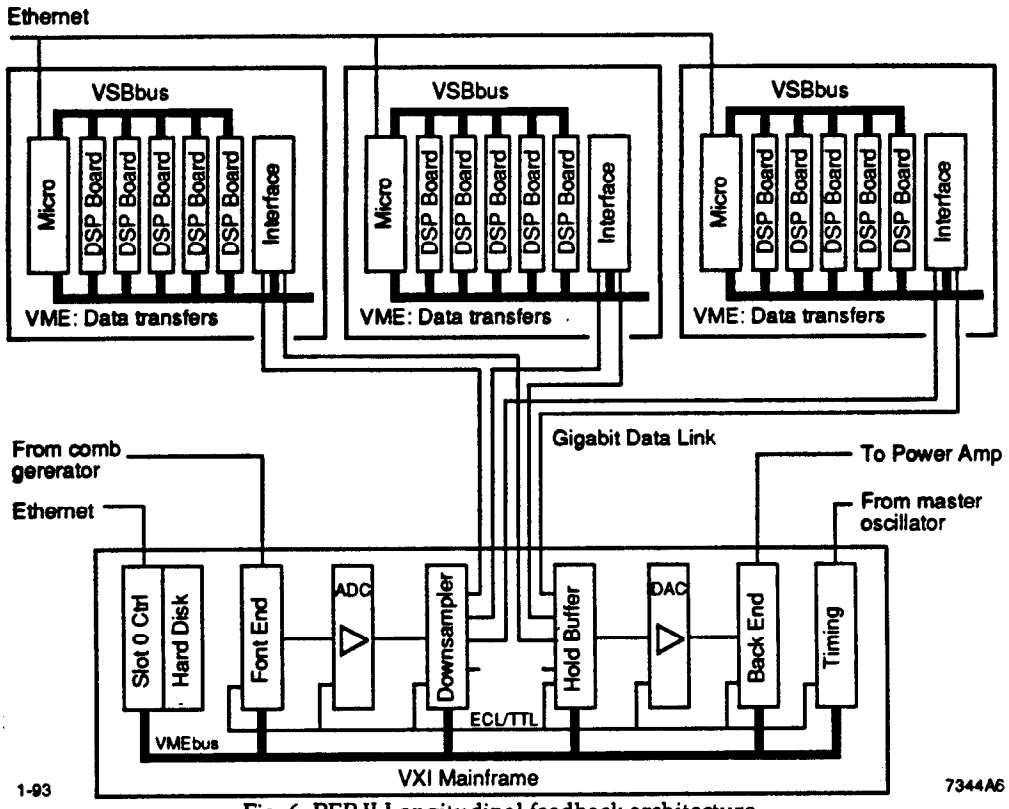

Fig. 6 PEP II Longitudinal feedback architecture.

Another facet of the architecture has to do with the downloading of the code and coefficients to the DSPs, and the system control and monitoring. These functions can be performed at the low data rate of a few kHz. The VMEbus can be used for downloading as long as this is done prior to operating the system, since the data transfers will consume the bus bandwidth during running. Another path had to be found for the control and monitoring functions. We selected the VME subsystem bus, VSBbus, as the control, monitoring and downloading path. The VSBbus has a 32-bit multiplexed address and data bus, read-modify-write capability, and single interrupt level. One of the often cited drawbacks of the VSBbus is its limitation to six slots. In the PEP II longitudinal feedback system design, it forces the designer to limit data transfers to a reasonable rate. For example, if the time for a DSP to execute the filter is 1μs, as determined experimentally, a DSP board can be accessed only every 1μs or longer; with five DSP boards per VMEbus segment, three VME/VSBbus segments are required, and the aggregate read-modify-write data rate per VMEbus segment is now reduced to 37 Mbytes per second.

Figure 6 shows the architecture we propose. We chose to package the phase detector, ADC, downsampler and hold-buffer, DAC and the amplitude modulator into a VXIbus mainframe, because of its good electromagnetic shielding, cooling, and system power. It has power for the ECL circuitry, and its 1.2 inch board spacing allows for large analog components.

Each VME/VSBbus segment has an interface to the downsampler and hold-buffer via a

Gigabit rate data link and a commercially available microcomputer which is used for loading the DSPs, control and monitoring. This architecture has been reviewed and approved, and the detailed design of the components is in progress. A prototype will be built and installed at the Advanced Light Source (ALS) at LBL.

6. OSCILLATION DAMPING AT SPEAR

A laboratory prototype longitudinal feedback system as described in Ref. 5 has been developed. This model implements a full speed (500 MHz) front end phase detector with digital signal processing for a limited number of bunches. It has been tested on the SLAC/ SSRL storage ring SPEAR. As the SPEAR storage ring does not have a wideband kicker, it is not possible in this configuration to control multiple bunches, though it is possible to measure multi-bunch effects using the fast front end.

It is possible to operate this feedback system around a single stored bunch by using the main RF cavity as a beam kicker to demonstrate the behavior of a single bunch acted upon by a digital feedback system. This approach follows naturally from the logical model of the bunch-by-bunch system. The behaviors of the various filter parameters (tap length, downsampling factor, etc.) can be studied with a real beam, and the performance of the front end comb generators, digitizers etc. measured using realistic conditions. For this experiment the beam was sensed by a button type BPM electrode and processed by the prototype *B* factory front end shown in Fig. 7. The phase detector and phase-locked master oscillator were operated at eight times the SPEAR RF frequency (2864 MHz or 8×358 MHz) using a comb generator circuit developed for PEP II, shown in Fig. 8.

The front end digitizer was run at the nominal 4 ns digitizing cycle, and a simple programmable downsampler hold-buffer circuit for single bunch was implemented. A single DSP was used to compute the feedback filter, and the feedback signal was then put back into the beam via a phase shifter acting on the RF cavity.

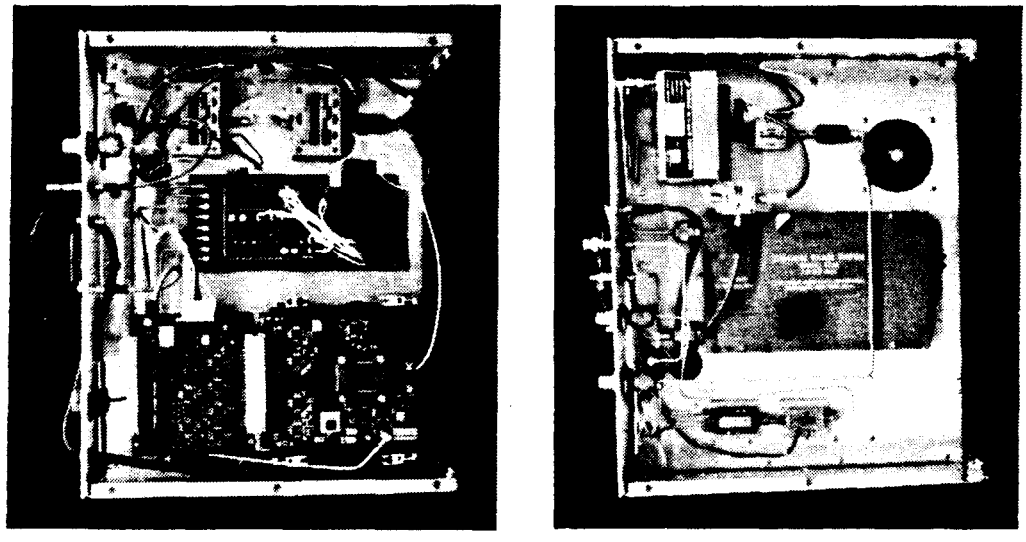

Fig. 7 Photographs of the feedback front end prototype.

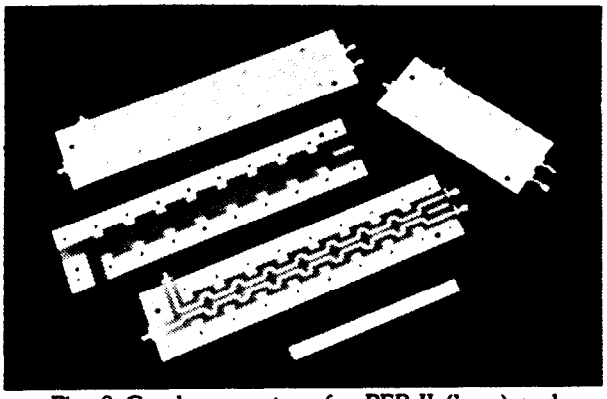

Fig. 8 Comb generators for PEP II (long) and ALS (short).

For this experiment we used a 5-tap FIR filter operating with a downsampling factor of eight. The SPEAR ring was operated with a nominal synchrotron frequency of 32 kHz. The revolution frequency in SPEAR is 1.28 MHz. Thus, a downsample by 8 filters updates a new result every 8 turns, while the ring itself requires approximately 40 orbit revolutions to complete a synchronous oscillation. Figure 9 shows the results of downsampling by eight.

Frequency domain measurements for this system can be made by driving the beam through the RF cavity while observing the response of the beam as a function of frequency.Figure 10 shows the magnitude and phase response of the beam transfer function for an open loop configuration, and for closed loop gains of 18 and 28 dB.In this figure, the open loop gain shows a weakly damped harmonic oscillator. The natural damping present in this case is due to Robinson damping as well as radiation damping. The configuration with 28 dB of loop gain barely displays any resonant behavior, and suggests that the transient response of the combined system will damp in just a few cycles.

The time response of the system can be observed in Fig. 11. In this experiment the feedback loop is opened, and a gated burst at

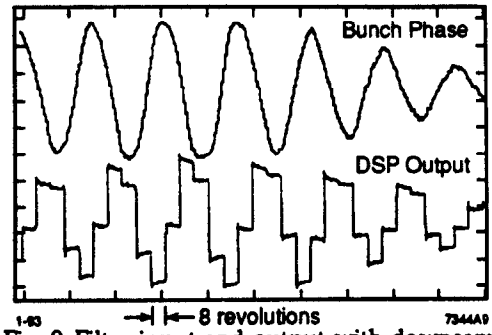

Fig. 9 Filter input and output with downsamplinging factor of 8.

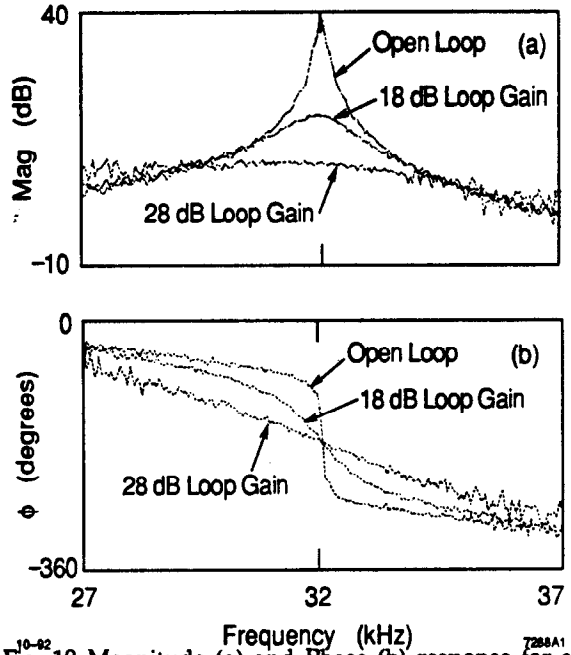

Fig. 10 Magnitude (a) and Phase (b) response for a single bunch for open loop and closed loop gains of 18 and 28 dB.

the synchrotron frequency is applied via the RF cavity. This excitation burst drives a growing synchrotron oscillation of the beam. The excitation is then turned off and the feedback system loop closed. The damping transients of the beam can then be studied for various designs of feedback filter and overall loop gain. The figure shows the damping transient of such a gated burst for a 33 dB loop gain configuration, which provides damped transients of only a few cycles. An alternative method of studying the transient response is to operate the feedback system with overall

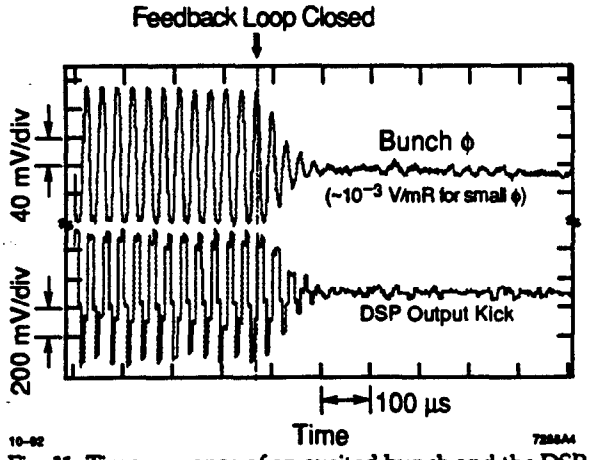

Fig. 11 Time response of an excited bunch and the DSP filter output.

positive feedback for short intervals, which causes any noise present at the synchrotron frequency to produce growing oscillations. After an interval with positive feedback, the gain is made negative to damp the oscillation. This can be made periodic, and the growth/damping rates studied for various configurations of filter gains, such as phase shifts and electronic imperfections.

7. SUMMARY

This system design is the work of a collaboration between staff at SLAC, LBL, Stanford University Electrical Engineering department and INFN Frascati. This group is preparing the detailed design for the prototype longitudinal feedback system to be installed at the LBL ALS facility, and collaborating on the system design of the transverse feedback

Acknowledgements

The ideas presented in this paper reflect the contributions of many people at SLAC, LBL, Stanford University and INFN Frascati. The authors wish to thank Jonathan Dorfan and Mike Zisman for their continued support, Flemming Pederson from CERN for numerous recommendations, and the staff at SPEAR who provided expertise and enthusiasm for the SPEAR experiment.

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