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600 kV Modulator Design for the SLAC Next Linear Collider Test Accelerator*

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Abstract

Preliminary design for the SLAC Next Linear Collider Test Accelerator (NLCTA) requires a pulse power source to produce a 600 kV, 600 A, 1.4 μs, 0.1% flat top pulse with rise and fall times of approximately 100 ns to power an X-Band klystron with a microperveance of 1.25 at ~ 100 MW peak RF power. The design goals for the modulator, including those previously listed, are peak modulator pulse power of 340 MW operating at 120 Hz. A three-stage darlington pulse-forming network, which produces a >100 kV, 1.4 μs pulse, is coupled to the klystron load through a 6:1 pulse transformer. Careful consideration of the transformer leakage inductance, klystron capacitance, system layout, and component choice is necessary to produce the very fast rise and fall times at 600 kV operating continuously at 120 Hz.

Introduction

As physicists look ahead to the next generation linear collider, designs are underway to build X-band klystrons and their pulse power sources. At Stanford Linear Accelerator Center (SLAC), preliminary studies indicate that this klystron will require a beam voltage of 600 kV and have a microperveance of 1.25. Thus the modulator needed to drive the X-band klystron must be capable of a peak power of 340 MW operable to 120 pulses per second. The difficulties in the design arise from the pulse duration and the fast rise and fall times needed. Because of the length (7 - 14 km) and acceleration gradient (50 - 100 MV/m) of the proposed Next Linear Collider, with more than 1600 klystrons [1], the modulator costs must be minimized, and power systems of high efficiency are essential to keep the wall plug power for the accelerator at a manageable level. The most efficient use of power in the generation of the klystron beam voltage comes from a modulator pulse which is as square as possible. For this reason, the rise and fall times of the klystron pulse must be less than 200 ns. Because the efficiency of the RF compression for the Next Linear Collider Test Accelerator (NLCTA) is presently unknown [2], the pulse duration of the modulator pulse could range from 800 ns to 1.4 μs. These conditions make the repetitive production of high peak power pulses difficult to achieve.

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Power Supply Design

The PFN charging circuit consists of a resonant inductor and a high-voltage rectifier unit. The low-voltage AC side of the rectifier is connected to a variable voltage transformer through a circuit breaker, a contactor, and an SCR-controlled bridge (see Figure 1).

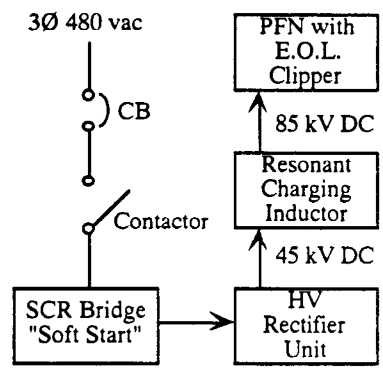

Figure 1. Modulator Power Supply Simplified Schematic.

The rectifier unit, which has a power transformer with two secondary windings, two three-phase full-wave bridge rectifiers, and a filter capacitor, will supply up to 45 kV DC at full load to charge the PFN through the resonant inductor at a maximum output pulse frequency of 180 Hz. The resonant charging inductor has an inductance of 8 mH on its primary high-voltage side and it is provided with a secondary low-voltage winding for a controlled deQueing of the PFN resonant charging. The voltage regulation of 0.1% should be achieved by the deQueing system. Maximum average charging current for the inductor is 3.3 A. Both the rectifier unit and the resonant inductor are housed in separate tanks and immersed in oil.

The nominal voltage on the primary side of the rectifier unit is 480 VAC line-to-line. The AC contactor functions as a main disconnect while the SCR bridge, on the other hand, provides a "soft start" for the rectifier unit.

Modulator Considerations

Different approaches were considered in the design of the modulator. The first consideration is a switch to repeatably handle a peak power of 340 MW. To switch a single charged line directly into a matched load requires a switch that can stand off greater than 1.2 MV, turn fully on within ~ 100 ns, and recover to 1.2 MV at 120 Hz, 24 hours a day. Such a switch does not exist. The switch

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voltage can be reduced to 600 kV if a Blumlein is considered, such as the proposed Japan Linear Collider (JLC) modulator [3], but high power repetitively pulsed magnetic switches have many problems still to be solved. A gridded klystron was considered as a high voltage switch, but none have been developed for near 600 kV operation. The limited lifetime of spark gaps prevent their use, and the gas handling systems for such a high quantity of blown spark gaps would be a nightmare. In the future, solid state switches may be used, but at present their expense is prohibitive. Back Lit Thyratrons (BLT's) need more research and development before they can be considered a viable option. Other switching modalities are also too unknown to consider at present. Thyratrons are a possibility for voltages of 100 kV and lower, but then a transformer becomes necessary to achieve the required voltage. The advantage is that thyratrons and pulse transformers are, relatively speaking, better known technologies for the required specifications.

If a thyratron is chosen as the switch, then a pulse transformer with a low leakage inductance is necessary to step up the voltage to 600 kV. Because the thyratron inductance and the capacitance of the klystron's load will slow the pulse rise time, the leakage inductance of the pulse transformer must be made small. This leads to either a pulse transformer with a limited turns ratio, or a transmission line transformer (TLT). Knowing that there are thyratrons available capable of switching 100 kV in 100 ns leads to a design of a transformer with a low turns ratio of 1:6. The disadvantage of this design arises from the unproven long-term high power operation of the 100 kV thyratrons. 50 kV - 75 kV thyratrons are a more proven switch technology, although 340 MW of peak power at 50 to 100 kW average power is still questionable. The issue then becomes the improbable design of a low-enough leakage inductance transformer with a turns ratio of higher than 1:6. This points back to the 100 kV thyratron design. A TLT is a possibility to step up the voltage, but a traditional pulse transformer with a turns ratio of 1:6 can most likely be built with a low enough leakage inductance to achieve the required pulse rise time. Because there are some concerns about operating a thyratron at 100 kV, a three stage Darlington circuit will be used to step up the modulator voltage into a pulse transformer to 100 kV while operating the thyratron at ~ 67 kV.

Modulator Design

The 600 kV modulator design is based on the standard type "E" PFN [4] used in a 3 stage Darlington configuration. For the klystron load pulse of 600 kV for 1.4 μs, with rise and fall times on the order of 100 ns, certain design parameters dominate. In order to achieve the 1.4 μs wide pulse with ~ 0.1% to 0.2% flat top, a PFN with a large number of sections is necessary. Discrete transmission lines would be preferable, but the physical size for long pulses tends to become quite large. For the output pulse to achieve 600 kV, a pulse transformer is used. The turns ratio and number of turns of the pulse transformer is minimized to reduce leakage inductance, and 6:1 was determined to be feasible. For a standard single PFN or line, operating at 120 Hz into a matched load of ~ 1000 Ω, a 200 kV switch would be required for a 600 kV load pulse with a 6:1 pulse transformer. A standard Blumlein was also considered, but the switch voltage would still have to be 100 kV with 0% to 100% rise times of approximately 100 ns for the entire pulse. Switches capable of operating in these ranges for any length of time are rare. A 3 stage Darlington network [4] with a voltage multiplication of 1.5 has been designed, which only requires a switch-tube to operate at ~ 67 kV.

The PFN design follows from the preliminary klystron parameters of a beam voltage of 600 kV with a microperveance of ~ 1.25. The peak klystron current is determined with the permeance equation:

$$I_{\text{klystron peak}} = kV^{1.5} = 581 \text{ Amps}$$

Therefore, for PFN design considerations, the klystron load impedance during the pulse is 600 kV/581 A = 1032 Ω. With a pulse transformer turns ratio of 6:1, the equivalent impedance of the PFN is:

$$Z_{PFN} = \frac{Z_{\text{klystron}}}{N^2} = \frac{1032\ \Omega}{36} = 28.7\ \Omega$$

Utilizing these numbers, the three stage Darlington network (shown in Figure 2) was designed.

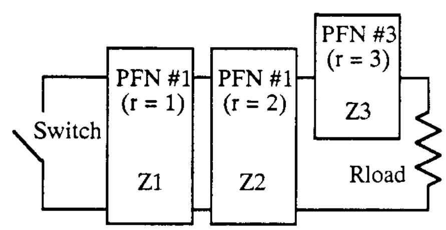

Figure 2. Three Stage Darlington Network Simplified Schematic.

The network impedances, Z_1 , Z_2 , and Z_3 are derived from the following formulas.

$$Z_r = R_{load}\left[\frac{r\,(r+1)}{n^2}\right] \text{ for 4 terminal devices}$$

where r is the PFN stage number, starting at 1 from the PFN nearest the switch, and n is the total number of stages. Therefore,

$$Z_1 = 28.7\ \Omega\left[\frac{1\,(1+1)}{3^2}\right] = 6.4\ \Omega$$

$$Z_2 = 28.7\ \Omega\left[\frac{2\,(2+1)}{3^2}\right] = 19.1\ \Omega$$

And for the 2 terminal device, which is the last of the Darlington stages,

$$Z_r = \left[\frac{R_{load}}{n}\right]$$

therefore,

$$Z_3 = 9.6\ \Omega$$

After consideration of the above mentioned parameters, the individual PFNs were designed. 15-section type "E" PFNs were chosen to achieve fast rise time and the required flat top characteristics. For standard type "E" PFNs, the total inductance and total capacitance are found from:

$$L_{PFN\ Total} = Z_{PFN}\left(\frac{\tau}{2}\right)$$

$$C_{PFN\ Total} = \frac{\tau}{2\,(Z_{PFN})}$$

where τ is the desired output pulse width. With the above equations, the individual inductor and capacitor values are determined.

The Darlington circuit produces line impedances that are proportional to the ratios of the line number to the total number of lines. In the 3 stage Darlington case, the ratios are 2/9, 2/3, and 1/3 the reflected klystron load impedance of 28.7 Ω. Fortunately, the PFN impedances, ranging from 6.4 Ω to 19.1 Ω, allow PFNs to be constructed that utilize components that can be built. With a Darlington network, voltage multiplication increases with the number of stages. For the SLAC X-band klystron load, 3 stages appear to be the optimum number. A Darlington with 4 stages, in our case, would yield a first line impedance of 3.5 Ω. For a pulse width of 1.4 μs, the individual inductances of the 4 stage Darlington PFN sections approach 160 nH, which could prove difficult to build. Therefore a 3 stage Darlington was designed, which has physically realizable component values. The overall schematic diagram is shown in Figure 3.

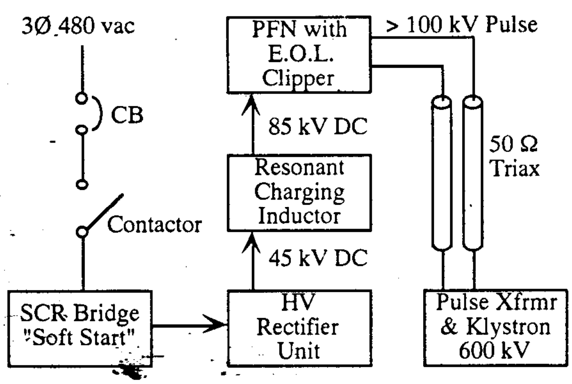

Figure 3. Overall Schematic Diagram of SLAC NLC Modulator.

Klystron fault conditions can produce reflected voltages in the PFN assembly, and an End-of-Line Clipper (EOLC) assembly will be used to dissipate the reflected energy. The EOLC consists of a stack of inorganic resistor modules of a few Ohms total, and a stack of fast solid-state diode assemblies that are individually shunted with Zinc-Oxide modules. The entire assembly will be built in to a low inductance assembly for fast response. The EOLC assembly, in fact, is expected to be between 50 and 100 nH, for a 67 kV stack. The inverse voltage protection diode for the thyratron switch tube is a similar solid-state diode, Zinc-Oxide assembly.

The switch tube, in this case a thyratron, will operate at up to 80 kV, with 12 kA peak currents for the 1.4 μs pulse width, all at 120 Hz continuous operation. This is extremely harsh duty for any switch device, and with the added specification of ~ 100 ns rise time for the pulse, a high peak power, high rep-rate, high voltage, high di/dt tube is required. Two devices will be tested: the EEV CX-2593 and the ITT F-263.

The PFN capacitors also undergo relatively harsh duty. The capacitors in the first PFN line undergo a 50% voltage reversal. The second PFN line capacitors undergo a full 100% voltage reversal. High voltage pulse reversal will generally decrease the lifetime of a capacitor, but the reversal has been taken into account in the capacitor design. The modeled voltage wave forms of the individual lines as well as the output pulse is shown in Figure 4.

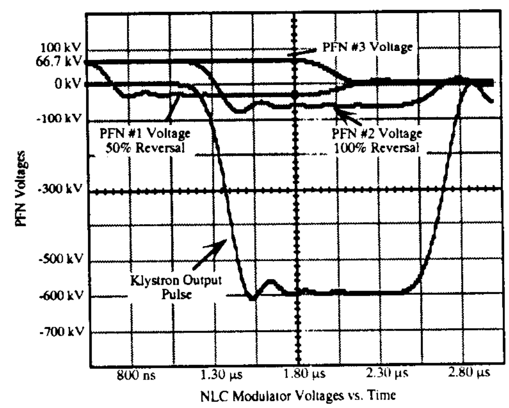

Figure 4. Modeled PFN Voltage Wave forms and Output Wave form into Klystron Load.

The circuit was modeled with SPICE using a three-stage Darlington network, with a primary pulse-transformer leakage inductance of 2.2 μH (80 μH on secondary), 150 nH thyratron inductance, and a Q of 15 for each inductor.

The individual inductors for each PFN section will be ~ 280 nH, 780 nH, and 390 nH. A single type of coil will be utilized for all three values, with taps at different turns to produce the proper inductance. Each coil will be mounted vertically from the top of the capacitors, and encased in a flux-excluding can, as shown in Figure 5. The vertical mounting enables tuning of the PFN during operation, by adjusting a "lid" that fills the cylinder horizontally and contacts the proper turn on the inductor. Figure 6 shows the top view of the modulator tank, including the folded PFN lines. The pulse width can be reduced by removing individual LC sections of each PFN without affecting the impedance of the line.

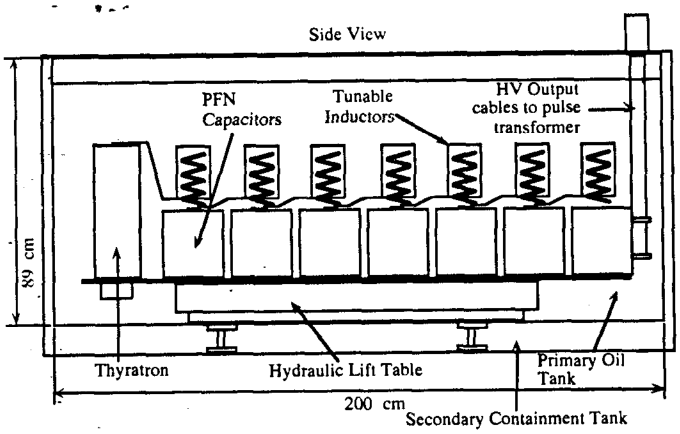

Figure 5. Side View of Modulator Tank Showing Thyratron, Capacitors, Tuning Inductors, and Lift Table.

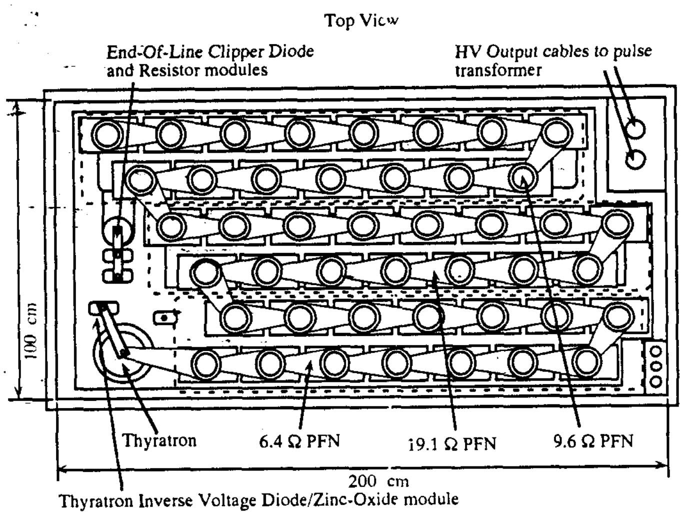

Figure 6. Top View of Modulator Tank Showing Thyratron, Tuning Inductors, and Folded PFN Lines.

Pulse Transformer Design

The pulse transformer is one of the most important items in connection to the rise time of the klystron voltage pulse. In most modulators, the leakage inductance of the pulse transformer is often the voltage rise time limiting factor. To minimize the leakage inductance of the transformer, voltage ratio of 6:1 is used for an output voltage of 600 kV at ~ 620 A with an input voltage of 100 kV at 3800 A. In general, the smaller the voltage ratio of the transformer, the lower the leakage inductance can be designed for a given core size. In addition, the transformer will be an auto-transformer type with a turns ratio of 5:1, which will further reduce the leakage inductance. The transformer, as designed by Magna Stangenes, will be this standard type, two parallel primary basket windings with two parallel tapered secondary basket windings. The secondary leakage inductance is expected to be less than 80 µH.

The transformer primary will be driven by two parallel 50 Ω cables (25 Ω), which is slightly positively mismatched to the secondary load of ~ 28.7 Ω (klystron impedance/turns ratio squared). The near-matched impedance of the cable will reduce the inductive effects of the cable leads on the rise time of the klystron voltage pulse.

The transformer voltage droop (due to magnetizing current-losses current) will be under 2.5% and compensated by adjusting the impedance along the PFN to reduce the flat top voltage droop to under 0.2%

The transformer core will be biased by an isolation inductor connected to the primary winding to increase the volt-second capability of the transformer to allow for a 1.4 µs pulse (ESW).

The klystron heater power will be provided through the transformer secondary/primary windings, eliminating the need for an additional heater transformer.

The pulse transformer is expected to have a voltage rise time into ~ 1000 Ω (with a source rise time of less than 100 ns) of less than 200 ns.

Summary

Based on the described design, construction will begin this summer, with initial testing anticipated for late summer. Critical components including the thyratron, pulse capacitors, end-of-line clipper assembly, and pulse transformer all remain to be thoroughly tested. This modulator is being constructed as a prototype, with potentially several hundred to be constructed in the future. Modularity in construction is important and is employed where feasible.

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References

1. "Towards the Next Linear Collider," J. Irwin, SLAC-PUB-5651(Sept. 1991)
2. "RF Power Generation for Future Linear Colliders," W.R. Fowkes *et al*, SLAC-PUB-5282, June 1990.
3. "A 600 kV Blumlein Modulator for an X-Band Klystron," Toshiba Corp & KEK, 8th IEEE Pulse Power Conference, San Diego, CA, 1991.
4. "Pulse Generators," G. N. Glasoe and J. V. Lebacqz, Volume 5, M.I.T. Rad Lab Series, Dover Publications, New York, New York.