SLAC-PUB-5661
November 1991
(I/E)

MASTER TIMING AND TOF MODULE*

G. Mazaheri
Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309 USA

Abstract

In conjunction with the development of a Beam Size Monitor (BSM) for the Final Focus Test Beam (FFTB) at SLAC, we have built a general purpose timing device with capabilities useful for many different applications. The Time Master consists of a fast clock, a large memory loaded via a PC, and a time vernier (analog) with 8-bit resolution. The Time Master generates an arbitrary pattern of pulses on 16 different channels (up to 256), with a resolution of $1/2^8$ times the clock period. The clock content is stored in another memory to measure the time of up to 16 channels, with a resolution of $1/2^8$ times the clock period (frequency is set at 50 Mhz), using a time-to-amplitude vernier. The data stored in the memory is accessed via a PC. The depth of the memory for pattern generation is 15 bits (32767), equal to the depth of the time measuring part.

The device is self-calibrating, simply by prescribing a pattern on the output channels, and reading it into the time measuring section. The total clock length is 24 bits, equivalent to 334 ms of time at 50 Mhz frequency. Therefore, the resolution is of the order of 32 bits (i.e., 24 bits of clock plus 8 bits of vernier).

INTRODUCTION

One of the requirements for the Final Focus Test Beam (FFTB) is the measurement of the beam size at the Final Focus. A method for doing this to submicron accuracy requires very accurate timing (fraction of nanoseconds) of long (hundreds of microseconds) time intervals. In order to measure this time interval, we chose a method which has very good linearity and a large dynamic range; i.e., the use of a high-frequency oscillator with a counter (Ref. 1). The resolution obtained by this method is proportional to the oscillator frequency (20 ns for 50 MHz). To obtain the high resolution required, we further subdivide the clock period with an analog time to amplitude converter, read by an 8-bit flash ADC.

The combination of a clock counter plus vernier has the linear dynamic range of the counting method and the high accuracy of the analog method for a short range interval (less than 100 ns) (Ref. 2).

PRINCIPLE OF OPERATION

The principle of operation and a simplified block diagram of the Master Timing and TOF module are presented in Fig. 1. As shown in the block diagram, it consists of two separate sections, the Time Master and the Time of Flight (TOF). The circuits described in this section have been designed using predominantly ECL 10 KH components to achieve good timing resolution and minimize propagation delay.

Time Master

This circuit generates an arbitrary pattern of pulses on 16 different channels (up to 256). It consists of a 24-bit synchronous counter (binary) with a free running clock. The output of this counter is converted to Gray Code to minimize the transition errors to $\pm 1/2$ least count. The resulting Gray Code is followed by a 24-bit word comparator. Pattern generation data (in Gray Code) are written in consecutive locations of a 24-bit × 32 K (15 bit) pattern memory (PAT MEM) via a PC. The content of this memory is then converted from TTL to ECL through a 24-bit TTL-ECL latch and is fed to the word comparator. The initialization and start of the pattern generation is by a start command from the keyboard, or by an external pulse. When a word is recognized, a pulse is generated and sent to a 15-bit memory address register (MEM ADD) and triggers an 8-bit programmable delay unit (Time Master Vernier). The MEM ADD is incremented each time a word is compared. The delay data for each pulse is loaded to an 8 × 32 K memory (VER MEM) via a PC. The full scale setting of the time vernier (programmable delay, AD 9500) is equal to the clock period. Output of the programmable delay unit is sent to a 1-to-16 decoder, which is addressed by an 8 × 32 K channel identification memory (CHID MEM). Output pulses are available either in NIM or TTL levels. The minimum pulse separation between two successive pulses is 140 ns, limited by the dead time of the circuit.

Time of Flight (TOF)

As is shown in the Fig. 1 block diagram, TOF accepts 16 different timing pulses (up to 256), and assigns to each timing pulse a channel identification number and time information. The time information is expressed in a 24-bit Gray Code, thus limiting the transition errors to $\pm$ 1/2 least count while latching data from a running clock. The rationale of using a Gray Code and details of its generation are given in Ref. 1. The time data and channel identification data are stored in a 24 × 32 K TOF time memory (TOF TIME MEM) and TOF channel identification memory (TOF CHID MEM) respectively. We use a time vernier circuit to measure the fraction of clock period between a timing pulse and the following clock pulse plus one. This circuit consists of a time-to-amplitude converter and an 8-bit high-speed Flash ADC (AD 9012, 10 ns conversion time, 1/2-bit LSB linearity). The digitized data are stored in the TOF Vernier memory (TOF VER MEM). The data stored in the memory are accessed via a PC.

Prototype Board

A wire wrapped prototype of the Master Timing and TOF module was constructed, and consists of two boards: a Fast Bus size board to accommodate 165 IC's, and a small size board for TOF Vernier. In order to ensure optimum performance, basic high-frequency design rules were used around ECL 10KH components, and especially for the TOF Vernier circuit that uses an AD9012 Flash ADC. See Fig. 2.

* Work supported by Department of Energy contract DE-AC03-76SF00515.

Presented at the IEEE Nuclear Science Symposium and Medical Imaging Conference, Santa Fe, NM, November 5-9, 1991.

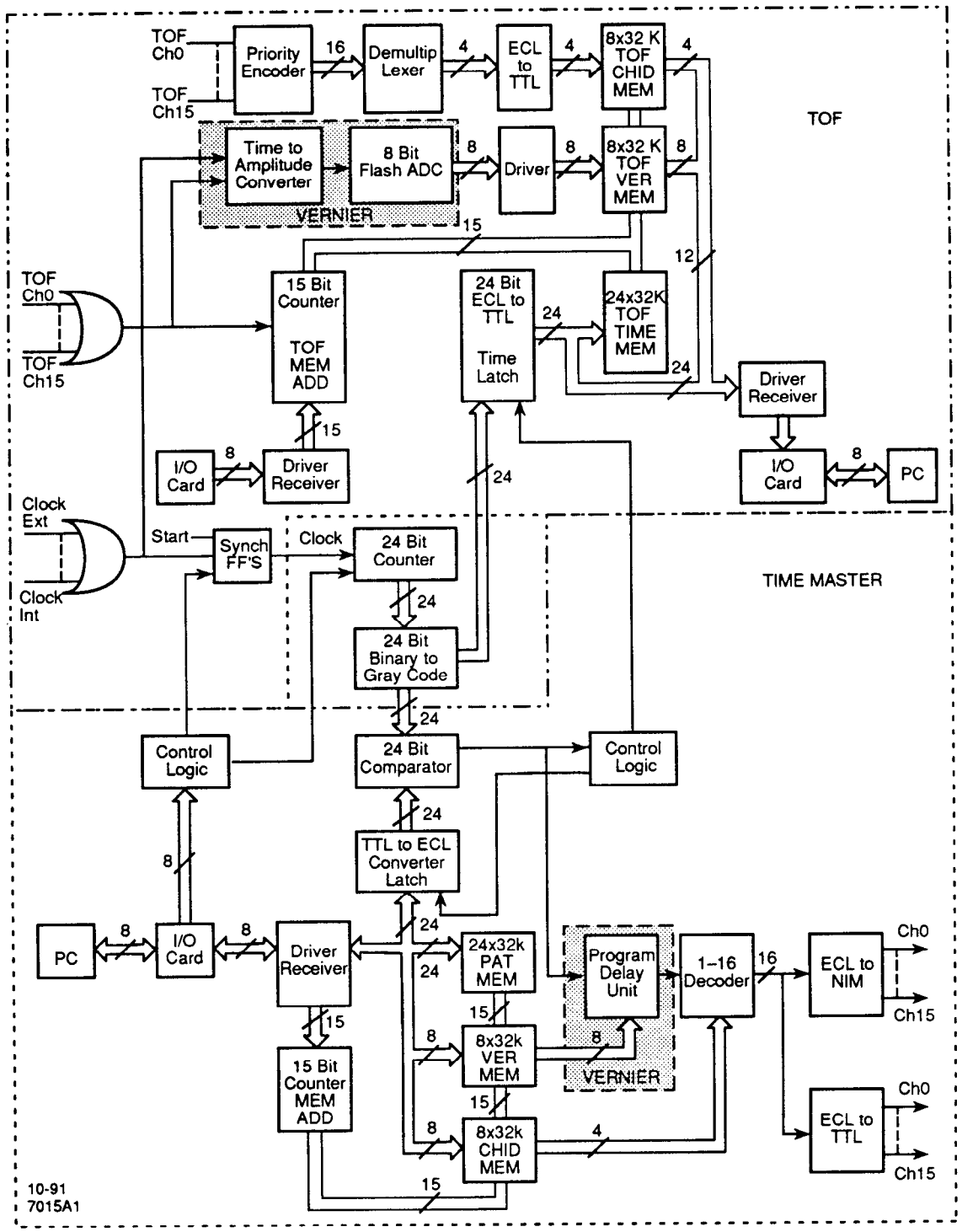

Figure 1. Principle of operation and simplified block diagram of the Master Timing and TOF module.

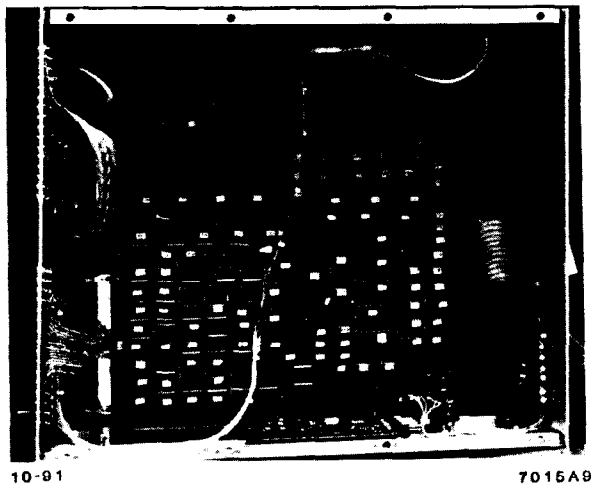

Figure 2. Picture of Master Timing and TOF module showing wire-wrapped board, Vernier board, and interconnections.

Test and Performance

The circuit has been tested using the Time Master part and an external pulse generator. Fig. 3(a) shows the pulse separation distribution between two channels in clock count units. As expected only one bin is filled. Fig. 3(b) shows the vernier distribution for the same sample; notice that the single channel sigma of the vernier data (σ_1 = 51 ps) is the combination of fluctuations from the Time Master and from the TOF. The values of Sigma given are the usual; $\sigma = \sqrt{\langle x^2 \rangle - \langle x \rangle^2}$the least count is 90 ps for all the data presented. In Fig. 3(c) the vernier difference between two channels is histogrammed. In this case we have $\sigma_2 = \sigma_1\sqrt{2}$, because we add two sigmas in quadrature.

Figure 4(a) shows the pulse separation distribution between two channels, using an external pulse generator. We have mainly two bins filled, because the two pulses are randomly distributed with respect to the internal clock.

Figure 4(b) shows the vernier difference distribution between two channels for the same data sample of Fig. 4(a). There are two different peaks, corresponding to the different pulse separations.

Figure 5(a) shows the vernier distribution for one channel, using the external pulse generator:

$$dN(v)/dv \ ,$$

where $dN(v)$ is the number of the event, with a vernier value within the interval $[v, v + dv]$. This distribution should be flat because the pulses are randomly distributed with respect to the internal clock:

$$dN(t)/dt = C(C \text{ an arbitrary constant,}) \qquad (1)$$

where $dN(t)$ is the number of events within the interval $[t, t + dt]$.

Indeed, assuming that the vernier value is linear with time:

$$v = K^* t \ .$$

With K a relative constant by differentiation, we obtain:

$$dv = K^* dt \ .$$

Substituting this in (1) gives:

$$dN(v)/dv = C/K \ .$$

The deviation from a horizontal line is a measurement of the non-linearity of the TOF system while converting

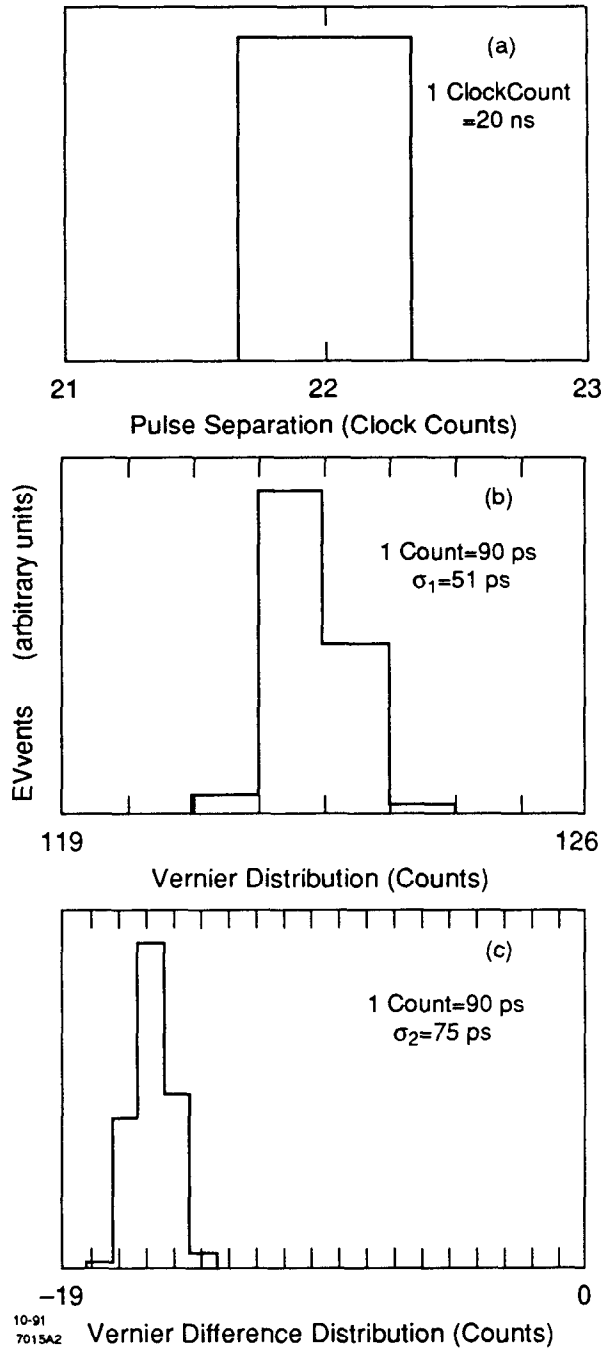

Figure 3. Using Time Master circuit, distributions of: (a) Pulse separation between two channel units of clock period; (b) Vernier for one channel; (c) Vernier difference between two channels.

the time to a digital number. If we now integrate the vernier distribution with respect to the variable vernier "v," using (1), we obtain the relation between the time and the vernier value "v" according to the following formulas:

$$I(v) = \int_{v\min}^{v} dN(v)/dv * dv = C * \int_{v\min}^{v} dt(v) = C * t(v) \ .$$

Figure 5(b) shows $I(v)$. This function is used to remove the non-linearity of the system, since we know that for each

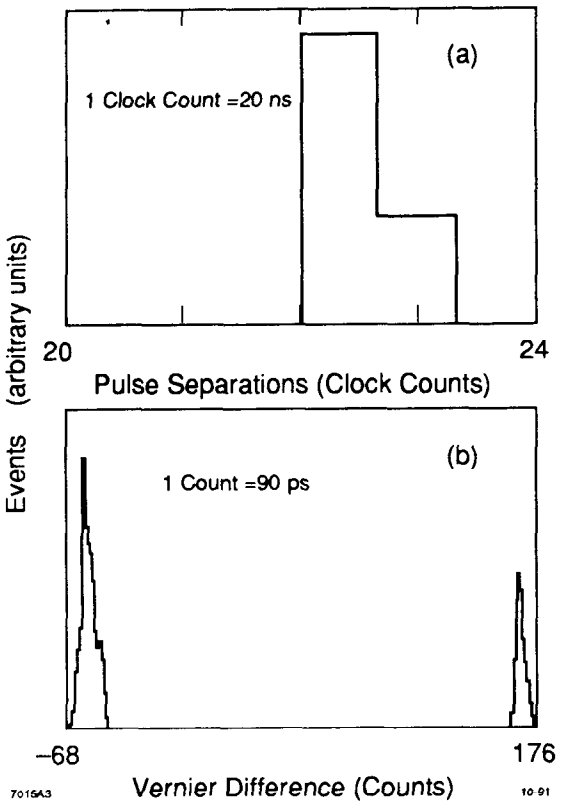

Figure 4. Using an external pulser, distribution of: (a) Pulse separation in units of clock period between two channels; (b) Vernier difference between two channels.

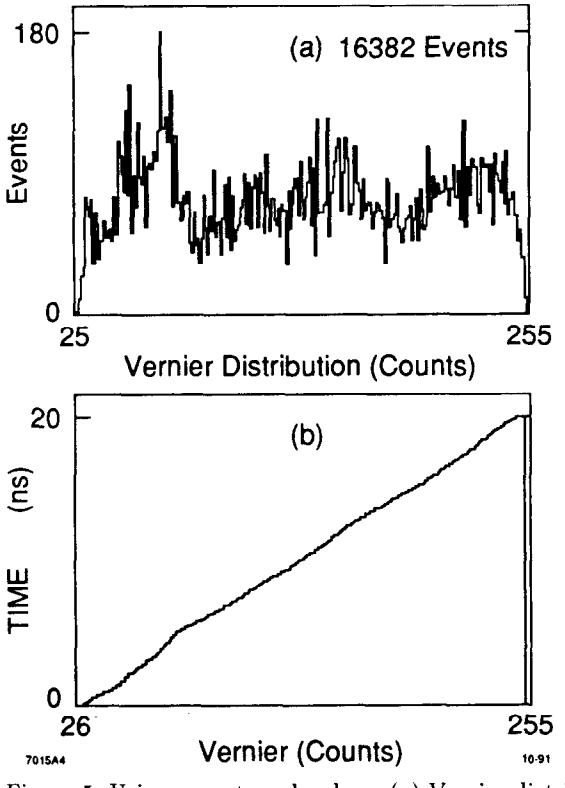

Figure 5. Using an external pulser: (a) Vernier distribution of one channel; (b) Time versus Vernier function obtained by integrating Fig. 5a.

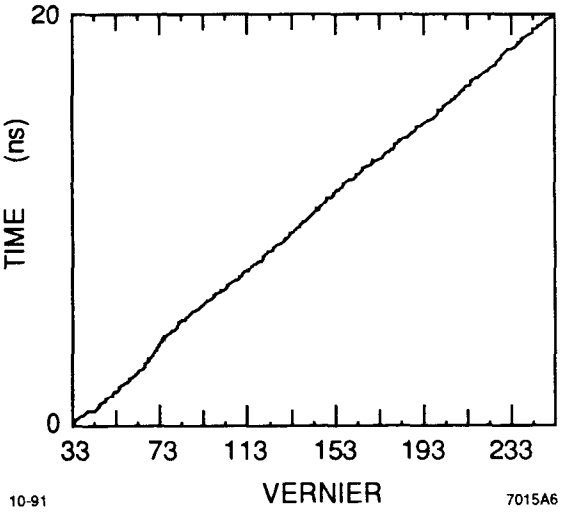

Figure 6. Time versus Vernier using Time Master and a variable delay.

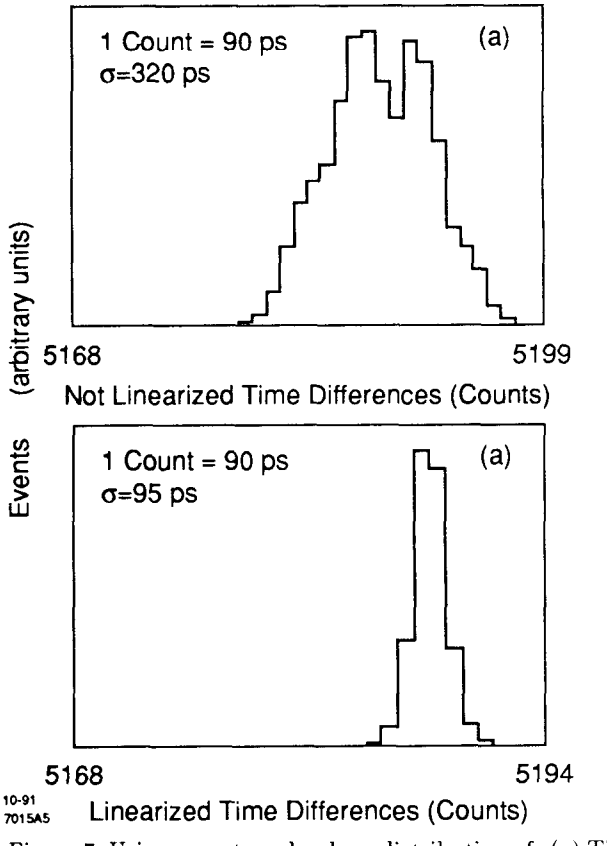

Figure 7. Using an external pulser, distribution of: (a) Time difference (not linearized) between two channels; (b) Time difference (linearized).

vernier value "v," the corresponding "true" time is

$$t(v) = I(v)/I(vmax) ,$$

in clock units; with the conditions that $t(vmin) = 0$ and $t(vmax) = 1$. The same non-linearity has been measured by using the Time Master plus a variable delay. The results are shown in Fig. 6. The two methods give the same results, within the errors. The non-linearity can be removed, using the calibration procedure described above.

Figure 7(a) shows the histogram of the time difference (not linearized) between two channels. The resolution is $\sigma = 320$ ps. Figure 7b shows, for the same data sample, the distribution of the linearized time difference. The resolution in this case is improved greatly with respect to the previous case, $\sigma = 90$ ps. We are measuring two different pulses so we can estimate the absolute resolution by measuring one pulse as $\sigma = 90\ \text{ps}/\sqrt{2} = 65$ ps.

The measured resolution is constant within $\pm 10\%$ for pulses separating from 300 ns up to 10 ms.

SUMMARY

We have developed a stand-alone module interfaced with a PC, with the capability to either generate or accept 16 different timing signals (up to 256), with an accuracy of less than 100 ps in measuring time in the range of 300 ns to 330 ms, at a clock frequency of 50 MHz.

ACKNOWLEDGEMENTS

The author thanks Dr. F. Villa for helpful discussions and technical assistance, K. Bouldin for assistance in the construction of the unit, and Dr. S. Williams for writing software to test the module. Special thanks to Dr. P. Raimondi for software support and data analysis.

REFERENCES

1. D. Porat and S. Wojcicki, "Fast synchronoous Gray counter," Nucl. Instrum. Methods 169 (1980) 243.

2. Juha Kostamovaara and Risto Myllyla, "Time-to-digital converter with an analog interpolation circuit," American Institute of Physics, Rev. Sci. Instrum. 57 (11), November 1986.