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VERTEX DETECTOR TECHNOLOGY FOR THE SSC*

P. Skubic[f], J. Arens[c], H. Attias[g], K. Barger[e], T. Collins[a], G. Jernigan[c], G. Kalbfleisch[f], D. Kaplan[f], P. Karchin[g], G. Kramer[a], J. Kuehler[f], M. Lambrecht[f], E. McCliment[e], W. Ross[g], S. Shapiro[d], J. Sinnott[g], S. Utku[g], C. Wilburn[b], S. Worley[a]

[a] *Hughes Aircraft Company, Carlsbad, CA 92009, Hughes Aircraft Company, El Segundo, CA 90245,* [b] *Micron Semiconductor, Inc., Longwood, FL 32750,* [c] *Space Sciences Laboratory, University of California, Berkeley, CA 94720,* [d] *Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309* [e] *University of Iowa, Iowa City, IO 52242,* [f] *University of Oklahoma, Norman, OK 73019,* [g] *Yale University, New Haven, CT 06511*

Abstract

An overview of a SSC R&D program for silicon vertex detector development is presented. The current test program with silicon microstrip and pixel detectors is discussed and selected results of beam tests are presented including measurements of position resolution as a function of angle of incidence. Plans for future tests are also discussed.

Introduction

We have a R&D program[1] in progress to develop detectors capable of reconstructing particle decay vertices in experiments at the SSC. This program includes development of VLSI readout electronics, radiation damage measurements[2], mechanical design, Monte Carlo simulations, and development of solid state tracking detectors in collaboration with industry. This work[3] is aimed at developing high resolution vertex detectors to be used at hadron colliders to measure secondary vertices from decays of particles with intermediate P_t such as charm and bottom particles.

A vertex detector must measure the impact parameter of tracks of decay secondaries relative to the primary vertex. The *r.m.s.* impact parameter resolution due to multiple scattering is approximately given by $\sigma = (0.015R/P_t)\sqrt{X/X_o}$ where X/X_o = fraction of radiation length of material up to and including the first detector layer, R = radius of the first position measurement, P_t = transverse momentum (GeV/c) of the secondary particle with respect to the beam. Since σ increases with R, the radius of the detector should be kept as small as possible. Such a detector in the SSC environment could be exposed to ionizing radiation doses of 10 Mrad per year and must provide good spatial resolution over a wide range of incident angles. Therefore, the vertex detector should have good intrinsic position resolution (< 10 μm), good signal-to-noise, and material must be minimized to reduce multiple scattering. Because of these requirements, our R&D work has concentrated on silicon tracking detectors including double-sided microstrip and pixel detectors, and associated VLSI readout circuits.

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Silicon Microstrip Detectors

AC-coupled silicon microstrip detectors were used in a 227 GeV/c pion test beam at Fermilab during the summer of 1990 to study the position resolution as a function of incident angle. Single-sided detectors (made by the Center for Industrial Research in Oslo, Norway) which had a strip pitch of 25 microns with every alternate strip read out[4], and double-sided detectors (made by Messerschmitt Bolkow Blohm in Munich, Germany[5]) of the design used for the Aleph experiment at LEP were used. SVX-D chips[6] were used to read out the silicon microstrip detectors which were used to measure positions in only one view. LBL designed SRS and SDA CAMAC modules[7] were built by the University of Oklahoma to control the SVX chips and read data out to the VAX on-line computer. The layout of the test beam and silicon microstrip results are described in more detail in a talk at this conference by P. Karchin.[8]

The SVX chips were operated in double-sampling mode with a sample time of 2.4 μs. All 128 channels per chip were read out on every event. A noise of 2.9 ADC counts (~ 1800 electrons) was obtained during the beam test with the Oslo detectors. The average signal for minimum ionizing particles at normal incidence was 43 ADC counts when summed over two adjacent readout strips. (Since alternate strips were read out, charge sharing occurs if a particle passes through an intermediate non-readout strip.) Therefore the maximum (when all charge is collected by a single strip) signal-to-noise ratio was 14.8.

Bench tests at Oklahoma were carried out with 34 SVX-D chips with no detector connected. Thirty of these gave an average noise per channel of 1.5 ADC counts (~ 900 electrons) with the 2.4 μs sample time. The other 4 chips

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were rejected because of significantly larger noise. The chips were operated successfully with a clock rate up to 20 MHz. Fig. 1 shows the negative gain linear response in ADC channels for two amplifier channels of the same chip to a calibration pulse which varied in 100 steps from 0 to -200 mV (gain 8 setting). The responses of the remaining 126 channels of the chip lie between the two curves shown.

During the beam test, a hodoscope of from three to five detectors was placed in a precision stand which allowed selected planes to be rotated about a horizontal axis. In one configuration, data where taken with the two outside detectors at normal incidence with respect to the beam and the center detector was rotated to angles of 0, 25, 35, and 45 degrees with respect to normal incidence with the rotation axis parallel to the diode strips. Fig. 2 shows the difference between measured position in the center plane and the predicted position from the outside planes for 35° which gave an *r.m.s.* position resolution of 15.6±0.7 μm.

In order to verify that the detector was working as expected, a Monte Carlo program was run which simulated operation of the microstrip detectors and SVX readout circuit. This program tracks particles through the silicon microstrip detector and simulates deposited ionization charge according to the expected dE/dx distribution for silicon. The collected charge at each amplifier was smeared according to a Gaussian distribution with an *r.m.s.* of 1800 electrons to simulate the effect of amplifier noise. Fig. 3 shows the position resolution versus angle of incidence for the Monte Carlo compared to the test beam measurements and shows good agreement between the data and the simulation.

Pixel Detectors

Beam tests were also performed with hybrid pixel detectors which consisted of a 256 x 256 diode array sensor with 30 μm x 30 μm elements (made by Micron Semiconductor Inc.) bump-bonded with Indium to a readout chip manufactured by Hughes Aircraft Company. This hybrid detector has been used previously in infrared imaging applications for space science and astronomy.[9] Two independent stand-alone data acquisition systems, one built by Hughes Aircraft Co. and the other built by UC-Berkeley Space Sciences Laboratory, were used in the beam tests and both systems performed well. Detectors of this type have many advantages compared to long microstrip detectors including good multi-track resolution, simultaneous measurement of positions in two dimensions, good signal-to-noise, and resistance to radiation damage effects.

The readout was designed to function as a camera and therefore all 65,536 elements were read out on every event in a minimum time of 16 ms. The detectors (and readout chips) were operated at room temperature. Fig. 4 shows a 128 pixel square region of a typical event with pedestals subtracted for an array with incident 227 GeV/c pions using the UC-SSL data acquisition system. We expect these data to be useful in measuring properties such as charge sharing which will determine the optimized design of future readout circuits. Further results from the pixel beam tests are presented in a talk by S. Shapiro at this conference.[10]

Future Plans

During the second half of the Fermilab fixed target run, we expect to continue our program of beam tests of silicon tracking detectors. A hodoscope of up to five pixel detectors will be used to measure their position resolutions as a function of incident angle. Similar measurements will be made with double-sided silicon microstrip detectors which will be supplied by Micron Semiconductor.

In parallel with the test beam work, design will proceed on the next generation pixel detector readout circuit which will subtract pedestals and have sparse readout and time slicing capability. The schedule for this R&D program is described in a talk by J. Arens at this conference and a preliminary design for the readout architecture is presented by O. Barkan.

VLSI readout design will be carried out by a collaboration of Fermilab and Oak Ridge National Laboratory, and radiation damage tests will be done with microstrip and pixel detectors, and with electronic readout circuits as part of the continuing R&D program. This future work will be coordinated with the Silicon Tracking Subsystem Collaboration, of which Oklahoma and Yale are members, and future development of detectors will continue in collaboration with Hughes Aircraft Company and Micron Semiconductor Inc.

References

[1] This work was supported by U.S. Department of Energy contracts DE-AC03-76SF00515, DE-AS05-80ER10629, and DE-AC02-76ER03075/A048.

[2] E. J. Kennedy, et. al., "Radiation Effects on JFETS, MOSFETS, and Bipolar Transistors, as Related to SSC Circuit Design", these proceedings.

[3] H. Castro et al., R&D proposal to Fermilab (E784/BCD) Jan. 2, 1989.

[4] M. Caccia et al., Nucl. Inst. Meth. **A260** (1987) 124.

[5] P. Holl et al., IEEE Trans. Nucl. Sci. **36** (1989) 251.

[6] Kleinfelder, S. A., et al., IEEE Trans. Nucl. Sci. **35** (1989) 171.

[7] F. Kirsten and C. Haber, IEEE Trans. Nucl. Sci. **37** (1990) 288.

[8] H. Attias et al.,"Beam Tests of Silicon Microstrip Detectors with VLSI Readout", these proceedings.

[9] S. Shapiro, et al., Nucl. Instr. Methods **A275**, 580 (1989).

[10] Stephen Shapiro, et al., "Performance Measurements of Hybrid PIN Diode Arrays", these proceedings.

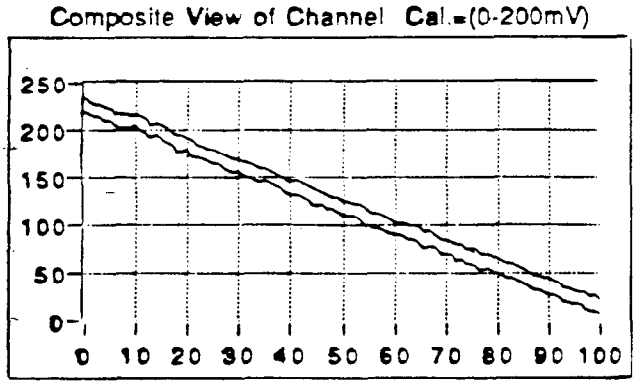

Figure 1: Negative gain response in ADC counts (ordinate) of two channels of a typical SVX-D VLSI readout chip to a calibration pulse which varied from 0 to 200 mV in 100 steps. The responses of the other 126 channels lie between the two curves shown.

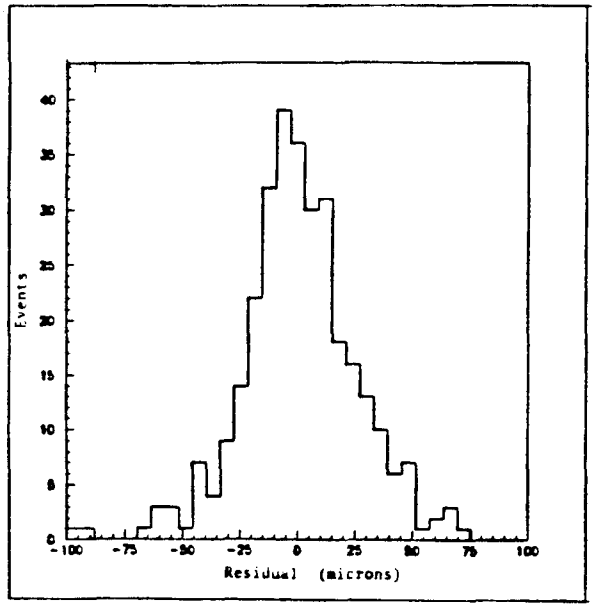

Figure 2: Residual in μm between the measured and predicted cluster position for tracks with an incident angle of 35°.

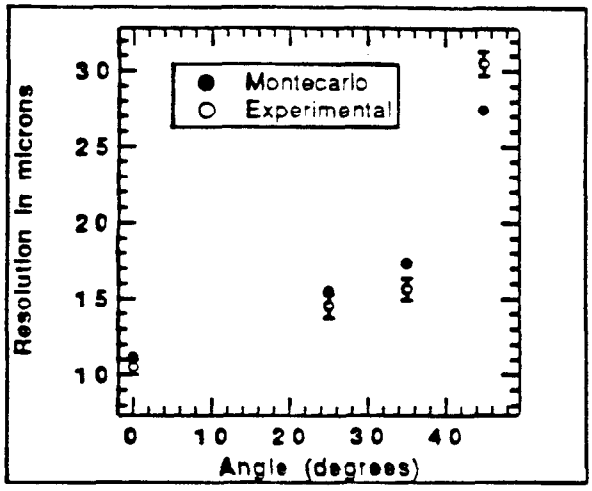

Figure 3: Position resolution versus track angle of incidence for Monte Carlo simulation and for test beam data.

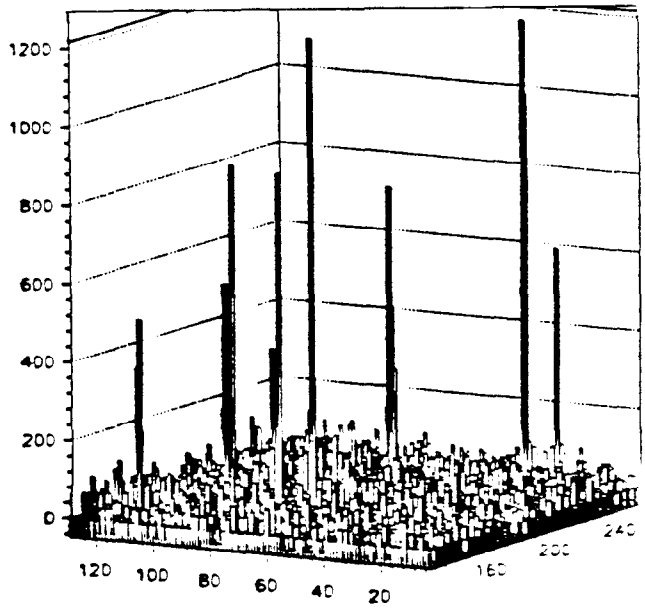

Figure 4: Event display showing pulse heights in ADC counts of a 128 pixel square region of the hybrid pixel detector operated at room temperature and illuminated with 227 GeV/c pions.