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SILICON PIN DIODE ARRAY HYBRIDS AS BUILDING BLOCKS FOR A VERTEX DETECTOR AT AN ASYMMETRIC B-FACTORY

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ABSTRACT

Silicon PIN diode hybrid arrays are proposed as the ideal building blocks for a vertex detector at an asymmetric B-factory. The two-dimensional nature of the detector segmentation allows for the maximum in confusion elimination. Fine spatial resolution, on the order of 10μm per layer, is more than adequate to resolve the displaced vertices of beauty and charm decays. A high signal-to-noise ratio allows for the thinning of the detectors, reducing multiple scattering. Time tagging within the detector permits higher background levels than could otherwise be tolerated, and on-board electronics which includes zero suppression and ghost elimination, eases downstream data handling and analysis.

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1. INTRODUCTION

Pixel devices, in particular silicon PIN diode arrays, are a natural choice for vertex detectors. These devices provide three-dimensional coordinate information with spatial resolution of a few microns, and so provide efficient trackfinding with a minimum number of layers.

An architecture which is appropriate for high-energy charged particle detection is that of a hybrid.[1,2] The charged particle detector, a silicon PIN diode array, and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips, indium bump bonded together, form the array hybrid.

The indium bump bonding process is one in which each diode of the detector array is bonded to an independent amplifier readout circuit on a mating VLSI chip via an array of aligned indium metal bumps that cold weld under pressure to form ohmic contact. This process allows flexibility in the detector and the readout electronics specification. In the case of the B-factory, this permits the eventual thinning of both the detector array and the electronics without a change in their design. Figure 1 is a schematic representation of a hybrid detector.

2. EXISTING ARRAYS

Development of hybrid arrays has been a goal of the author since 1984. To this end, three hybrid arrays have been designed and fabricated. The high resistivity silicon diode arrays were fabricated by Micron Semiconductor Inc., and the readout arrays by the Hughes Aircraft Company. The indium bump bonding was also done by Hughes Aircraft Company with bumps measuring less than 15 μm in diameter.

A program of laboratory and high-energy beam line testing of the arrays has been carried out, and is nearing completion. Support for this project has been primarily from SLAC and from generic detector development funds provided by the SSC Laboratory.

The first array, a 10×64 array, having pixels 120 μm on a side, has ten readout channels per array, one for each column. The readout structure allows random access to any pixel. There is no power necessary during the time data is being detected and stored by the array; however, during the read cycle 10 mW (1 mW per channel) is necessary. The readout electronics is an NMOS VLSI circuit which is radiation resistant at the level of 1 MRad of ^{60}Co gamma rays.

The second array, a 256×256 array, having pixels 30 μm on a side, has two readout channels per array. Random access readout is available via row and column shift registers. Data stored in the pixel represented by the intersection of row and column address is presented to the readout node. No power is necessary for storing data, and only 2 mW is necessary for readout. The readout electronics is an NMOS VLSI circuit which is not particularly radiation-hard.

The third array is similar to the second, except that the readout electronics, though identical to the second array, is implemented in a PMOS VLSI circuit. This variation was found necessary to preserve the option of using these arrays at room temperature. The PMOS array is more appropriate to collect the holes rather than the electrons generated by the passage of the charged particle through the silicon. The PMOS circuit has a much larger dynamic range of operation, and dark current integrated over the time necessary to read the 32,768 pixels on each readout node no longer develops voltages that drive the circuit to its supply rails.

A description of the hardware necessary to read out these arrays is published elsewhere,[3,4] as are the results of preliminary laboratory tests.[5]. In brief, alpha and beta sources have been used on the first two of the above arrays, confirming their ability to detect charged particles. The noise level has been measured to be less than 300 electrons rms at room temperature, resulting in a signal-to-noise ratio of about 80:1. The spatial resolution for those particles which share their charge between two pixels has been found to be less than 2 μm.

In August 1990, arrays of the third type were placed in a 250 GeV/c pion beam at Fermilab. These results, unpublished at this time due to the preliminary nature

of the data, show clearly the detection of these high energy pions, with a signal-to-noise ratio in excess of 50:1 at room temperature. Figure 2 is a three-dimensional plot of a single frame of data showing a number of particles traversing the array.

3. THE PROPOSED ARRAY

The hybrid array being designed and developed for use at the SSC has many features which are useful and exciting for the asymmetric B-factory. A summary of the design goals is presented in Table 1.

TABLE 1

SPECIFICATION	PROTOTYPE	FINAL GOAL
Pixel size	50 μm $\times$ 150 μm	50 μm $\times$ 50 μm
Array size	128 $\times$ 64	256 $\times$ 256
Noise	$< 200\ e^-$	$< 200\ e^-$
Time stamping	YES	YES
Time resolution	50 ns	16 ns
Ghost elimination	NA	YES
Nearest neighbor read	NA	YES
Readout time	10 μs	1.5 μs
Radiation hardness	NO	10 MRad
Power	NA	0.1-1.0 W/cm^2
Technology	0.8-1.2 μm	0.5 μm SOS/CMOS
Clock speed	NA	1 GHz

There are actually three phases to the design effort. The first phase requires the implementation of the essential elements of the design in a FORESIGHT chip. FORESIGHT is a fabrication capability similar to MOSIS offered by the Orbit

company, which allows circuits to be fabricated on a community wafer for quick turnaround. The actual pixel design, shown in Fig. 3, is incorporated into a 32×64 array and only minimal external support circuitry is included on the chip itself. The goal is to confirm that the time between the arrival of the charge, and the DETECT signal arriving at the periphery of the chip, is about 50 ns. This feature (called time stamping) requires a discriminator within each pixel, and is one of the more exciting features of this design. One will also be able to test details of the analog circuitry of the pixel, such as linearity, a noise level of less than 300 electrons rms, and pixel-to-pixel variations. All array operations will be under external contro, rather than being generated internally, but confirmation of the random access nature of the Read/Write signals can be achieved. The FORESIGHT chip was received on September 20, 1990, and is undergoing tests at this time.

After successful operation and testing of the FORESIGHT chip, the PROTOTYPE chip design will proceed. The pixel cell will be identical to that in the FORESIGHT chip, differing only in that the feature allowing electronic testing of the pixel will be removed. Thus, to test the PROTOTYPE chip one will have to hybridize it to an array of PIN diodes. The entire support circuitry will be implemented so that one can read out only interesting data. The self-timing operation will be tested, confirming the time stamping and the time resolution with the chip internally generating all of its control signals. The reading of interesting pixels will be controlled by a single TRIGGER command. The actual design of the support circuitry is complete and is described elsewhere.[6]

The third phase of the program is the reduction in size of the pixel to 50 μm $\times$ 50 μm by the use of 0.5 μm minimum feature size SOS/CMOS technology. The FORESIGHT chip employed 1.2 μm double-metal technology; however, the reduction in minimum feature size does not necessarily guarantee a smaller pixel, as many features of the circuit (such as capacitors and metal line width) do not scale with this parameter. Lastly, the implementation of radiation hardening techniques, such as thinning of the gate oxide to achieve the 10 MRad specification, will be implemented. Additionally, changes in circuitry to further harden the

circuit will be attempted at this stage. The radiation hardness specification is certainly not the driving issue for the B-factory that it is for the SSC, and this step can possibly be relaxed to 1 MRad in this case.

A few details are noteworthy concerning the pixel design in the FORESIGHT chip. It has 21 transistors, 5 capacitors, and 17 lines comprised of power rails, clocks, biases, and outputs per pixel. Theoretically, the noise will be below the 300 electron limit, the power consumption is less than 20 μW per pixel, dead time is about 400 ns, the feedback capacitor is designed to be about 10 fF and the open-loop gain of the first stage is about 200. These parameters are being put to the test this month. A calculation of the fill factor—the area of the chip containing pixels compared to the total area of the chip—for the final 56 $\times$ 256 array is 94%.

4. MECHANICAL DESIGN ISSUES

Pixel array hybrids differ from microstrips in that they are not self-supporting as are microstrip detectors, but must be supported on a substrate. The substrate must provide support, not only for the arrays, but for the their support circuitry such as traces, preamps, ADCs, output multiplexers, and DSPs (if necessary). Two candidates for this substrate material are foams made of either silicon carbide or boron carbide. Boron carbide has the longer radiation length, 20.8 cm compared to 10.1 cm for silicon carbide. Both materials can be foamed to 3% of their density while retaining machineability. They are both electrical insulators. Silicon carbide has superior thermal properties when compared to silicon, thus allowing one to consider other than room temperature operation. A number of mechanical design studies are under way[6] investigating the proper use of these foams as support material for SSC vertex detectors. These studies also deal with cooling requirements at the level of 1 W/cm^2.

An embryonic mechanical design study of a silicon vertex detector for the B-factory has been reported.[7] The pixel detectors described in this note and

the use of either of the foam materials mentioned would provide the basic material for such a vertex detector. However, much mechanical design work remains to be done.

5. A DESIGN CHALLENGE

A number of colleagues have reached the conclusion that in the measurement of CP asymmetry parameters, one should not expend heroic efforts to design a vertex detector having the smallest possible inner radius.[8] The gain in overall precision when one takes into account large-angle tracks and the multiple scattering in material interior to the first detector array does not warrant the effort. This is true, up to a point.

However, there are interesting decay channels that contain soft pions that will be unavailable to analysis unless these soft pions and the decay vertices from which they originate are recognized. This can be accomplished if we place the vertex detector within the beam vacuum. Pixel detectors can sustain orders of magnitude more background radiation than can microstrip detectors, due to their inherent two-dimentional nature, the small size of an individual pixel, and the time stamping of each hit with its time of arrival, and they can be fabricated radiation hard to 10 MRad. If one designs a Faraday cage between the vertex detector and the beam, to provide a continuous path for the beam image charge, and if this Faraday cage has less material than a conventional beam pipe, then one can press the vertex detector inward radially to the limits set by the machine designers. This would open up new physics channels for study and increase the resolution in impact parameter as well. Philosophically one is doing the best job possible of finding displaced vertices, while separating this function from that of tracking by placing the actual beam pipe between the vertex detector and the tracking detector.

In designing the Faraday cage, one can combine the cooling problems presented by both the vertex detector electronics and the ohmic and RF heating of the

Faraday cage by the beam. The heating of a beam pipe by the beam is proportional to the resistivity of the beam pipe material. Thus, cryogenically cooling the Faraday cage would reduce its resistivity, and remove this source of heating at its source.

The placement of a vertex detector within the beam vacuum may not be the most prudent first step in the design of a new machine. However, this design takes full advantage of the features of pixel arrays which have not heretofore been available, and as such is deserving of further professional study.

6. CONCLUSIONS

Silicon PIN diode hybrid arrays are serious candidates as building blocks of a vertex detector for an asymmetric B-factory. The two-dimensional nature of the detectors provide the optimum in confusion elimination and ease in downstream software analysis. The high signal-to-noise ratio allows for the thinning of the detector arrays reducing multiple scattering. Time stamping allows the separation of background-induced hits from those related to the event of interest. Much additional work is needed to understand completely the properties of these detectors and to generate a viable vertex detector design based on them.

ACKNOWLEDGMENTS

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FIGURE CAPTIONS

1. Schematic representation of a hybrid detector showing the two separate silicon chips and their bump bond interconnects.
2. A three-dimensional plot of a number of minimum ionizing particles from the Fermilab test beam incident on a detector array, demonstrating excellent signal-to-noise and the power of two-dimensional arrays to eliminate confusion in complex events.
3. Schematic block diagram of the pixel design employed in the FORESIGHT chip, including the input test circuit.

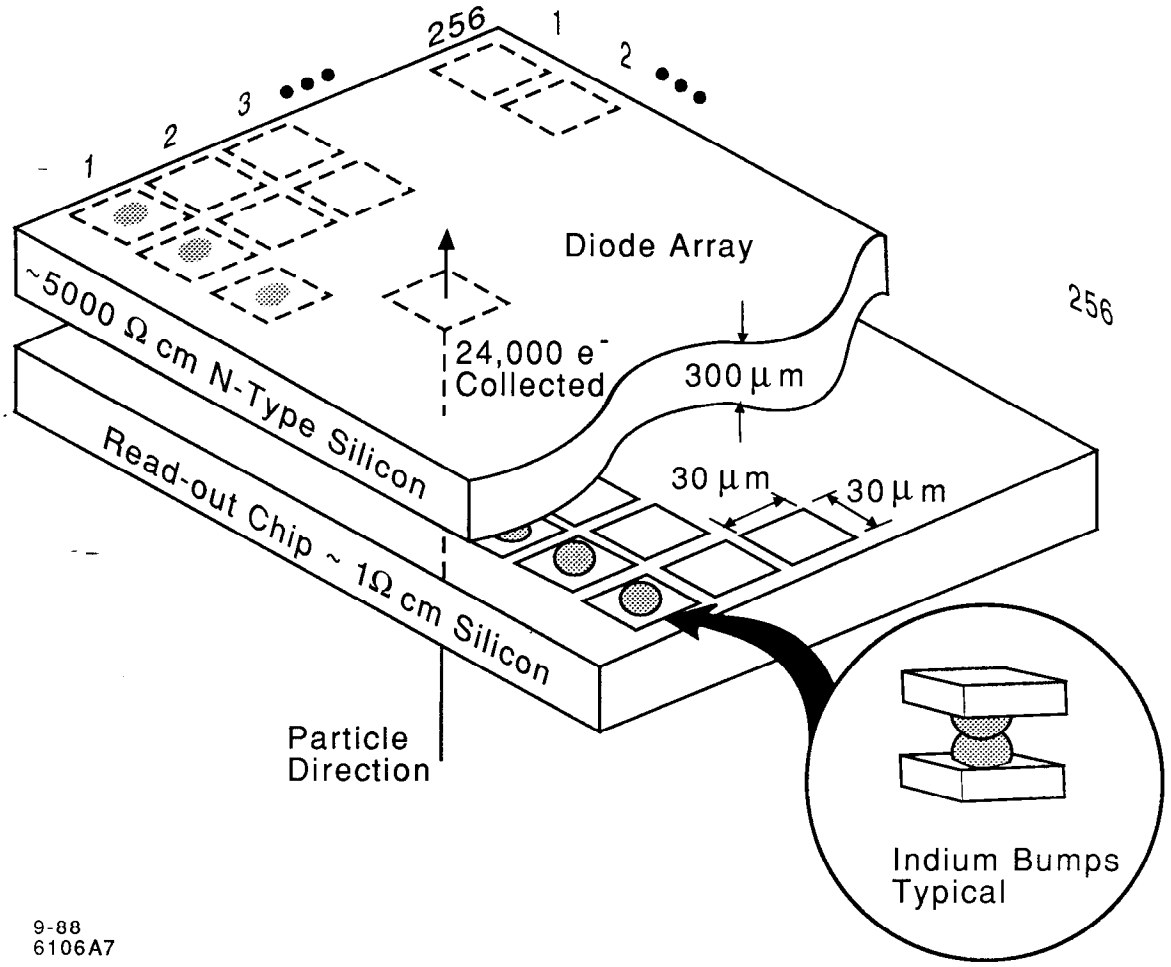
256
1
2
3
1
2
Diode Array
256
~5000 Ω cm N-Type Silicon
24,000 e⁻
Collected
300 μm
30 μm
30 μm
Read-out Chip ~ 1Ω cm Silicon
Particle
Direction
Indium Bumps
Typical
9-88
6106A7

Fig. 1

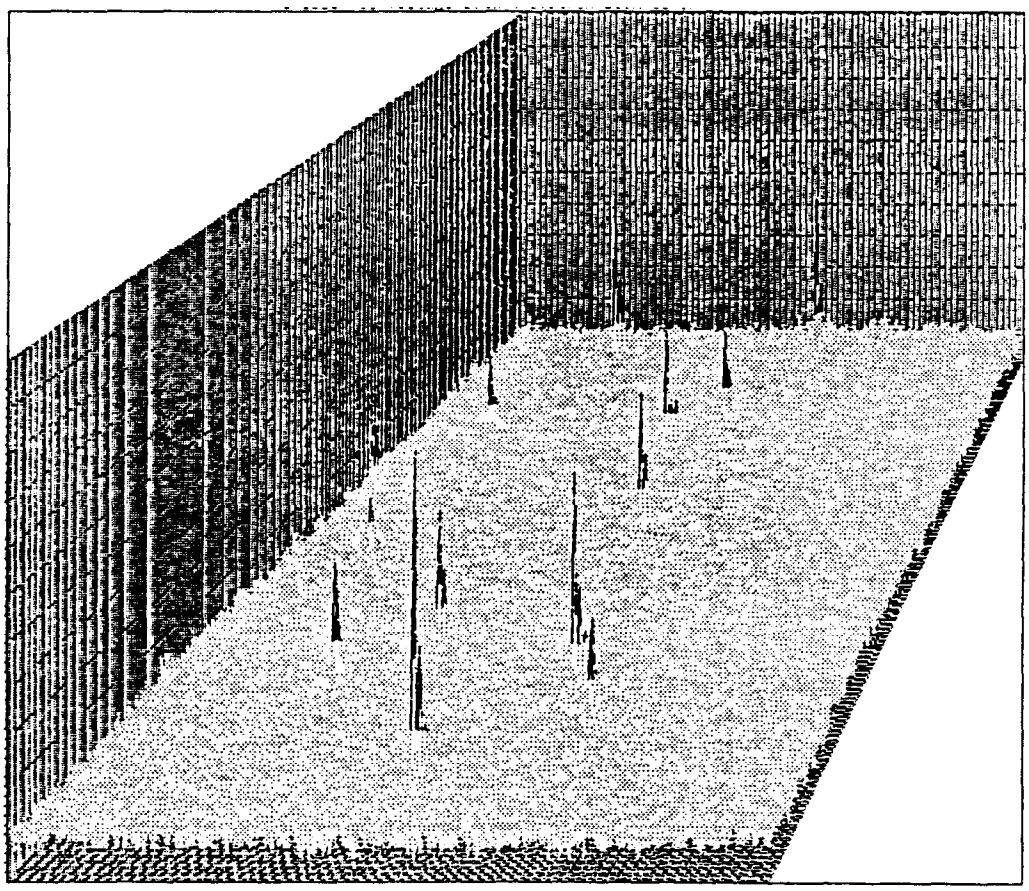

Fig. 2

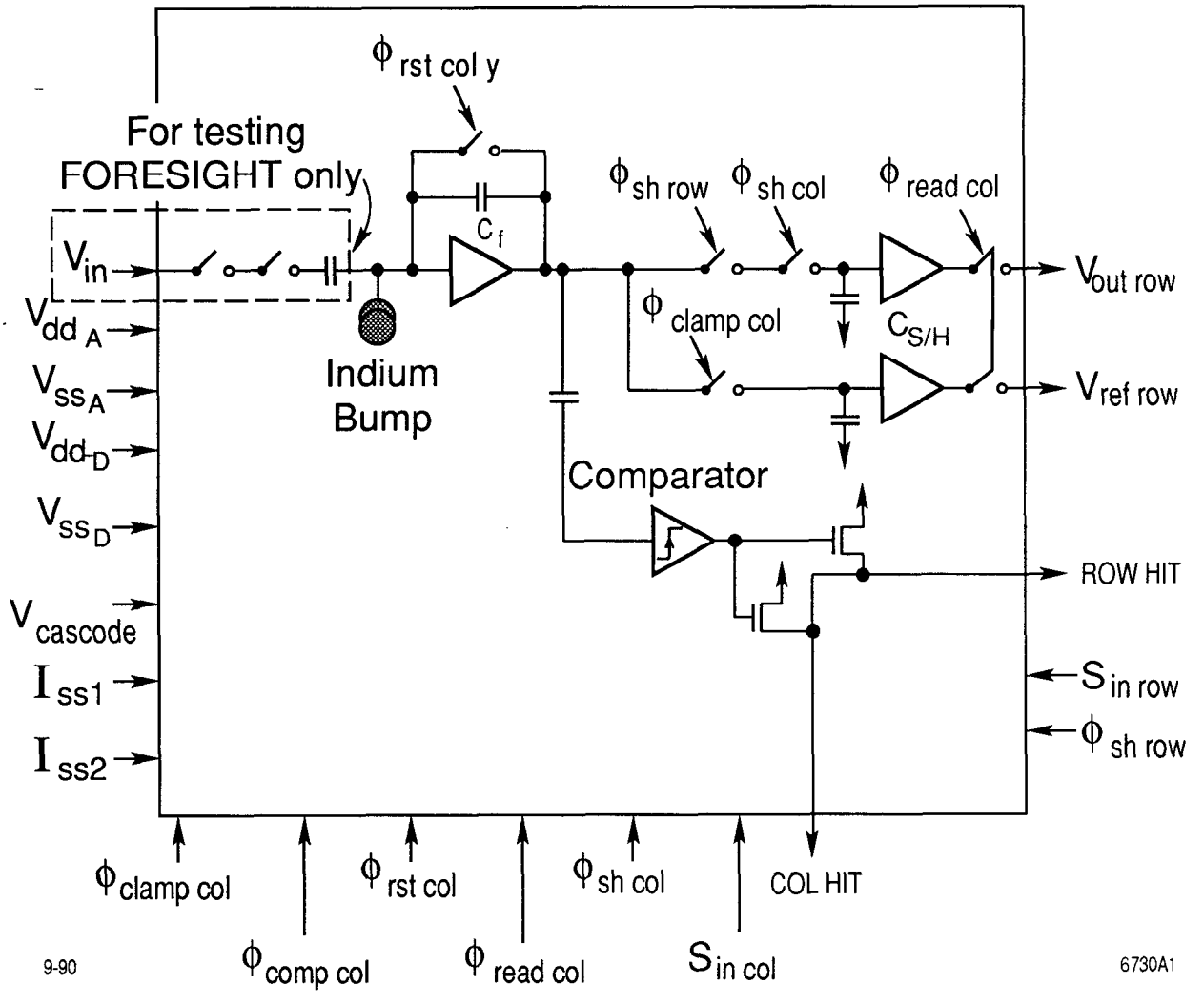
For testing
FORESIGHT only
$\phi_{rst\ col\ y}$
$\phi_{sh\ row}$
$\phi_{sh\ col}$
$\phi_{read\ col}$
C_f
V_{in}
$V_{dd\ A}$
V_{ss_A}
V_{dd_D}
V_{ss_D}
$V_{cascode}$
I_{ss1}
I_{ss2}
Indium
Bump
$\phi_{clamp\ col}$
$C_{S/H}$
$V_{out\ row}$
$V_{ref\ row}$
Comparator
ROW HIT
$S_{in\ row}$
$\phi_{sh\ row}$
$\phi_{clamp\ col}$
$\phi_{rst\ col}$
$\phi_{sh\ col}$
COL HIT
$\phi_{comp\ col}$
$\phi_{read\ col}$
$S_{in\ col}$
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Fig. 3