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The Front-End Analog and Digital Signal Processing Electronics for the Drift Chambers of the Stanford Large Detector*

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Abstract

The front-end signal processing electronics for the drift-chambers of the Stanford Large Detector (SLD) at the Stanford Linear Collider is described. The system is implemented with printed-circuit boards which are shaped for direct mounting on the detector. Typically, a motherboard comprises 64 channels of transimpedance amplification and analog waveform sampling, A/D conversion, and associated control and readout circuitry. The loaded motherboard thus forms a processor which records low-level waveforms from 64 detector channels and transforms the information into a 64 k-byte serial data stream. In addition, the package performs calibration functions, measures leakage currents on the wires, and generates wire hit patterns for triggering purposes. The construction and operation of the electronic circuits utilizing monolithic, hybridized, and programmable components are discussed.

I. Introduction

The Stanford Large Detector (SLD) is a device for the study of electron-positron collisions in order to gain insight into the fundamental particles and forces of nature [1–4]. The SLD measures positions, momenta, energies, velocities, and types of the particles produced in electron-positron collisions at energies near the rest energy of the Z^0 particle, a carrier of the weak force.

The SLD provides charged particle tracking and momentum measurement through a cylindrical Central Drift Chamber (CDC) organized in 10 superlayers [3,5] and two sets of two Endcap Drift Chambers (EDC). Waveform sampling, control, and readout electronics [5] are mounted on both sides of the Central Drift Chamber to permit accurate determination of drift times, charge division z measurement for position along the wire, and dE/dx measurement for particle identification. For the endcap drift chambers there is no charge division measurement and thus electronics is connected only to one side of the wires.

The signal-processing electronics are located on printed-circuit (mother) boards which are mounted on pins connected to the sense wires of the chamber. The 170 boards for the CDC are curved and arranged on circles with ten different radii, corresponding to the 10 tracking superlayers. A CDC motherboard processes signals of up to eight neighbor vector cells, each comprising eight drift wires. The 60 boards for the EDC are rectangular and process signals from up to six drift cells of six wires each. Since these boards have to be bent around the circumference of the endcaps [5], they are made out of rigid-flex material. The electronic circuits on the CDC and the EDC boards are similar to each other.

This paper describes the organization of the motherboards for the CDC and EDC as well as the design of the custom hybrids and monolithic devices which are needed to achieve the required high packing density. The performance of the motherboard is the subject of a separate paper [6].

II. Architecture of the Drift Chamber Motherboard

The drift chamber motherboard is a printed circuit board with surface mount components on both sides of the board. Surface mount components allow high packing densities and provide good electrical isolation of the two board sides through the use of blind vias. This is important because the preamplifier side (facing the chamber) processes low level analog data, while the opposite side, containing Hybrid Analog Memory Units (HAMU), carries high level control and clock signals. Figure 1 shows the block diagram of the board. The signals from the drift chamber are amplified in eight-channel, surface-mount, custom preamplifier hybrids. The amplified signals are then routed to the HAMU side of the board, where 16 four-channel custom unity-gain buffer hybrids increase the drive-current to charge the capacitance at the input of the HAMU hybrids. The buffer hybrids also contain pulse shaping circuitry to realize an approximate $1/t$ tail cancellation of the detector signal. The waveform is sampled and stored in eight-channel, custom HAMU hybrids, containing analog memory monolithics. The TTL-level four-phase sampling clock to the hybrid is generated

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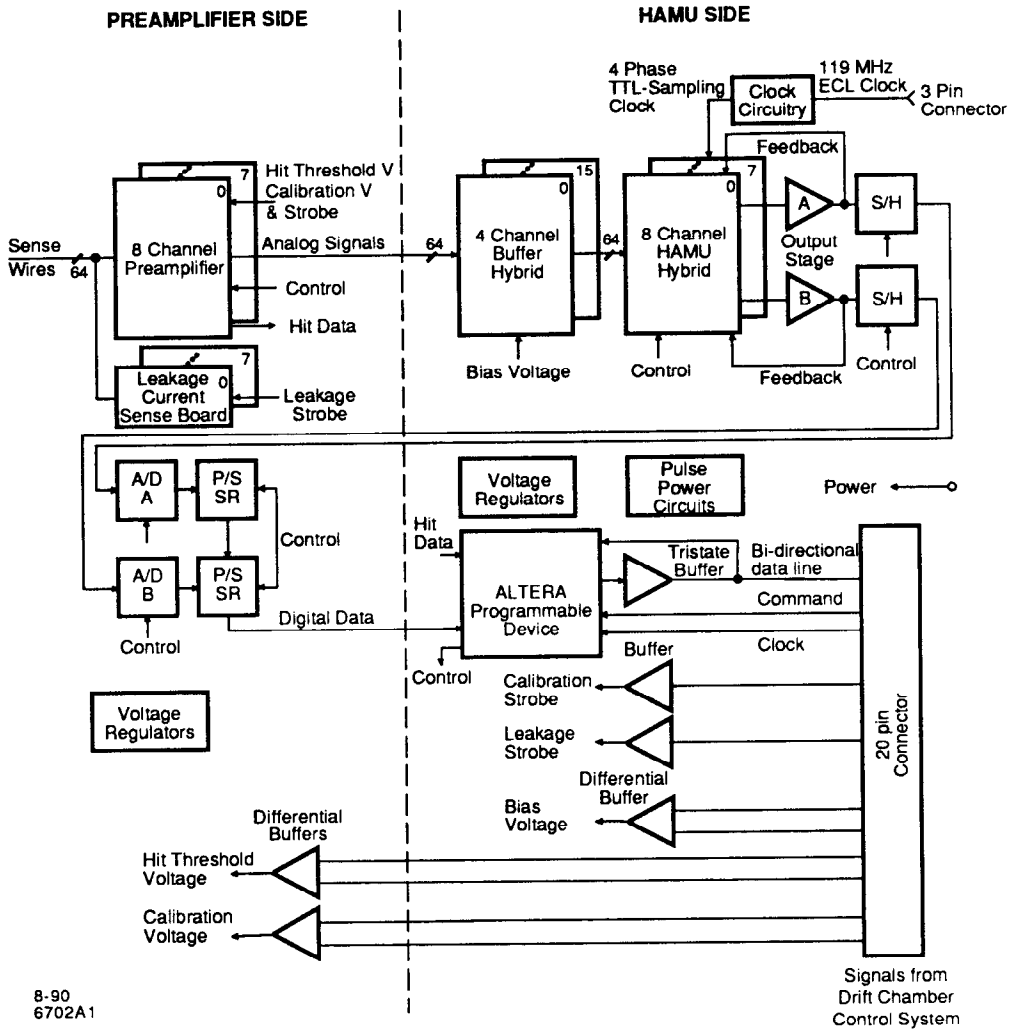

Fig. 1 Block diagram of the drift chamber motherboard. The side of the board facing the chamber is indicated as the preamplifier side.

from a 119 MHz differential ECL clock, which enters the board on a three-pin connector. An ECL line-receiver, an ECL flip-flop package, and an ECL-TTL converter chip are employed to create the four-phase clock on the board.

Readout of the stored signals in the HAMUs occurs only for selected events. Upon an external read request, the stored analog information is multiplexed onto two sets of output buses which are connected to output stages and Sample-and-Hold (S/H) devices. The pipelined signals are then routed back to the preamplifier side of the board, where two 3.2 μsec 12-bit CMOS A/D converters digitize the data. The digital information is serialized in shift registers, in which framing bits for data alignment are added. The conversion and serialization is performed on the preamplifier side, to reduce crosstalk of the digital data to the analog information read out simultaneously on the HAMU side.

Three input signals, COMMAND, DATA, and CLOCK, determine all operations on the board according to the SLD data protocol [7]. These signals are decoded by a 68-pin, surface-mount, programmable ALTERA 1800 EPLD, which functions as a state machine. The data line is bi-directional to minimize the number of wires routed in the chamber, and in output mode the digitized chamber signals and the digital hit data from the amplifiers are multiplexed onto the line by the EPLD.

Three analog voltages are received differentially from the control system [5] by unity gain surface-mount amplifiers. Two of the buffers are located on the preamplifier side for the pulse calibration and hit-threshold voltages for the amplifiers. The third amplifier buffers an offset voltage to bias the HAMU signal inputs or to perform a DC calibration of the HAMU hybrids.

In fig. 1, two digital strobes are shown entering the board on the 20-pin connector. The calibration strobe is routed to the preamplifier hybrids, and the leakage current strobe is connected to the eight-channel Leakage Current Sense Boards. In the leakage current mode, these boards inject a charge at the input of the amplifiers which

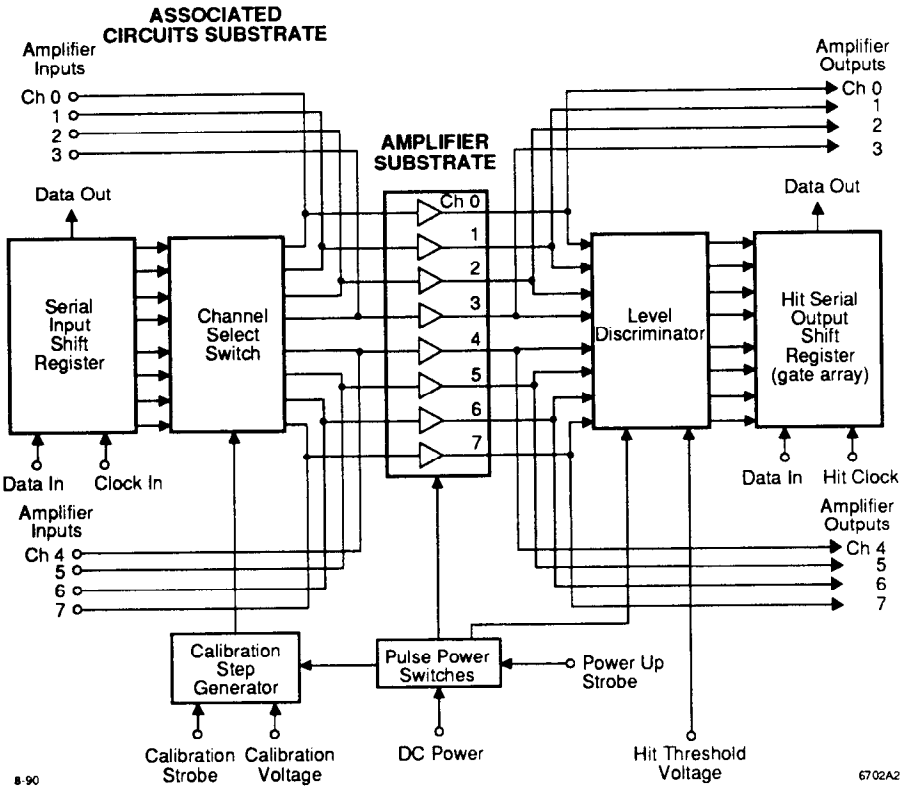

Fig. 2 Block diagram of the drift chamber preamplifier hybrid. Calibration and digital hit readout circuitry are included as well as logic to turn on the power.

is proportional to the leakage current on the drift chamber sense wires.

Most of the electronics on the board are power pulsed to minimize power dissipation. The power pulse circuits for the preamplifiers are incorporated in the amplifier hybrids. The HAMU side contains switching circuits for the clock-circuitry, the buffer and HAMU hybrids, and for the output stages. The board requires five voltages which are regulated by discrete circuits on both sides of the board, since the response time of regulator packages is not sufficient under the pulsed load conditions.

III. Preamplifier Hybrid and Leakage Current Sense Board

The block diagram of the drift chamber preamplifier hybrid [8] is shown in fig. 2. The 6.85 cm x 4.6 cm 40-pin surface-mount device includes eight channels of transimpedance amplification with a gain of 50 mV/μA and a rise-time of 8 nsec. Some changes to the original design [8] of the amplifier were necessary in order to increase the stability margin when it was incorporated into the large drift chamber system. These included removal of the White follower output stage from the amplifier and allocating the power drive function to a separate buffer hybrid on the HAMU side of the board. This results in a higher stability since the current driver needed to charge the large HAMU input capacitance (180 pF) is removed

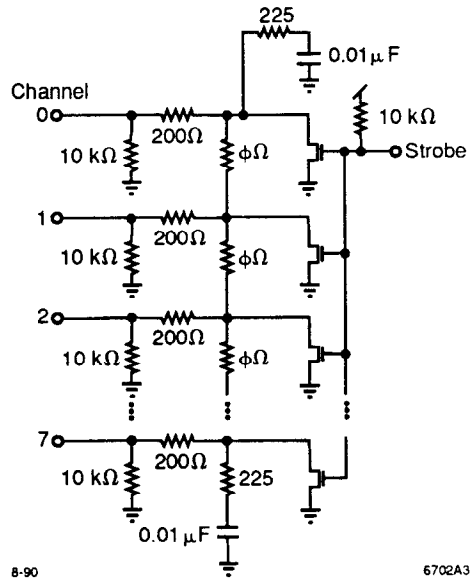

Fig. 3 Schematic of the leakage current sense pc board. The 0 Ω (jumpers) and 225 Ω resistors are not loaded for the central drift chamber. The resistor values are chosen for optimum resolution and settling time of the signal under the power pulse conditions for the preamplifier hybrid.

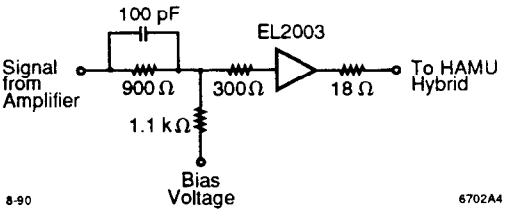

Fig. 4 Schematic of one of the four channels of the buffer hybrid.

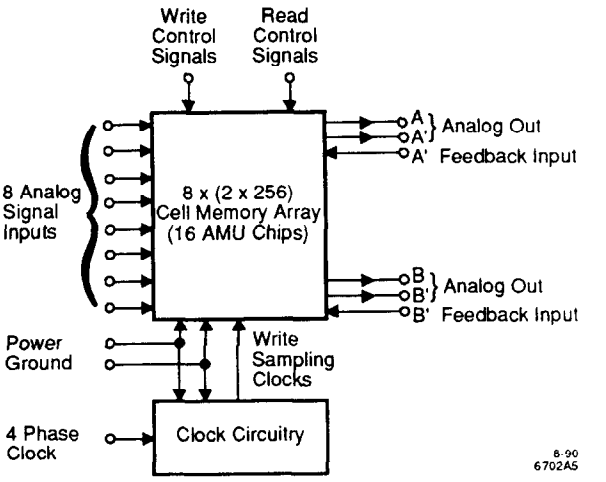

Fig. 5 Block diagram of the HAMU sampling and storage hybrid.

from the high gain preamplifier side. A crosstalk compensation of 5% to the nearest neighbor channels is included in the amplifier to compensate for crosstalk on the wires in the chamber.

Pulse calibration of the amplifiers is realized by sending a pattern into the serial input shift registers (fig. 2) which enables calibration of any combination of channels on the board. The shift registers of the hybrids on the motherboard are daisy-chained and the pattern is sent into the chamber via the SLD three-wire protocol. During run time a power-up control signal from the local EPLD turns on the power to the amplifiers through a power switching circuit included in the hybrid. A sequence of calibration voltage levels and calibration strobes are then applied to determine the pulse response of the amplifiers.

One additional function of the hybrid is a wire-hit data readout. The outputs of the amplifiers are connected to high speed comparators which are set if the signal exceeds the hit threshold voltage. The hit pattern is stored in a gate-array in the hybrid and read out serially after the analog waveform is written into the HAMU storage hybrids. The hit clock shifts the hit data out of the daisy-chained amplifier hybrids and via the ALTERA device onto the bi-directional data line (fig. 1).

In fig. 3, the circuit of the Leakage Current Sense Board is illustrated. This 4 cm x 2 cm board is employed to measure the leakage current of the drift chamber sense wires. A strobe applied to the board injects a charge into the inputs of the preamplifier hybrids which is proportional to the leakage current of the sense wires. This signal is amplified, sampled, and read out like a regular detector signal for off-line processing. The 10 kΩ resistors at the input provide ground return for the sense wires. The resistors between the channels allow for additional crosstalk compensation to all wires of a vector cell, which is only used by the endcaps.

IV. Buffer Hybrid and HAMU Hybrid

Figure 4 shows one of the four channels on the 1.4 cm x 1.3 cm custom buffer hybrid. This hybrid serves three functions. An approximate $1/t$ tail cancellation of the detector signal is achieved by an R-C-R circuit. A low impedance offset voltage applied to the buffer hybrid is used for DC calibration of the system and, during run time, biases the HAMU inputs to 1.9 V for optimum performance. The unity-gain buffers drive the inputs of the storage hybrid and thus remove the currents from the high gain amplifier side of the motherboard.

The simplified block diagram of the analog sampling HAMU [9,10] hybrid is shown in fig. 5. Waveforms of eight channels are sampled on the 6 cm x 4.3 cm device at a rate of 119 MHz for the CDC and 59.5 MHz for the EDC, respectively. The signal of each channel is stored in 512 time buckets on a total of 16 custom AMU [11,12] monolithics. The sampling clocks needed by the AMU chips are generated on the hybrid from the four-phase clock entering the device.

The control signals for the hybrid are supplied by the ALTERA device. During data collection all channels are sampled in parallel. The 4096 memory cells of each hybrid are read out on two sets of output buses (A and B) with an address interval of 4 μsec per cell. The readout of the HAMUs on a board (fig. 1) occurs sequentially and takes 65 msec.

V. Analog Output Stage

The schematic of the analog output stage is illustrated in fig. 6. The goal of the circuit is to reproduce the voltage V_x, stored internally on the AMU sampling capacitor, at the input of the S/H device (V_y). Only one cell of 256 cells on an AMU is shown. The AMUs are read in current readout mode in order to achieve an adequate signal rise time in the presence of the considerable parasitic capacitance of the output buses. The sampled voltage V_x is converted to a current I_x by an enhancement transistor in the AMU. The current is multiplexed onto Analog Out A and converted to a voltage by operational amplifier U1. Amplifier U2 insures that V_y is adjusted so that I_y equals I_x. The voltage V_y is therefore equal to the sampled signal V_x. The purpose of this output stage is to maximize the read-rate, to reduce the effect of changes of the supply voltage, and to compensate for the considerable temperature dependance [9] of the current from the transistors on

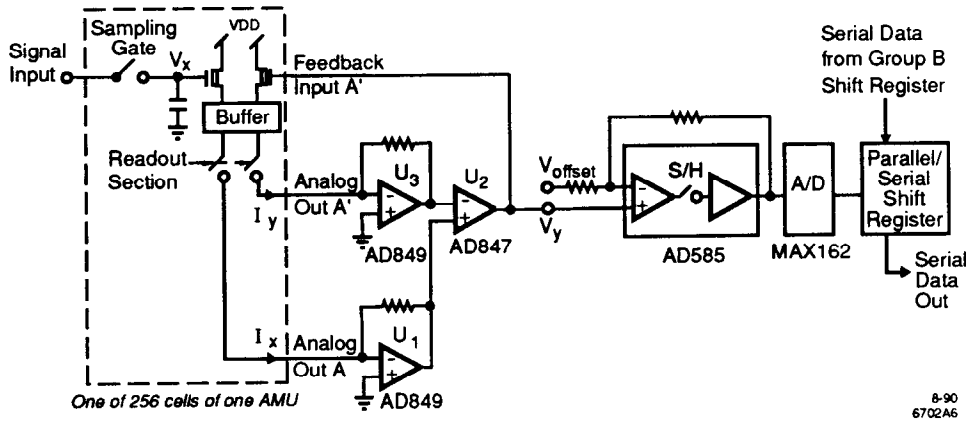

Fig. 6 Schematic of one of the two output stages on the motherboard. The outputs of 8 AMU chips are connected to one set of output buses. Shown is only one cell of one AMU.

the AMU. The performance [6] is superior to the circuit in reference 9, in which the feedback input is connected to a fixed voltage level.

In order to digitize the analog voltages while the output of U2 is settling, a S/H device is inserted into the pipeline. The signal at the output of the S/H is offset and gain adjusted to utilize the full input range of the 12-bit A/D converter. During each digitization cycle a pair of sequential cells located in different dies (groups A and B) are processed simultaneously. The digital information is then loaded in parallel into shift-registers (two 8-bit registers for each group) and read out in sequence at a rate of 8 Mbit/sec.

VI. Power Considerations

Most of the electronics on the motherboard is on pulsed power to reduce the heat load to the detector. The preamplifiers are turned on 400 μsec before the beams collide in the detector. The buffer and HAMU hybrids, and the ECL clock circuitry require less settling time and are powered 50 μsec before beam crossing. The power to the HAMUs and the buffers is switched by CMOS-level power-on signals from the ALTERA, which control via buffers and level translators (MAX627) the gates of surface-mount MTD3055 power switches. The negative supplies are switched by circuits comprising transistor packs. At the end of the write cycle the power is turned off and the sampled waveforms from the chamber are held in the powered-down HAMU hybrids. The RMS power for one motherboard is 3 W when operated at a 120 Hz beam interaction rate.

After a decision for readout, power is turned on for the S/H stages, the A/D converters and sequentially for the HAMUs on a board. The average readout rate for the SLD detector is 2 Hz which yields a RMS read power consumption of 1 W for each board.

The electrical energy for the five supply voltages is stored locally on 1000 μF capacitors which reduces the required current capacity of the power supplies and cables.

VII. Modes of Operation

There are several write modes which can be set by the controller [5]. In all these modes the power for the amplifiers, buffers, and HAMUs is turned on and the signals at the inputs of the HAMU are sampled and stored. In pulse calibration mode a strobe and various calibration voltages are applied to the preamplifier hybrid. In DC calibration mode the bias voltage at the input of the HAMU hybrid is stepped through the input range. In the leakage mode a strobe is applied to the leakage current sense boards, and in regular physics mode a 1.9 V bias voltage is applied to the HAMU and the chamber signal is stored in the HAMU. The length of the record is 512 cells $\times$ 8.4 nsec = 4.3 μsec, which defines the write cycle in normal data taking mode. In test mode using cosmic rays, data is written into the HAMU in a recirculating mode until a cosmic trigger stops the process, or up to the end of the cosmic ray write gate, which is set to 100 μsec.

In read mode the data in the HAMU is digitized and sent out as a serial bit stream. In the calibration pattern mode a stream of 64 data bits is sent to the amplifier hybrids to select the pattern of channels to be calibrated.

VIII. Construction of the Motherboards

The motherboard itself is a 13-layer blind-via board with two layers of surface-mount components on each side. The HAMU side (4 conductor layers, 2 ground planes, 1 power plane) is shielded from the preamplifier side (2 conductor layers, 2 ground planes, 1 power plane) by a shield layer. Only power connections, the amplifier output signals and the control lines from the EPLD to the amplifier side penetrate the whole board. The bulk of the signals are connected within each side utilizing blind via technology, which minimizes feed-through of digital signals to the amplifier side. The two sides of the 43 cm$\times$7 cm CDC curved motherboard with the first layer

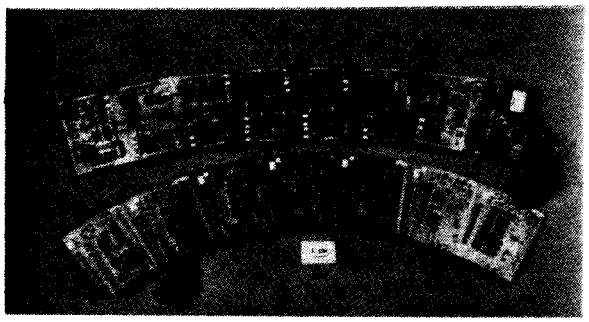

Fig. 7 Picture of the two sides of the central chamber motherboard with the first layer of components loaded (two different radii).

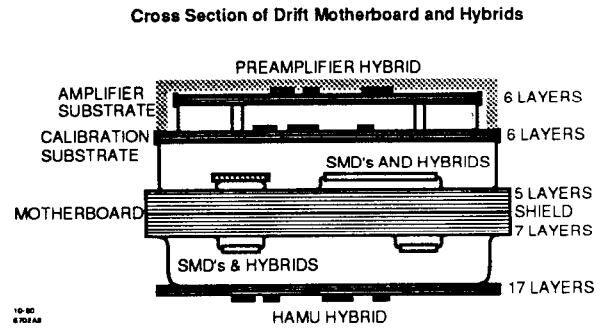

Fig. 9 Cross section of the CDC or EDC drift motherboard showing the two levels of surface mount components on both sides of the board.

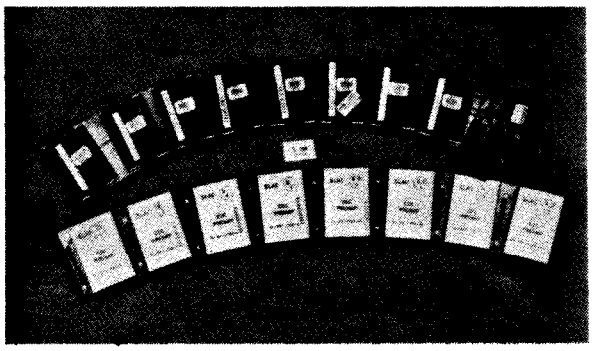

Fig. 8 Picture of the two sides of the CDC motherboard with the preamplifier and HAMU hybrids mounted on top of the first layer components (two different radii).

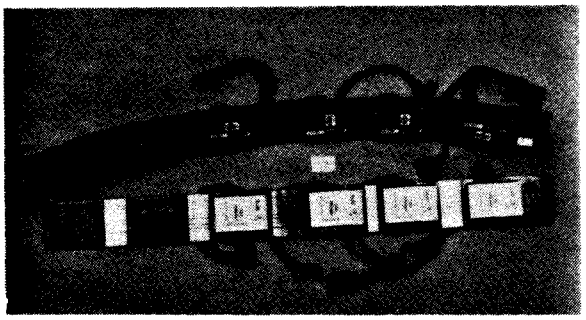

Fig. 10 Picture of the EDC mother board with four each of the large preamplifier and HAMU hybrids loaded. Shown are also the cable jumpers which connect the endcap chamber signals to the board.

of components loaded are shown in fig. 7. The boards are tested with a special test fixture before the preamplifier and HAMU hybrids are mounted on top of the smaller components as shown in fig. 8. The cross section of the drift motherboard is illustrated in fig. 9.

The motherboard for the endcap drift chambers are fabricated with a rigid-flex process to enable bending of the board around the endcap chambers. Figure 10 shows a picture of the 63 cm × 6.3 cm board with the rigid and flex sections. The board shown is only partially loaded with hybrids. To compensate for crosstalk in the six-wire drift cells the resistors are loaded between channels on the leakage current board (fig. 3).

IX. Summary

An electronic system is described which is mounted directly on the detector and processes drift chamber signals from low-level analog waveforms into serialized digital information. The signals are recorded as waveforms, which in the case of the central drift chamber, have a length of 512 buckets × 8.4 nsec = 4.3 μsec. Information from 5120 wires from each side of the central drift chamber is transformed into 85 streams of serial digital data. These are multiplexed again four-to-one and transmitted over optical links at a rate of 32 MHz from the detector to the counting house. All 170 central and most of the endcap drift chamber motherboards are tested and installed in the SLD detector.

Details of the performance, i.e., dynamic range, accuracy, stability etc., for the readout electronics of the Central Drift and Endcap Drift Chambers will be given in a separate paper [6].

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