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PERFORMANCE OF THE FRONT-END SIGNAL PROCESSING ELECTRONICS FOR THE DRIFT CHAMBERS OF THE STANFORD LARGE DETECTOR*

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Abstract

This paper reports on the performance of the front-end analog and digital signal processing electronics for the drift chambers of the Stanford Large Detector (SLD) detector at the Stanford Linear Collider. The electronics mounted on printed circuit boards include up to 64 channels of transimpedance amplification, analog sampling, A/D conversion, and associated control circuitry. Measurements of the time resolution, gain, noise, linearity, crosstalk, and stability of the readout electronics are described and presented. The expected contribution of the electronics to the relevant drift chamber measurement resolutions (i.e., timing and charge division) is given.

I. Introduction

The SLD experiment is designed to study electron-positron collisions at high energies [1-3]. The Central Drift Chamber (CDC) and the four Endcap Drift Chambers (EDC) comprise a major subsystem of the detector, whose purpose is to provide charged particle tracking and momentum measurement. The drift chambers provide three-dimensional track position information by means of layers of sense wires arranged in a vector cell geometry. Accurate measurement of the drift time should provide < 100 μm position resolution in the azimuthal coordinate for a CDC sense wire (< 200 μm for the EDC). The position along the wire is determined by stereo angle placement of groups of wire layers, although in the CDC, readout of both ends of the wires provides a redundant (but less accurate) measurement by charge division.

The signal-processing electronics for the drift chambers performs the functions of waveform sampling, wire hit triggering, control, and readout. Most of the electronics are located on multilayer printed circuit boards (motherboards) that are mounted on pins connected directly on the ends of the drift chamber sense wires. The 80 layers of sense wires in the CDC are arranged in ten concentric superlayers of vector cells, each cell consisting of eight sense wires. The CDC motherboards are connected to seven or eight adjacent cells in a superlayer, thus containing 56 or 64 channels for signal processing. Each EDC is arranged in three superlayers of cells, each cell having six sense wires. An EDC motherboard is connected to four, five, or six cells and thus processes up to 36 channels of sense wire signals.

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The overall organization, as well as more detailed descriptions of the drift chamber front-end signal processing electronics, are discussed in separate papers [4,5]. An overview of the signal processing chain is presented in the next section. The rest of this paper will examine the results of performance tests of the front-end electronics conducted primarily in the laboratory (e.g., inputs not connected to drift chamber sense wires). However, expected on-chamber performance will be discussed for relevant measurements. Results presented are from the CDC electronics, but in general are applicable to the nearly identical EDC electronics, if the lower sampling frequency for the EDC (one-half that of the CDC) is taken into account.

II. Electronics Overview and Description of the Test Setup

A simplified schematic overview of the performance test setup is shown in Fig. 1. The front-end signal processing chain up to the optical fiber digital data link are production versions of a CDC motherboard, controller, and transition board. While the final SLD drift chamber system will utilize a FASTBUS control and digital readout acquisition system, the tests reported here use a CAMAC prototype system under control of a microVAX 3100. Owing to the optical decoupling of the data and control signals, and to the use of identical control and timing signals, the performance results from the CAMAC-based system should be identical to the final FASTBUS system.

The signal arriving from a drift chamber sense wire enters the input of the transimpedance amplifier. This amplifier has a gain of 1 V/20 μA and a risetime of 8 ns. For each channel, a calibration circuit can be used to inject a programmable amount of charge into the amplifier for test purposes. A second circuit connected to the amplifier input can be enabled to measure the leakage current (due to corona, wire damage, or aging effects) on the sense wire. At the output of the amplifier the signal is split. One path sends the signal to the opposite side of the motherboard for waveform sampling. The other path sends the signal into a variable threshold discriminator circuit that provides a fast signal for charged track triggering. One bit of wire-hit data is stored for each channel, then the data from all channels on the motherboard is serially transmitted off the board for further multiplexing and transmission, via optical fiber, to the trigger and data acquisition system.

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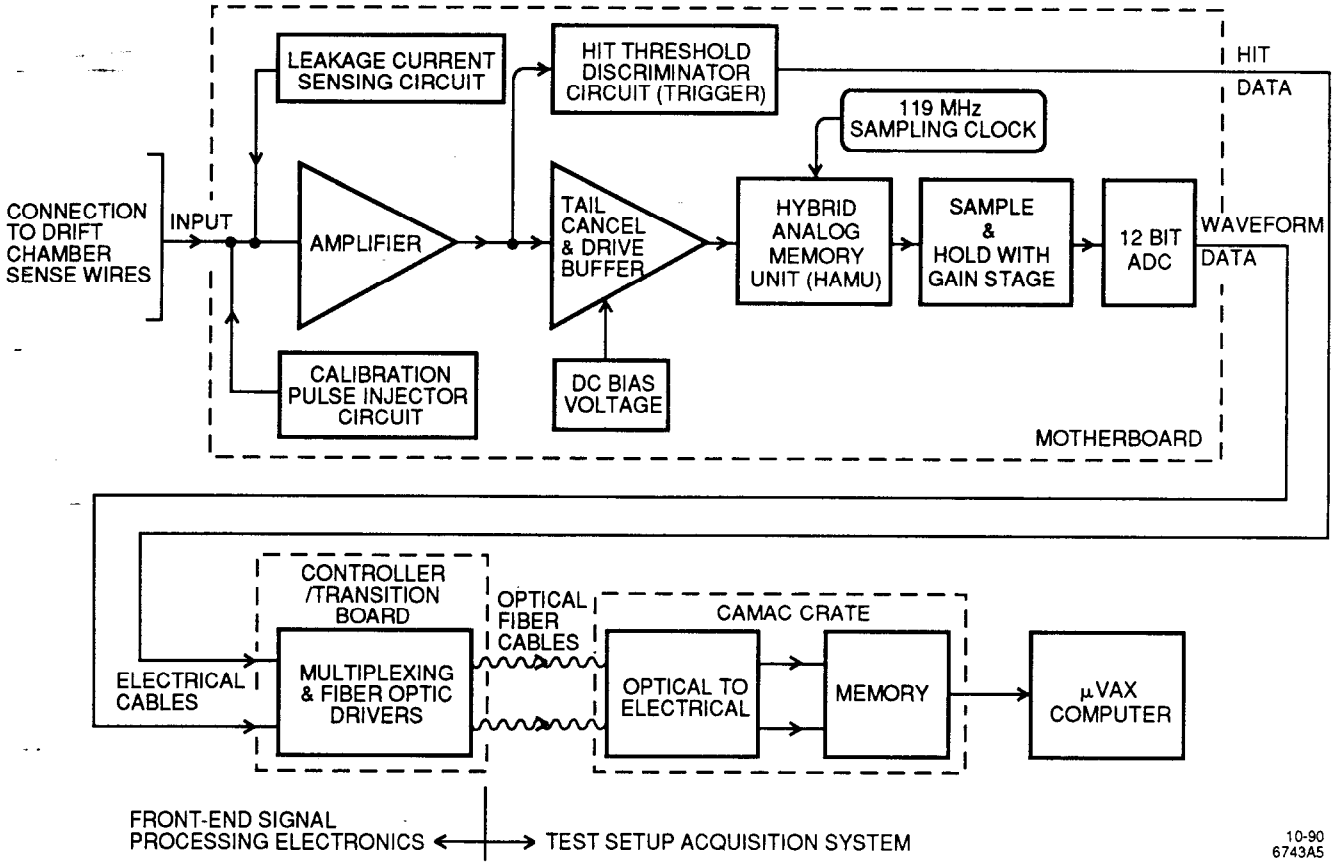

Fig. 1 Signal path for a single readout channel of the front-end electronics.

The analog signal sent for waveform sampling is processed by a unity gain buffer that provides additional current drive, pulse tail cancellation (to improve double pulse resolution), and a DC bias voltage offset. The DC bias is needed by the Hybrid Analog Memory Unit (HAMU) which follows the buffer. In the HAMU, the waveform is sampled and stored as charge in 512 time "buckets" of 8.4 ns duration (i.e., 119 MHz clock frequency). This waveform memory is continually overwritten for every beam crossing (i.e., at the SLC machine repetition rate of 120 Hz) until a triggered event occurs. Then the analog memory is serially read out into a sample-and-hold (S/H) device. The S/H has a gain stage that allows the output range of the HAMU to be matched to the 0 to 5 V input range of the 12-bit A/D converter (ADC). The digitized data is serially transmitted at 8 MHz to the controller/transition board for multiplexing and conversion to fiber optic signals.

A raw waveform processed by this system is shown Fig. 2(a). The calibration circuit has been used to inject a pulse into the amplifier. The baseline variations from bucket to bucket are mostly due to the different offsets of the buckets [6]. To correct for the different bucket gains and offsets, an extensive calibration procedure has been defined. This procedure, a piecewise linear interpolation algorithm, divides the range of the ADC into eight equal segments and then determines the gain and offset needed for each segment and for each bucket. The result is nine calibration constants per bucket needed to do the correction.

If one applies this calibration procedure to the uncalibrated waveform of Fig. 2(a) one obtains the corrected waveform in Fig. 2(b). Application of the calibration constants converts the vertical scale from ADC counts to volts, as measured at the input to the HAMU. To give an indication of the scale, the calibration pulse seen in the waveform corresponds to that expected for a "typical" pulse; i.e., equivalent to the average charge expected for a minimum ionizing particle (MIP) at the midpoint along the length of a sense wire (half the charge to each wire end). This 1/2 MIP charge is equal to 0.3 picocoulomb (pC) at the input of the amplifier, and will be used from now on as a standard reference charge.

III. Timing Resolution

The most critical function of the drift chamber subsystem is to provide high-precision drift distance measurements. This requires that the electronics have sufficient time resolution so as not to contribute significantly to the inherent drift time resolution of the chambers. The CDC design goal of better than 100 μm resolution

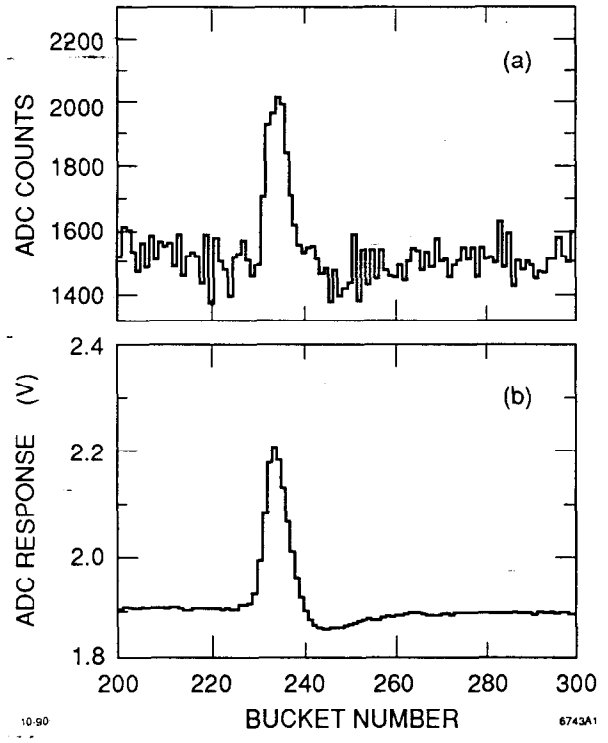

Fig. 2 (a) A raw (uncalibrated) waveform for a typical channel, and (b) the same waveform after applying the calibration procedure. For clarity, only 100 of the 512 time buckets are shown.

implies an electronics contribution of less than 50 μm, which translates to about 6 ns for the expected drift velocity.

In the final system, the drift time will be determined from the digitized waveform, using a software algorithm which will determine a time and charge for each pulse found. Since we are only concerned here with the effect of the electronics, a simple threshold requirement on the leading edge of a pulse is used to determine the pulse arrival time. A pulse generator is used to inject a large amount of charge at a random time during the 4.3 μs (512 x 8.4 ns) live-time window. A 2 ns least count TDC is used to time the interval between the start of the live-time window and the arrival of the pulse. This is compared to the time interval determined from the threshold requirement, applied to the digitized waveform. The RMS of the time interval difference is 2.6 ± 0.2 ns. This value is consistent with the value expected from the measurement resolution alone (2.5 ns—mostly due to the waveform sampling-frequency) showing that the electronics has no significant resolution degrading effects (such as time jitter).

Note that for pulses with very low signal-to-noise, time resolution can be degraded, since any leading edge finder could have problems both with noise fluctuations and with time slewing of the rising edge. This issue will be discussed further in Section V.

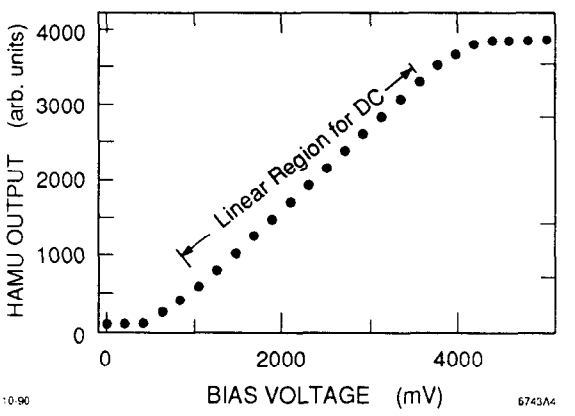

Fig. 3 Response of a single HAMU time bucket as a function of input DC bias voltage. Only the indicated linear region is used in the final system.

IV. Gain and Dynamic Range

There are two main gain stages in the system; the first is the amplifier gain and the second is the gain of the S/H stage at the input to the ADC. The amplifier gain is chosen to match the expected range of chamber pulse heights to the dynamic range of the HAMU. The full dynamic range of the HAMU is obtained by varying the DC bias level at its input, and is shown in Fig. 3. It has sensitivity starting at 500 mV going to about 4 V before saturation occurs. However, the regions below 1.0 V and above 3.5 V are too nonlinear for use in our implementation. The offset and gain of the S/H stage is chosen so that the range corresponding to 1.0 to 3.5 V at the HAMU input is mapped into the 0 to 5 V range of the 12 bit ADC input. Thus, one ADC count corresponds to 0.6 mV at the input of the HAMU. In spite of the good linearity for DC levels, the linearity of the HAMU for pulses (AC linearity) is found to be less than desired for low bias values (discussed further in Section VI). This and edge effects reduce the effective range at the input of the HAMU to be between 1.9 and 3.4 V.

The amplifier gain is such that a standard 1/2 MIP charge should give a pulse height of about 300 mV. If the particle is at the extreme end of a wire, the near-end amplifier will see nearly 1 MIP or 600 mV in pulse height. The dynamic range of 1.5 V therefore allows for pulse height fluctuations of up to 2.5 times the average. Only a negligible fraction of pulses will exceed this range.

The gain of the amplifier, when read out through the full waveform sampling system, is determined by injecting a known charge into the amplifier input. After application of the calibration procedure on the waveform, the total charge of a pulse is measured by integrating all buckets above the baseline. This gain factor is 5500 mV-buckets per picocoulomb (pC). Thus, charge measurements can be expressed in picocoulombs at the amplifier input. However, pulse height measurements and single bucket noise will be measured in volts referred to the HAMU input.

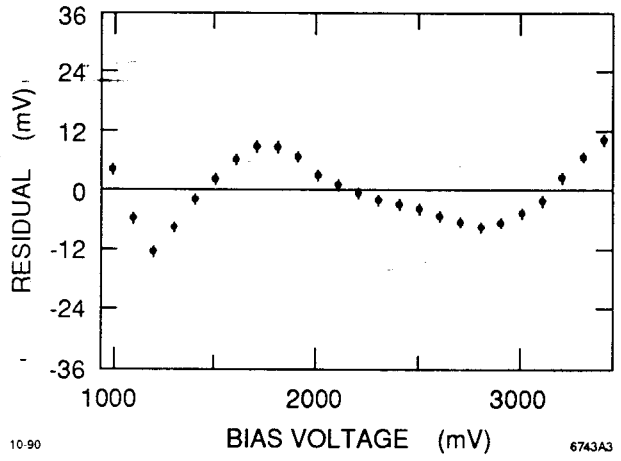

Fig. 4 Residuals from a linear fit for a typical single bucket response as a function of input DC bias voltage.

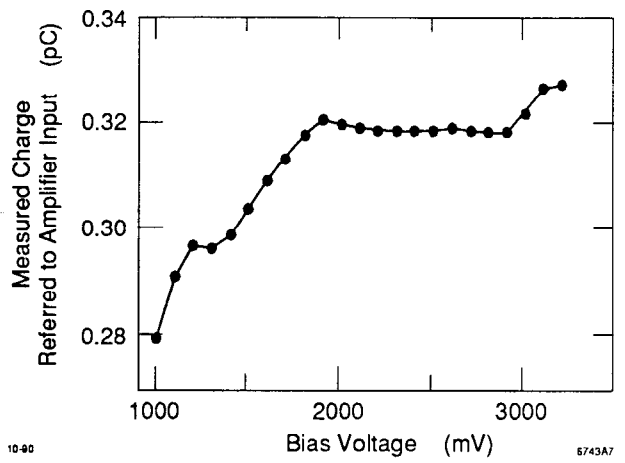

Fig. 5 Measured charge integral for the same injected charge as a function of input bias voltage. Each point is an average of four channels. The range of flat response starting at 1.9 V and above indicates the region of good AC (pulse) linearity used in the final system.

V. Noise and Expected Signals

Single bucket noise is defined as the RMS variation in the readout value of a bucket. When the amplifier input load impedance is 10 KΩ (i.e., not connected to a sense wire), the noise is on average 1.1 mV and is very consistent from bucket to bucket for all buckets in all motherboards. When the input load consists of a 300 Ω resistor in series with the input of another amplifier input (simulating the two-ended readout on a CDC sense wire), this noise increases to 2.4 mV (this is consistent with preliminary measurements on the CDC). The bucket noise is a major factor in determining the effective signal-to-noise ratio in order to find the leading edge of a pulse. However, one must also take into account the variations from bucket to bucket due to the inability of the calibration procedure to produce a perfectly flat baseline. Studies of this effect show bucket height variations with an RMS from 0.5 to 2.0 mV depending on the applied bias offset and the exact method of calibration. These variations are mostly due to nonlinearities in bucket gain. Since this is less than the expected bucket noise performance on the CDC, it should not be of major concern.

From chamber pulse studies it was concluded that bucket noise levels up to about 2% of a 1/2 MIP peak pulse height have no significant effect on pulse arrival time resolution [7]. For this system, that noise level corresponds to 6 mV at the amplifier output, so that the expected bucket noise of 2.4 mV should not adversely affect the timing resolution.

The noise figure of merit for the total charge measurement of a pulse depends on the pulse width. The typical expected pulse width is about 135 ns, or 16 HAMU buckets. The measured pulse noise for 16 buckets is 1.5 femtocoulombs (fC) with a 10 KΩ input load. The expected noise for on-chamber performance is 3.0 fC. The charge division resolution is about 1.4 times the relative charge measurement error (relative to the total charge summed over both wire ends). For a 1 MIP charge (0.6 pC), this implies that the noise will contribute a charge division resolution error of 0.7% of the 1.8 meter wire length. The final charge division resolution can also be strongly influenced by the linearity which is discussed in the next section.

VI. Linearity and Charge Division Resolution

As was mentioned in Section III, the DC linearity of the HAMU is quite good. The residuals from a linear fit are shown for a typical bucket in Fig. 4. The average residual is on the order of 5 mV for a full range of 2.5 V. Note that this is without calibration. If one uses the calibration correction, the residuals can be kept to about 2 mV, or less than 0.1%. However, the response of the HAMU to fast pulses (the AC linearity) is not linear for input voltages below 1.9 V. A clear indication of the problem below 1.9 V input bias is shown in Fig. 5 where the measured charge integral for the same 1/2 MIP calibration pulse is plotted as a function of the HAMU input voltage bias. From 1.0 to 1.8 V bias the measured charge increases until a plateau is reached at 1.9 V. Finally, at about 3.1 V the pulse peak enters the saturation region where the nonlinearity causes the calibration correction to overestimate the charge. It is possible that the region below 1.9 V could be used if one is willing to do an extensive AC calibration. However, this may not be sufficient since the frequency dependence of the calibration could imply the corrections are pulse shape dependent. Such corrections could be too difficult for practical purposes.

By restricting the usable range to above 1.9 V, the measured charge integral linearity exceeds the 0.5% design requirements. The average residual from a linear fit is 0.1% of the total 1 MIP charge. This is much smaller

Table I
Typical matrix for channel-to-channel crosstalk (A) within the same cell, and (B) between adjacent cells.
All numbers are in percent of the charge in the pulsed channel.
Measurement error is ±0.1%, and the variation from cell to cell is ±0.1%.

Pulsed Channel	(A) Readout Channel 1	2	3	4	5	6	7	8
1		5.6	0.0	0.2	0.0	-0.2	0.0	-0.1
2	4.6		5.7	0.1	0.0	-0.2	-0.1	-0.1
3	-0.2	4.7		5.7	0.1	-0.2	-0.2	-0.3
4	-0.2	-0.3	4.9		5.6	-0.2	-0.2	-0.3
5	-0.2	-0.2	-0.1	5.2		5.2	0.1	0.0
6	-0.3	-0.2	-0.1	0.1	5.0		5.7	0.0
7	-0.2	-0.2	-0.3	0.0	0.0	4.8		5.5
8	-0.2	-0.2	-0.3	0.0	-0.1	-0.2	4.8	

Pulsed Channel	(B) Readout Channel in Adjacent Cell 1	2	3	4	5	6	7	8
1	-0.3	-0.1	-0.1	0.0	-0.1	0.0	0.0	0.0
2	-0.6	-0.2	-0.1	-0.1	-0.1	-0.1	0.0	-0.1
3	-0.5	-0.5	-0.1	-0.1	0.0	0.0	0.0	0.0
4	-0.3	-0.6	-0.3	-0.1	-0.1	0.0	0.0	-0.1
5	-0.1	-0.1	-0.1	-0.1	-0.2	-0.3	-0.4	-0.2
6	-0.1	-0.1	-0.1	-0.1	-0.1	-0.2	-0.4	-0.3
7	-0.1	-0.1	-0.2	-0.1	-0.1	-0.1	-0.3	-0.5
8	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.1	-0.3

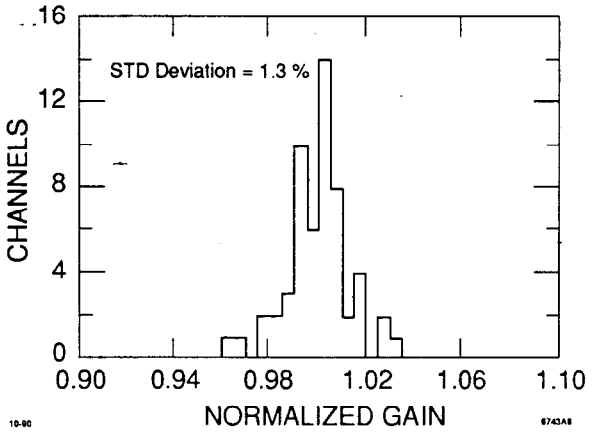

Fig. 6 Variation in integral charge gain for the 56 channels of a typical seven-cell CDC motherboard.

than the measurement error due to noise of 0.5%. However, since the charge measured by two different electronics channels determine the charge division measurement, the gains of the two channels must also be precisely known. The channel-to-channel variations in gain for one motherboard are shown in Fig. 6. This distribution has an RMS of 1.3%, and is mostly due to the different AC gains of HAMU channels. The pulse calibration circuits of the amplifier were trimmed to be within 0.5% of each other. The HAMU gain variations can therefore be corrected to that level through a simple pulse gain calibration.

The total contribution of the electronics to the charge division resolution is on the order of 1% of the wire length. This exceeds the design goal of 2 to 5% resolution [8]. The charge division measurement will be used primarily to reduce the iterations needed for track pattern recognition. The modest design goal is due to the fact that the stereo angle measurement should ultimately provide a resolution of better than 0.2% of the wire length.

VII. Crosstalk

The measured electronic crosstalk is summarized in Table I. The crosstalk matrix for the eight channels within a cell is shown in Table I(A) and the crosstalk matrix for the channels of neighboring cells is shown in Table I(B). The approximately 5% crosstalk to nearest neighbor channels within a cell is intentional. Five percent crosstalk compensation is designed into the amplifier, since earlier chamber studies revealed sizeable opposite sign crosstalk of about 5% to nearest-neighbor sense wires. Except for the intentional crosstalk compensation, there is no other case of channel-to-channel crosstalk within the same cell or to adjacent cells, exceeding 1% of the main pulse. There is no measurable crosstalk (i.e., $< 0.1\%$) from channels that are further away than the neighboring cells.

Large channel-to-channel crosstalk could lead to substantial errors both in the time and in the charge measurements. More recent chamber studies showed larger amounts of crosstalk between sense wires than initially measured, especially in the EDC. This led to an additional compensation network for the EDC electronics [5]. For the CDC, the approximately 2% uncompensated crosstalk is considered acceptable. The effect of the small (unintentional) electronic crosstalk should therefore be negligible compared to the remaining uncompensated chamber crosstalk.

VIII. Further Results

The average drift of the signal output of a motherboard channel referred to the HAMU input is less than 1 mV over a period of one day. The stability of the charge integral is measured to be the same to within 0.2% of the standard 1/2 MIP charge over a similar time period. This assumes a stable ($< \pm 1°C$) environmental temperature. Under these conditions, one calibration run per day is sufficient to achieve the accuracy required of the electronics. The temperature dependence of the system is measured to be 1.3 mV/°C referred to the HAMU input, independent of the HAMU input bias level. This translates to 0.43%/°C of the standard charge measurement.

The leakage current sensing circuit at the input of the amplifier, when a special strobe is applied [5], injects a small current into the amplifier that is proportional to the leakage current on the wire. This results in a DC shift in the waveform with a magnitude of 30 mV per μA of leakage current. A sensitivity of less than 100 nA should therefore be possible. This diagnostic tool is intended to help locate problem (noisy or damaged) wires or cells.

The discriminator threshold circuit which receives one of the analog outputs of the amplifier is designed to provide hit information for each end of each sense wire. The design goal was to be able to trigger with a threshold level equivalent to 1/5 of a standard 1/2 MIP charge. This translates to approximately 60 mV at the output of the amplifier. The lowest threshold level for which the discriminator fires less than 1% of the time is considered to be the minimum triggering threshold for that channel. The average minimum threshold for all of the channels on a board is typically less than 10 mV. More important, however, is the fact that although a single D/A converter supplies the common threshold for all channels on a board, there are offsets in effective thresholds of up to 20 mV. Nevertheless, the performance of this circuit is adequate to provide a noise-free triggering threshold of less than 60 mV.

IX. Conclusion

Performance tests of the front-end signal processing electronics for the drift chambers indicate that the primary design goals of good timing resolution and good charge division resolution have been achieved. For large signals, the timing resolution is 2.6 ns and is dominated by the inherent resolution of the sampling frequency. The good signal-to-noise ratio and the fast risetime of the amplifier should prevent any loss of timing resolution due to the electronics. The range of the system for good linearity of fast pulses is about 1.5 V at the input of the HAMU, which corresponds to five times the MIP pulse-height for a track at the midpoint of a wire. The ADC least count is 0.6 mV, or about 0.2% of the MIP pulse-height. Bucket noise is 1.1 mV without an input load, and 2.4 mV with the equivalent chamber load. Noise for the charge integral measurement for a MIP is expected to be 0.5% for each wire end. The signal-to-noise ratio, combined with the good pulse linearity, should permit a charge division resolution of about 1% of the wire length, provided that the channel-to-channel gain variation is accounted for. Electronic channel-to-channel crosstalk is less than 1%. Both the leakage current sensing circuit and the discriminator (trigger) circuits display adequate performance.

Acknowledgments

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