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PERFORMANCE MEASUREMENTS OF HYBRID PIN DIODE ARRAYS*

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ABSTRACT

We report on the successful effort to develop hybrid PIN diode arrays and to demonstrate their potential as components of vertex detectors. Hybrid pixel arrays have been fabricated by the Hughes Aircraft Co. by bump bonding readout chips developed by Hughes to an array of PIN diodes manufactured by Micron Semiconductor Inc. These hybrid pixel arrays were constructed in two configurations. One array format having 10×64 pixels, each 120 μm square, and the other format having 256×256 pixels, each 30 μm square. In both cases, the thickness of the PIN diode layer is 300 μm.

Measurements of detector performance show that excellent position resolution can be achieved by interpolation. By determining the centroid of the charge cloud which spreads charge into a number of neighboring pixels, a spatial resolution of a few microns has been attained. The noise has been measured to be about 300 electrons (rms) at room temperature, as expected from KTC and dark current considerations, yielding a signal-to-noise ratio of about 100 for minimum ionizing particles.

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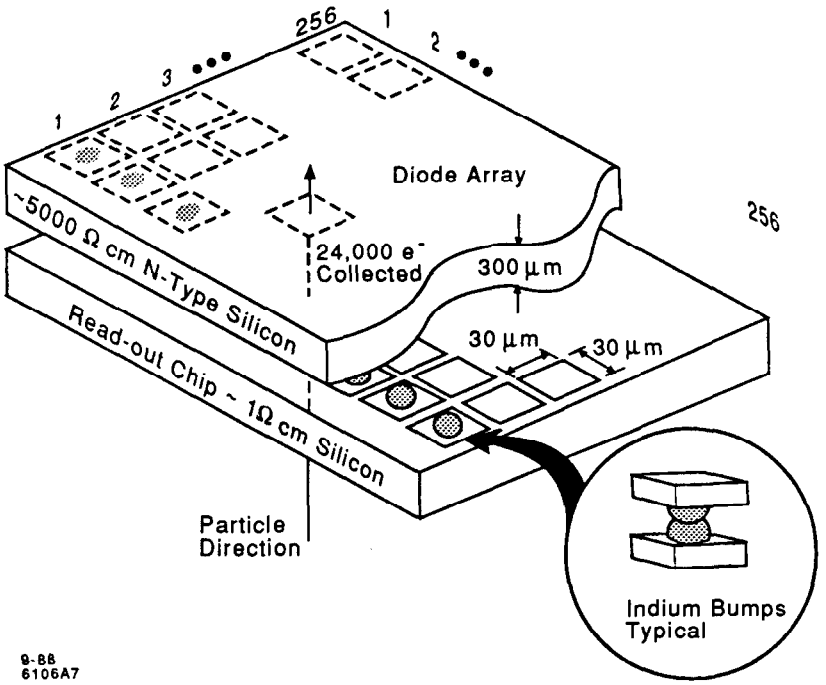

Fig. 1: Schematic representation of a Silicon PIN Diode hybrid detector.

INTRODUCTION

An architecture well suited for charged particle detection at the SSC is that of a hybrid.[1–3] The charged particle detector and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips, indium bump bonded together, then provide the basic building block for the construction of a detector array.

The choice of the hybrid design (viz., one in which each diode of the detector array is bonded to an independent amplifier readout circuit on a mating VLSI chip via an array of aligned indium metal bumps that cold-weld under pressure to form ohmic contact), allows for additional flexibility in the selection of detector and readout electronics.[4] For instance, a change in the leakage current specification of the detector array will not affect the readout electronics, nor will a change in the VLSI chip oxide thickness to accommodate a radiation hardness specification affect the detector array. Figure 1 is a schematic representation of a silicon PIN diode array hybrid.

SILICON HYBRID ARRAYS

Development of hybrid vertex detectors has been the goal of the authors since late 1984. To this end, two hybrid arrays have been designed and fabricated. The sensor arrays were fabricated by Micron Semiconductor and the readout arrays by Hughes Aircraft. The indium bump bonding was done by Hughes with bumps measuring under 15 μm in diameter. The properties of the two arrays are described in Table 1.

Figure 2 is a schematic diagram of the MOSFET circuit of the 10×64 readout array. The diagram has been divided into its several functional portions. The section replicated for each pixel contains four MOSFETs. Signal charge is generated by the detector diode, and is fed to the gate of the signal MOSFET where it stays until a readout is made. The pixel selection circuit indicates how a sequence of address lines can select an individual pixel by turning on the gates of the V_{DD} bias MOSFET and

Table 1. Summary of Device Parameters

Array dimension	10 × 64	256 × 256
Pixel size	120 μm	30 μm
Detector material	Silicon	Silicon
Number of readout channels	10	2
Power during "write" cycle	0 mW	0 mW
Power during read cycle	10 mW	2 mW
Present clock speed	1 MHz	2 MHz
Theoretical clock speed	10 MHz	10 MHz
Readout mode	Random access	Random access
Processing power	20 MIPS/channel	20 MIPS/channel
Radiation hardness	1 Mrad	?
Noise at room temperature	<300 e^- rms	<300 e^- rms

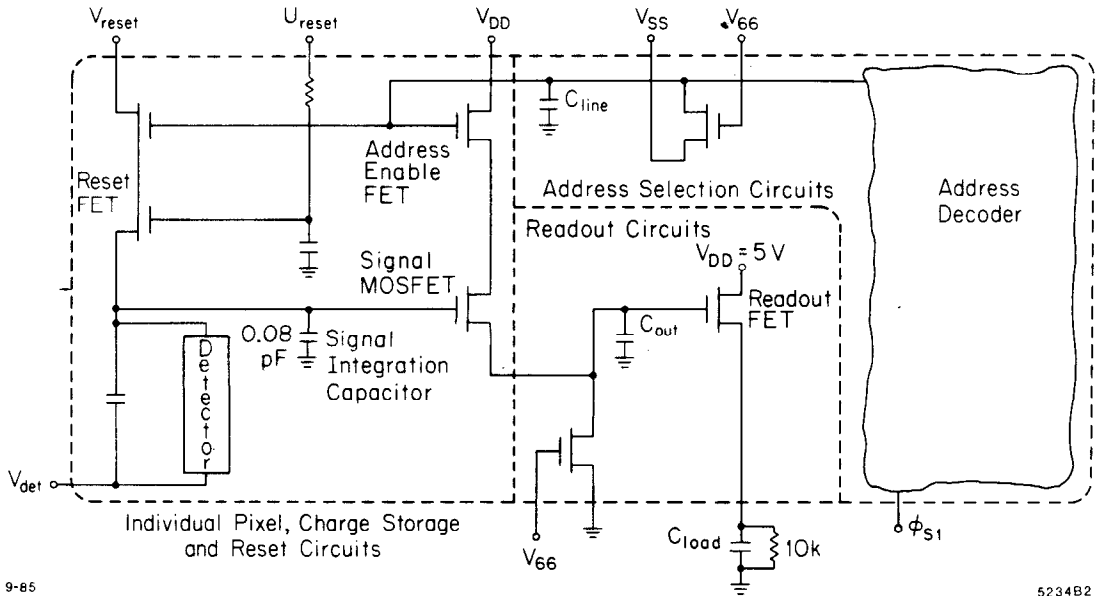

Fig. 2: Schematic drawing of the readout electronics of the 10 × 64 readout array.

the enable gate of the reset MOSFET. The U_{reset} signal allows the gate of the signal MOSFET to be reset to the V_{reset} level for any pixel that is enabled by the reset MOSFET. All of the signal MOSFETs in a column of the array are connected to a readout MOSFET in a source follower configuration which provides power for driving an external circuit.

The present readout chips allow random access to any pixel, which then operates as an independent detector. By virtue of its geometry alone, each pixel detector (PIN diode) provides about 3000 times less sensitivity to diode leakage current than a microstrip detector, which will increase the radiation hardness to neutrons. To complement this increase in the radiation hardness of the detector diode, the readout chips can be fabricated in a technology which is radiation hard to 1 Mrad of ^{27}Co gamma rays at cryogenic temperatures.

The two readout chips are similar, but have some differences. The 10 × 64 array has a random access architecture in that a unique setting of its address lines will select one and only one row of pixels. The 256 × 256 array, on the other hand, is random

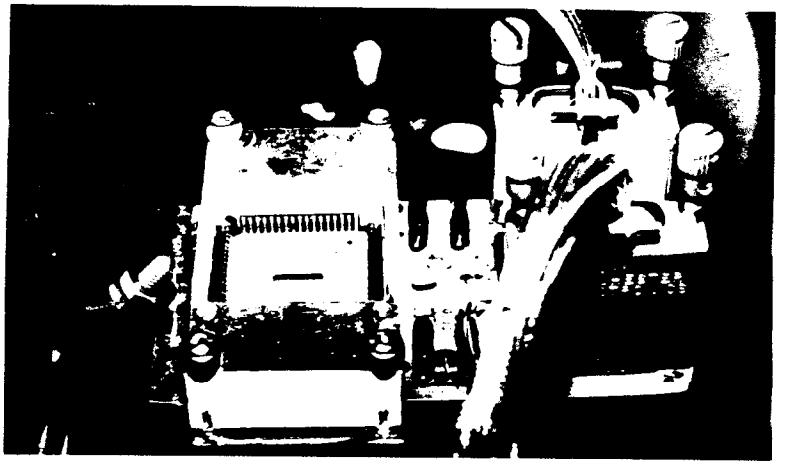

Fig. 3: A photograph of the 10 × 64 Silicon PIN Diode Hybrid in its mount in the laboratory.

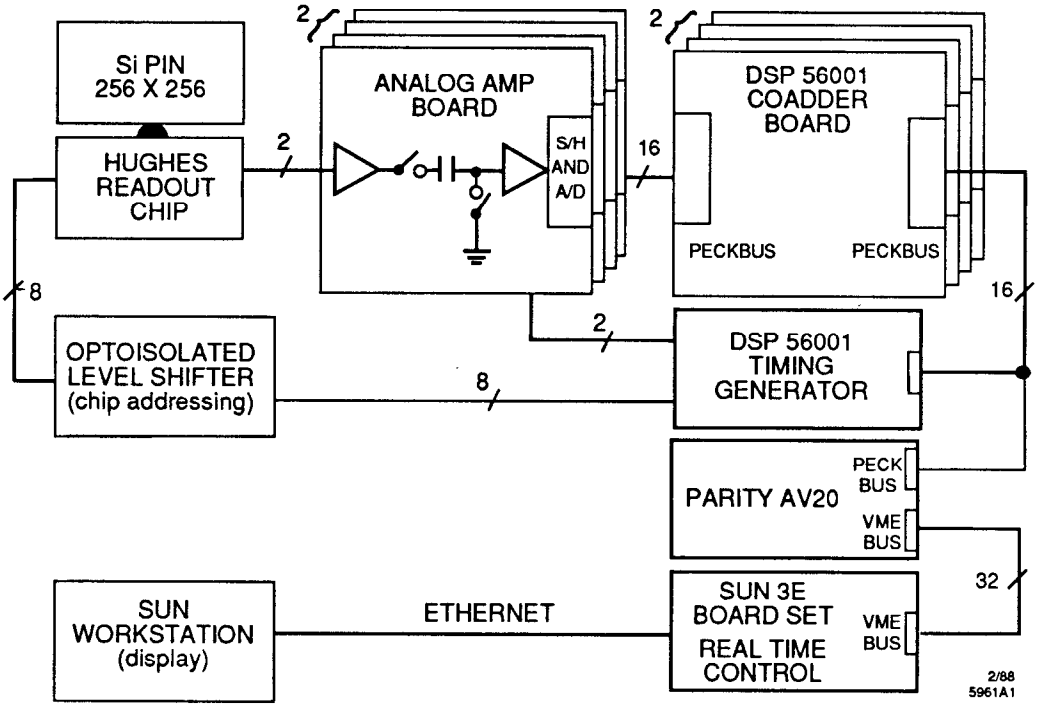

Fig. 4: A block diagram of the High Energy Physics readout and display electronics.

access in that the pixels are addressed via row and column shift registers. This feature makes addressing a given pixel more complicated but allows easy implementation of a sparse scan algorithm. This particular readout chip has been optimized to collect electrons but is bipolar at the signal levels we expect.

DESCRIPTION OF PRESENT HARDWARE

Figure 3 is a photograph of the 10 × 64 array in its mount in the laboratory. Figure 4 is a block diagram of the high energy physics data acquisition system. This system, used to read out the 256 × 256 array, is more modern and more up-to-date than the system described in Ref. 2 on which the 10 × 64 data described in this paper were taken. A Sun Microsystems Sun–3/110LC–4 workstation controls a system housing

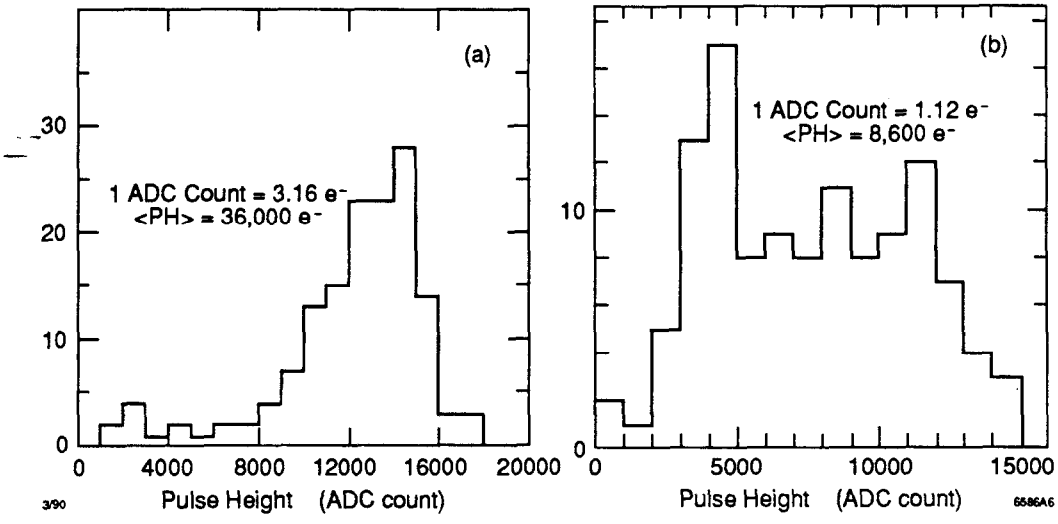

Fig. 5: (a) The pulse height spectrum of the alpha data; and (b) the pulse height spectrum of the beta data.

a Sun 3/E CPU, a Motorola 68020 bus converter board, amplifiers, ADCs, digital signal processors, and a clock generator. The digital signal processor is the Motorola DSP56001. This device acquires data at a rate of 10 MIPS, processes it, and passes it, via the MC68020 to the Sun 3/E. The bus converter board, a Parity systems AV20 dual port processor, interfaces the local analog bus (PECKBUS) to the VME bus.

Detector development funds were used to begin the fabrication of the dedicated high energy physics data acquisition system described above. The amplifier/ADC/ DSP56001 boards and the clock generator in the present system, however, are circuits remaining from the infrared data acquisition system. These need to be redesigned to high energy physics criteria.

A data acquisition and display software package based on the previous system has been written. The operating system is UNIX, the DSP has been programmed in assembly language, and various control functions are written in Magic/L, an interactive language derived from Forth. The Parity AV20 dual port processor has been programmed in C, and the DSP will be reprogrammed in C.

RADIOACTIVE SOURCE TESTING OF THE ARRAYS

Testing of the 10 × 64 hybrid array started in mid-September 1989 at the Space Sciences Laboratory in Berkeley while testing of the 256 × 256 array started in December 1989 at Hughes Aircraft, Carlsbad.

A ^{106}Ru beta source and an ^{241}Am alpha source were used to irradiate the 10×64 array. Spectra for both alphas and betas were obtained, and the data are presented in Fig. 5. From this data, we roughly calculate both the signal in the hit pixels and the noise in the surrounding pixels. We have verified that both signal and noise agree with models of the readout electronics.

In our geometry, particles enter the device on the cathode of the PIN diode, the side farthest from the bump bonds. Thus, much of the charge collected must drift across the entire depletion distance of 300 μm. The charge cloud, spread by scattering of the initial radiation and by diffusion, will have a finite lateral size. If a particle were closer to the edge of a pixel than to the center, one would expect charge to be shared by adjacent pixels. On average, we see charge spread over 9 pixels; a 3 × 3 array.

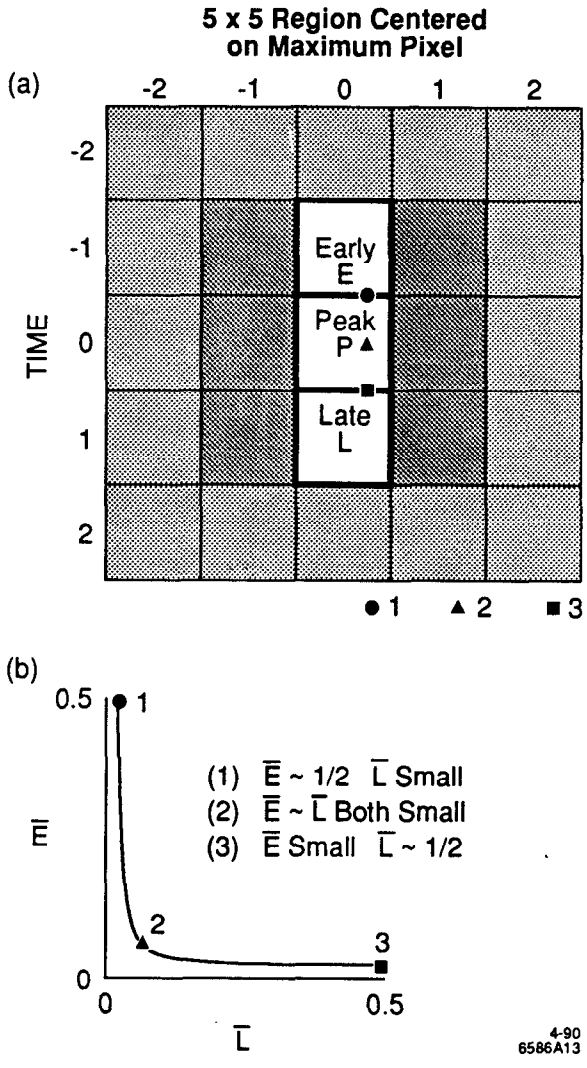

Fig. 6: (a) A schematic of a 5 × 5 pixel region centered on a particle hit; and (b) a schematic plot of the $\overline{E}$ versus $\overline{L}$ planes indicating the result of various hypothetical incident positions of a particle within the central pixel.

A detailed analysis of a set of pixels near a particle hit allows the calculation of four quantities: signal-to-noise, noise, size of the charge cloud, and spatial resolution. In Fig. 6(a), a schematic of a 5×5 region centered on a particle hit is shown. The pixel with the maximum signal is located at $(0,0)$ is labelled "$PEAK$" and the pulse height of its signal referred to as P. Nearby pixels are located by offsets between -2 and $+2$. Each pixel in the 5×5 region has its zero set by analyzing other frames of data wherein there have been no particle hits in its vicinity. Further, in analyzing a particular hit, an average of the outer boarder of 16 pixels is subtracted from the inner 9 pixels to remove any systematic offset which arises because of the separation in time between the measurement of the background frame and the frame containing the particle hit. The direction of time in Fig. 6(a) refers to the sequence of the readout of the pixels. In this device, columns are read out in parallel, thus, the five pixels in the row labeled -2 at the top of the figure are readout first, with sequential readout, by row, from -2 to $+2$ on the time axis. For convenience, the pixel just above the $PEAK$ is labelled "$EARLY$," and its contents referred to as E, while the pixel just below the $PEAK$ is labelled "$LATE$," and its contents referred to as L.

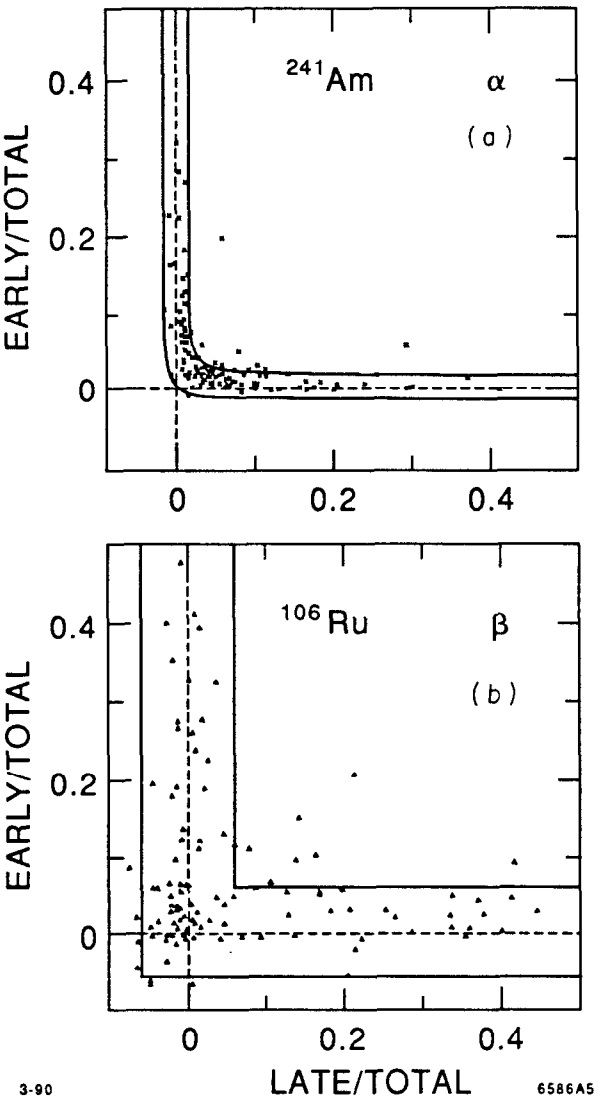

Fig. 7: Scatterplots of the charge sharing for alpha and beta radiation incident on the 10×64 array. The $\pm 2\sigma$ limits are shown on the solid lines.

E, P, and L are used to derive the $\overline{E}$ and $\overline{L}$ ratios from the relation:

$$\overline{E} = E/(E+P+L) \qquad \text{and} \qquad \overline{L} = L/(E+P+L) \quad .$$

Figure 6(b), a schematic plot in the $\overline{E}$ versus $\overline{L}$ plane of what should happen if a particle were to hit different parts of the central pixel. Possibilities 1, 2, and 3 are indicated in the central pixel, with their corresponding results shown in Fig. 6(b). The position of possibility 2 will be close to or far from the origin depending on the size of the charge cloud.

Figure 7 shows the $\overline{E}$ or $EARLY/TOTAL$ versus $\overline{L}$ or $LATE/TOTAL$ scatterplots for the alpha and beta data. The trend of the data to fall near the axes, as explained schematically by Fig. 6(b), is as expected. The difference in the two cases is dominated by the somewhat larger charge cloud generated by the alphas compared to the betas. If one uses the measured signal to noise of the total charge deposited by a particle hit, one can derive the expected deviations from perfect correlation in the $\overline{E}$ versus $\overline{L}$ plane. The $\pm 2\sigma$ limit curves for the alpha and beta data are shown in Fig. 7. Note that the data scatter approximately as expected. These curves are not fits to the data shown, but are instead predicted from the signal-to-noise ratio only.

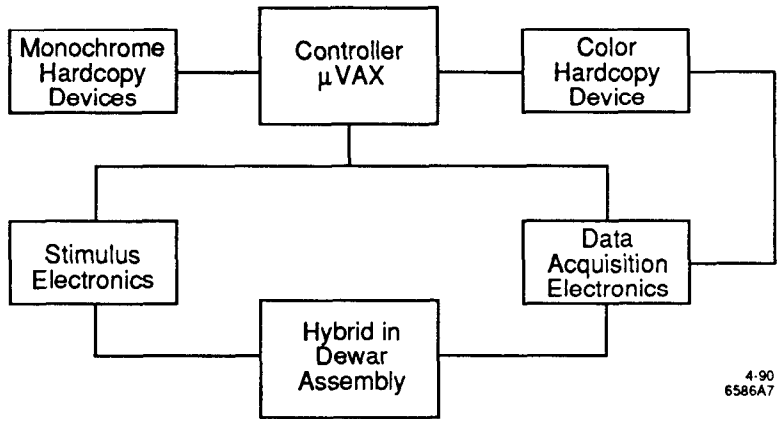

Fig. 8: A block diagram of the Hughes/Carlsbad readout system.

In Fig. 7, the data points near the ends of the L-shaped locus of points represent data which have no charge deposition in either the $LATE$ or $EARLY$ pixel. Thus, the variance of these data is a measure of the fluctuation of the ratio of the signal of a typical nonhit pixel and the total signal from the three pixels in a hit column. This variance is the inverse of the average signal-to-noise ratio. For this analysis, the variance of $\overline{E}$ for data where $\overline{L} \geq 0.25$, and the variance of $\overline{L}$ for data where $\overline{E} \geq 0.25$ is used. The signal-to-noise ratio for the beta sample from this variance is about 36. The same analysis for the alpha data set yields a signal-to-noise ratio of 113. The mean signal size for the betas is about 8,600 electrons, while that for the alphas is 36,000. Thus, the two independent measurements of noise yield 239 and 319 electrons, respectively, for the beta and the alpha data. The error in making this measurement is not statistical, but is dominated by systematic errors, estimated to be at the 20% level. Thus, for both alphas and betas, the noise measurement corresponds to about 300 electrons (rms).

The noise measurements are somewhat higher than a calculation of KTC noise and dark current noise, which are the dominant sources of noise at room temperature. For our devices, these are 110 electrons (rms) and 120 electrons (rms), respectively yielding a combined noise of 165 electrons (rms). We attribute this extra noise to the external electronics, and expect that it can be removed by better calibration and filtering. We have, however, achieved our goal of 300 electrons (rms) at room temperature.

From the ratio of the number of data points which lie near the axes and the number of data points in the cluster near the origin, one can determine the average size of the charge cloud produced by an incident charged particle. For betas, this size is 19 μm (1σ) and for alphas this size is 28 μm (1σ), assuming a two-dimensional Gaussian profile.

To determine the spatial resolution, one uses the fact that the cluster of data points near the origin corresponds to events which deposit nearly all of their charge in the central pixel. Thus, within this region, no interpolation is possible. For those events which are near the edge of a pixel, one can use the variance noted earlier to estimate the error in the position within the pixel. For the betas which strike within 30 μm of an edge, the centroid of the 19 μm distribution can be located to within about 2 μm. A similar result for the alphas is 2–3 μm across the entire 120 μm pixel, due to the larger size of the alpha-induced charge cloud.

Preliminary testing of the 256×256 array has been started in the test laboratory of Hughes Aircraft in Carlsbad, California. Figure 8 is a block diagram of the readout

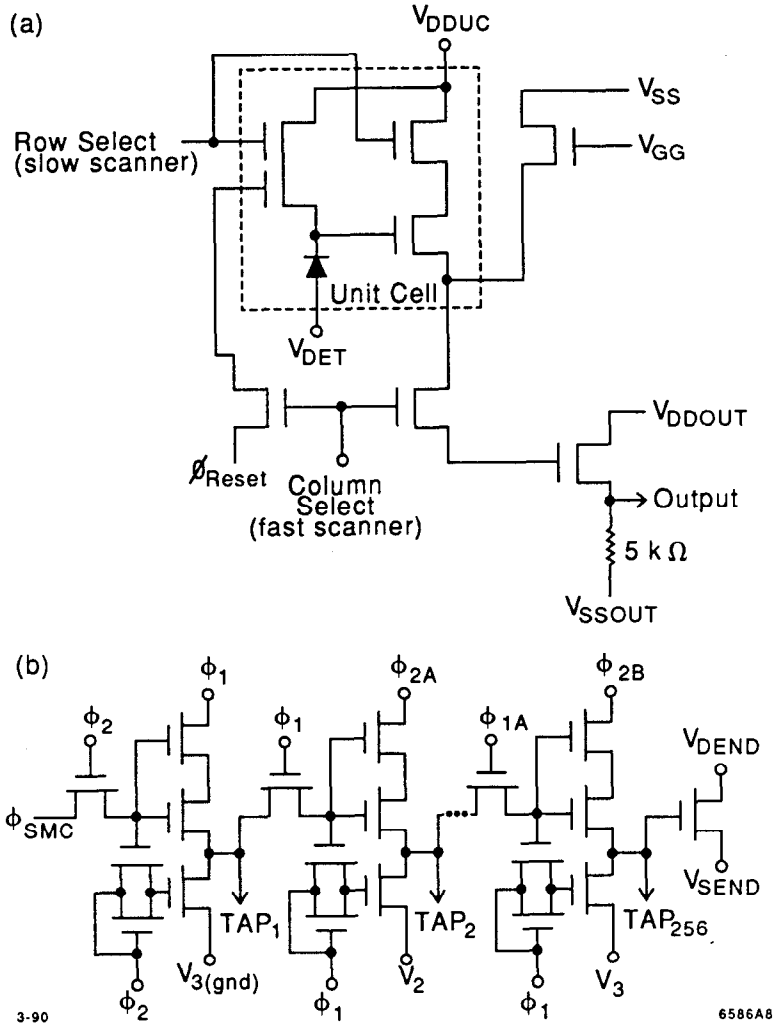

Fig. 9: (a) A schematic diagram of the MOSFET circuit of one cell of the 256 × 256 array; and (b) a schematic diagram of the six transistor slow scanner.

system used. The hybrid, mounted in a 68 pin leadless chip carrier, is mounted in a Dewar on a pc card having an amplifier gain of 2.5. DC power, and clock stimuli are provided by a general purpose test station designed and fabricated by the Hughes Technology Center. This station has emphasized flexibility over high data rate. A DEC Workstation II (μVax) is used to control the data acquisition and stimulus electronics. Data reduction, evaluation and storage codes have been developed. Data is acquired at a 60 Hz frame rate, resulting in a 500 ns pixel read time. The system employs low noise, high bandwidth drive electronics, with tunable rise and fall times for the clock pulses. Voltages are maintained with a resolution of 0.5 mV.

To acquire the data, acquisition and gain electronics is interfaced to a TRAPIX 5500 imaging system supplied by Recognition Concepts. This electronics features adjustable gains from times 1/4 to times 64, and adjustable offsets with very low noise, 8 MHz, track and hold circuitry. A 12 bit, 10 MHz, A/D converter is interfaced to the Q bus of a μVax processor. Digital data is displayed in real time on the high resolution color monitor, and is stored on hard disk. By using the array processing capabilities of the TRAPIX 5500, events with signal levels only a few mV above the read-noise level may be detected in real time.

Figure 9(a) is a schematic diagram of the MOSFET circuit of one cell of the 256 × 256 array, and Fig. 9(b) is a schematic of the six transistor slow shift register.

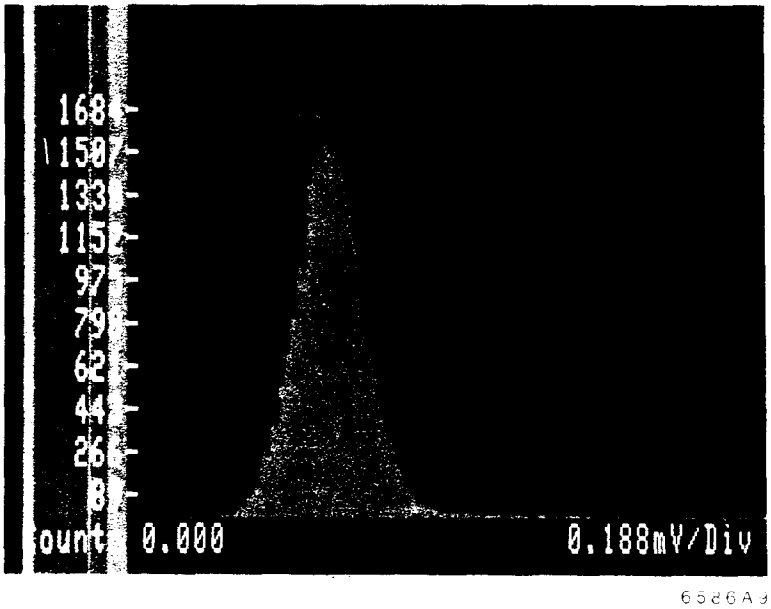

Fig. 10: A noise spectrum of the 256 × 256 array at 200 °K.

The fast shift register enjoys the same circuit configuration, but has transistors of slightly different geometry.

The bulk of the preliminary data on this hybrid was taken at 200 °K. The hybrid evidenced dark current at room temperature at twenty times the expected level. Rather than wait for a new hybrid, it was felt that characterizing the existing chip, cold, would be more instructive.

Figure 10 is a measurement of the noise for this hybrid at 200 °K. Sixteen frames of data were taken and a pixel by pixel average taken at the normal frame rate of 60 Hz. The data displays the average pulse height at the output of the chip in mV. The truncated mean is about 3.5 divisions at 0.188 mV/div. Using a pixel capacitance of 40 fF, one calculates the noise to be 165 electrons (rms) at this temperature. KTC noise is about 65 electrons (rms) and the dark current is negligible at these temperatures. This data was taken with no double-correlated sampling techniques used, thus, other sources of noise such as $1/f$ noise will remain in the measurement.

The array was exposed to radiation from a ^{207}Bi source. This provides a source of 1 MeV electrons, which directly give a measurement of the signal to be expected from minimum ionizing particles. Figure 11 is a spectrum of the radiation from the Bismuth source. The 1 MeV electrons will result in 24,000 electron hole pairs (channel 1000 in Fig. 11) if they transit the PIN diode detector array normally. However, due to multiple coulomb scattering they will certainly not do this, but rather will exit the bottom of the array after scattering through an angle of about 38 degrees, and going through about 380 μm of material. This will result in an average pulse height of about 30,000 electrons (channel 1200).

The explanation for the pulse height distribution which occurs below channel 1,000 is found in the myriad of gamma rays which also are produced by the Bismuth source. For every 100 Bismuth decays, one gets 9–1 MeV electrons; but one also gets: 100–574 KeV gammas, 75–1 MeV gammas, 75–(70–90) KeV gammas, and 30–(10–13) KeV gammas. When all of these gamma rays are multiplied by their respective conversion probabilities in 300 μm of silicon, one observes that for every 100 Bismuth decays one sees: 1 event from the 175 high-energy photons, 9 events from the 1 MeV electrons,

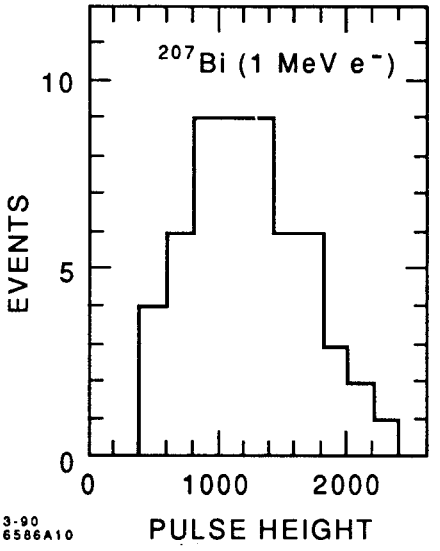

Fig. 11: The pulse height spectrum measured using the 256 × 256 array when irradiated by a ^{207}Bi source, emitting 1 MeV electrons, and a number of gamma rays.

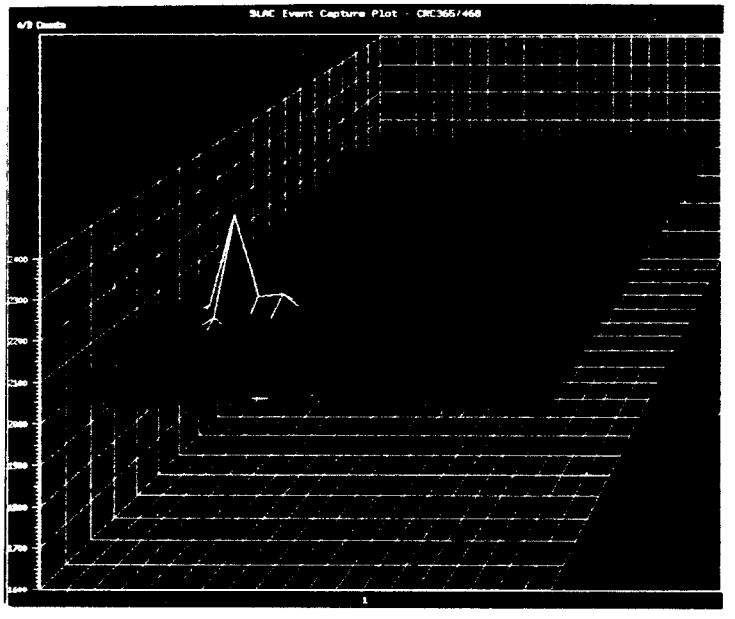

Fig. 12: A three-dimensional plot of a 1 MeV electron being detected by the 256 × 256 array.

and 10 events from the 70–90 KeV photons. There are no events recorded from the low-energy photons, as we set a threshold of about 6,250 electrons for this data set. Figure 12 is a three-dimensional plot of a characteristic minimum ionizing particle event. Figure 13 is a photograph of a 256 × 256 silicon PIN diode hybrid similar to the one used for these measurements.

SUMMARY OF RESULTS

Room-temperature operation of the 10 × 64 arrays has been demonstrated with noise levels less than 300 electrons (rms). Charged particles have been detected and imaged using this array with excellent signal to noise, and a preliminary measurement of 2–3 μm spatial resolution has been achieved. A measurement of the noise in the

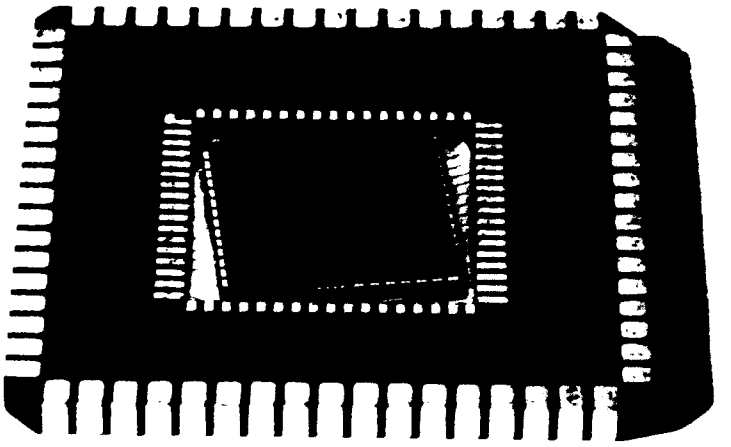

Fig. 13: A photograph of a 256 x 256 silicon hybrid similar to the one used in these measurements.

256 x 256 array has been made at 200 °K, and found to be about 165 electrons (rms). Charged particles have been detected and imaged and pulse heights consistent with those expected have been achieved.

REFERENCES

1. S. Shapiro and T. Walker, "The Microdiode Array—A New Hybrid Detector," SLD New Detector Note No. 122 (1984).
2. S. Shapiro, W. Dunwoodie, J. Arens, J. Gernigan, and S. Gaalema, "Silicon PIN Diode Array Hybrids for Charged Particle Detection," *Nucl. Instrum. Methods* **A275**:580 (1989).
3. S. Gaalema, G. Kramer S. L. Shapiro, W. Dunwoodie, J. Arens, and J. G. Jernigan, "Silicon PIN Diode Hybrid Arrays for Charged Particle Detection: Building Blocks for Vertex Detectors at the SSC," *Proc. Int. Industrial Symposium on the Supercollider,* 1989, New Orleans, LA, p. 173.
4. S. Gaalema, "Low Noise Random-Access Readout Technique for Large PIN Detector Arrays," *IEEE Trans. on Nucl. Sci.* **NS–32**, No. 1:417 (1985).