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A STATUS REPORT ON THE SLD DATA ACQUISITION SYSTEM*†

THE SLD COLLABORATION

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ABSTRACT

The basic design of the SLD data acquisition system and its present status are reviewed. Aspects of the design that take particular advantage of the relatively low e^+e^- cross section and the low beam crossing rate of a linear collider are explained.

INTRODUCTION

The SLD is an e^+e^- detector optimized for Z^0 physics at the Stanford Linear Collider (SLC). It is being built by an international collaboration [1] and should be complete in late 1989. The SLD has been described in previous overview papers [2] and more completely in the SLD Design Report [3].

The detector is shown schematically in Figs. 1 and 2. Charged particle tracking and momentum measurement are provided by a CCD vertex detector and high precision drift chambers in a 0.6 T magnetic field. Particles are identified by Čerenkov Ring Imaging Detectors (CRID's). Total energy measurement is provided by a Liquid Argon Calorimeter (LAC) located inside the magnet solenoid. The LAC has sections for both electromagnetic and hadronic energy measurements. Hadronic shower tails from the LAC are measured in the Warm Iron Calorimeter (WIC), which consists of limited streamer mode tubes in the laminated iron of the magnet flux return. The WIC streamer tubes have pad readout for calorimetry and strip readout for muon tracking. All of the systems (except the vertex detector) are implemented as cylindrical central sections with endcaps that utilize the same technology. A photograph of the present state of the detector is shown in Fig. 3. The detector has been rotated to accept the LAC which is visible in the foreground.

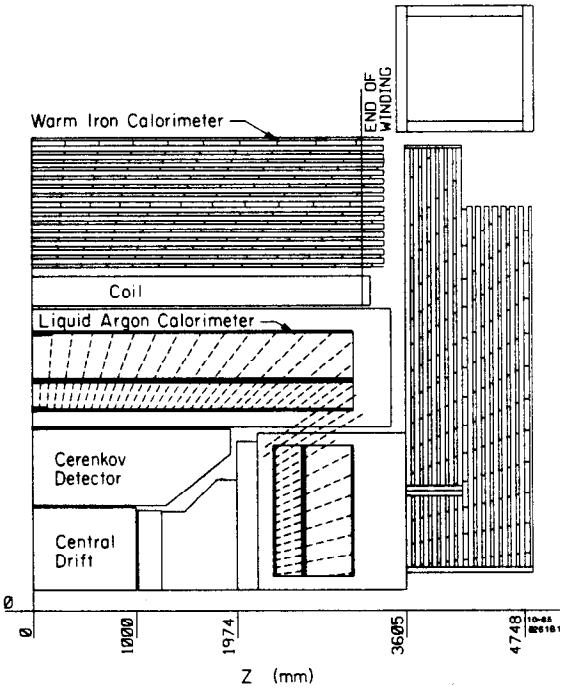

Fig. 1. Quadrant view of SLD.

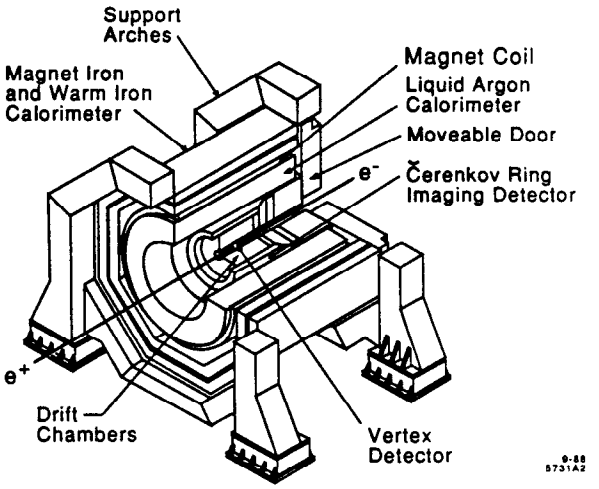

Fig. 2. Isometric cut-away drawing of SLD.

Fig. 3. Photograph of SLD in the SLC Collider Hall. The detector has been rotated 90° to swallow the LAC, visible in the foreground.

The $e^+e^- \rightarrow Z^0$ cross section is sufficiently small that the trigger rate will be dominated by beam background. This rate is expected to be less than 1–2 Hz, so that event acquisition times of 50–100 ms will result in acceptable dead time. The beam crossing rate in SLC will be 120 Hz (180 Hz is possible in a future machine upgrade) giving 8.3 ms for trigger data acquisition and processing. These rates make data acquisition and triggering much easier than in hadronic colliders and invite extensively time multiplexed system designs. A generic block diagram is shown in Fig. 4a and the generic organization of the preamplifier is shown in Fig. 4b. For each live beam crossing, detector signals are amplified, shaped, and stored in analog form awaiting relatively slow readout. For the drift chambers and the CRID's, 512 wave form points are stored on Analog Memory Unit [4] (AMU) chips. The AMU is a custom VLSI NMOS array of 256 sample-and-hold circuits for fast write, slow read waveform capture. Another custom integrated circuit, the Calorimetry Data Unit [5] (CDU), is employed in the calorimeter, where the base line and signal peak of each channel are measured. In the vertex detector, the scheme is essentially the same, except that the order of analog storage and amplification

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† Presented by M. Breidenbach.

is reversed with the CCD's. The WIC strip readout stores a discriminated signal digitally.

After the fast write cycle, the data are multiplexed from the AMU's and CDU's and digitized by local ADC's. The serialized digital data stream is transmitted by optical fibers to FASTBUS modules for data correction and compaction, and to Aleph Event Builders (AEB's) [6] for further data organization before transmission to the host computer. The full FASTBUS organization is shown in Fig. 5. Synchronization of the data acquisition is provided by a Timing and Control Module (TCM) for each subsystem.

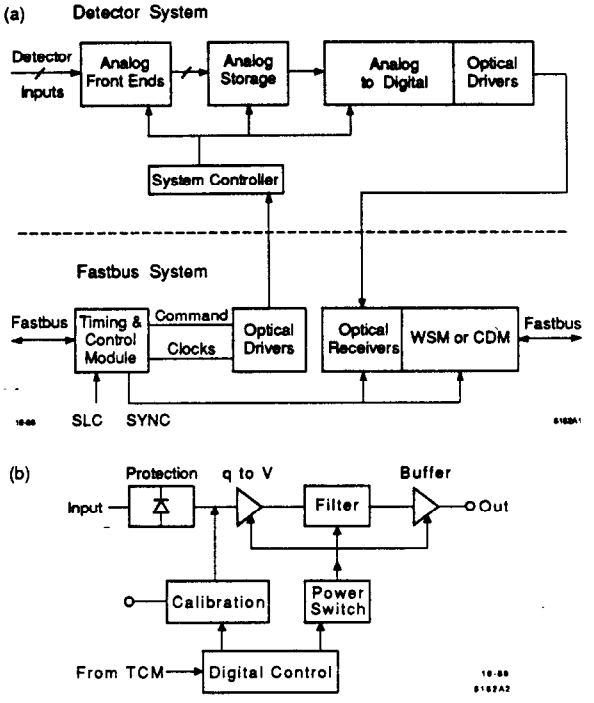

Fig. 4. a) "Generic" block diagram of the SLD data acquisition systems. b) "Generic" organization of a preamplifier.

The complimentary design consideration to the timing of the e^+e^- collider is the benign radiation environment, again in contrast to high luminosity hadron colliders. On the scale of radiation damage to electronics, there is no significant dose at reasonable angles from beam-beam interactions; the synchrotron radiation from the final bends and quadrupoles is controlled by masking (which is required for the drift chambers and CRID's in any case); and the machine backgrounds are controlled by upstream collimation and shielding (again, these backgrounds would prevent detector operation before radiation damage to electronics was important). Consequently, it is possible to locate electronics in and on the detector to improve performance and minimize cable plants which are often unwieldy in large modern detectors. The preamplification and data capture circuitry has been physically integrated with the SLD detectors, so that, for example, the drift chamber and LAC electronics mount directly on the detector feedthrough pins and only the channel multiplexed, serial digital data stream on optical fibers emerges from the detector. This has the advantage of requiring only a small cable plant with small apertures in the angular coverage, but it does require careful thermal management and attention to reliability because of limited access to the electronics. Again, the time structure of SLC helps with the thermal management — most of the electronics is power pulsed with a 10% duty cycle, and the remaining heat is taken out by radiation and convection to water cooled surfaces. The reliability

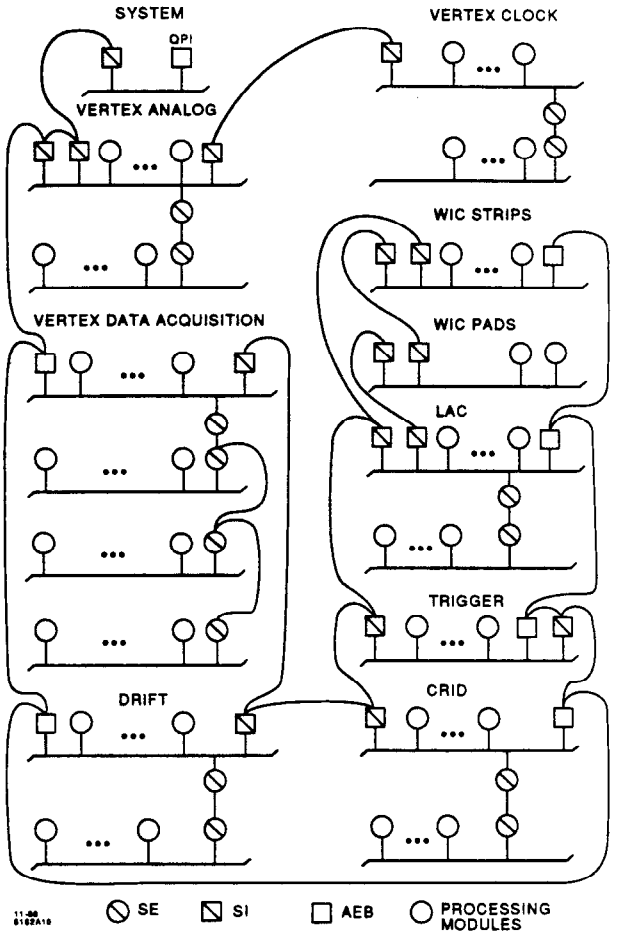

Fig. 5. Organization for the SLD FASTBUS system.

problem is addressed in two ways: the first is an effort to minimize interconnections by developing VLSI and hybrid analog front end circuits with multiplexed outputs. These parts are burned in before acceptance. The second major approach is to limit the number of channels which can be affected by a single point failure. For example, power pulsing is associated with each preamplifier hybrid rather than a board or larger grouping, and power supplies are external and accessible. Additionally, critical control and timing signals have redundant physical paths which can be selected from the Timing and Control Module.

Another requirement of this instrumentation strategy is that the electronics be physically small to economically utilize expensive detector volume. SLD has approximately 13,000 channels of charge division wave form sampling electronics for the drift chambers, 16,000 similar channels for the CRID, 50,000 channels of calorimeter readout, 110,000 channels of WIC strip readout, and 260 CCD channels. Fitting all of this electronics into the desired small spaces has required constant attention: The analog storage circuits are implemented in VLSI and packaged in hybrids, the preamps are hybridized, and there is reasonably dense use of surface mount devices.

The FASTBUS system is located in an enclosure on top of the detector since SLD is self-shielded. There are 18 crates in 7 racks cooled by water-to-air heat exchangers. High and low voltage power supplies are located in racks atop the SLD support arches adjacent to the cable penetrations.

One major change has occurred in the architecture of the data acquisition system: the slow output of the AMU's and CDU's was to be transmitted to the FASTBUS system as an analog signal on optical fibers. The analog transmission proved

to be difficult and has been replaced with digitization by 12 bit 3 μsec CMOS ADC's on the detector. The digitized data are then interlaced on an optical fiber at 32 Mbaud.

SUBSYSTEM DESIGNS

Vertex Detector

The vertex detector utilizes Charge Coupled Devices (CCD's) giving two-dimensional position resolution for charged tracks of about 5 μm, so that relatively unambiguous track association in a dense jet is straightforward. However, the good space point performance comes with relatively expensive devices that are slow to read because about a quarter million pixels are processed through a single serial port. In addition, the CCD is ungated and does not have a viable fast clear. Nevertheless, the CCD's are extremely attractive in the e^+e^- collider environment because the small beam pipe permits a vertex detector with a total sensitive area of only a few hundred cm^2; the CCD's can be sufficiently cleared by shifting rows in the 2 ms before beam crossings; the background produced by beam crossings subsequent to a SLD trigger can be suppressed while CCD's are being readout (by changing the SLC linac phase for a sector near the end of the machine so the beams are stopped by energy defining collimators); and finally because the CCD readout cycle can be completed in roughly 50 ms consistent with the detector dead time goals.

The vertex detector consists of 4 coaxial cylinders of CCD "ladders" arranged about the beampipe with the inner cylinder at a radius of 18.5 mm. The basic arrangement is shown schematically in Fig. 6a. Each ladder consists of 6 or 8 CCD's bonded to a thin ceramic substrate with wire bonded electrical connections to the substrate. The organization of the electronics is sketched in Fig. 6b. Each CCD has about 220,000 22 μm square pixels that are serially read out following a trigger; each CCD has a separate readout channel and each ladder has a separate set of clock drivers. The preamplifiers and the column clock drivers are located adjacent to the CCD assembly; the row clocks are relatively slow and are driven from FASTBUS modules. The amplified signals are averaged by a 4 section transversal filter and digitized. Signal enhancement is performed by two dimensional clustering using a semi-custom gate array chip.

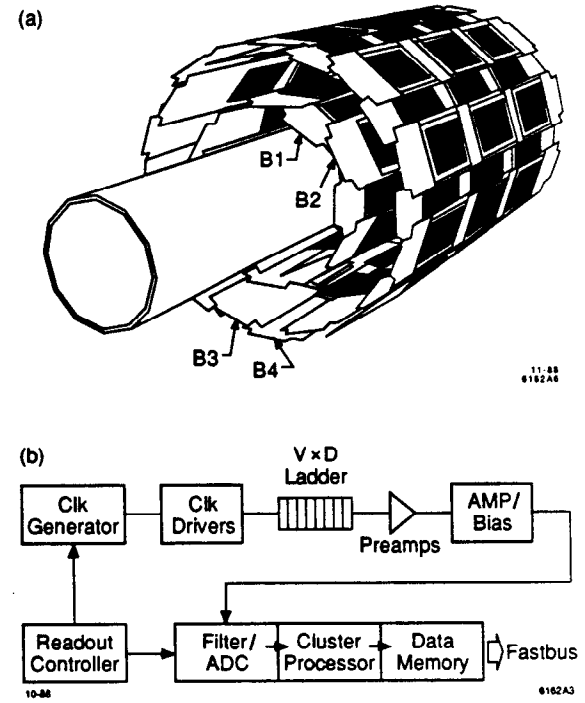

Fig. 6. a) Schematic view of the vertex detector. b) Block diagram of the CCD data acquisition.

Tracking System

The central drift chamber consists of 80 layers of sense wires arranged in 10 superlayers of vector cells with a total of 5120 wires. Wave form sampling readout is employed on both ends to permit accurate determination of drift times, charge division z measurement, and dE/dx measurement for $e-\pi$ separation. The 4 endcap drift chambers have an additional 1812 sense wires. The central drift chamber is now being strung, and the end cap chambers are complete.

The heart of the drift chamber electronics is a set of "motherboards" that conform to the superlayer structure of the chambers. A typical board is shown in Fig. 7; there are 38 variants of this board for the central chamber, accommodating 6 or 8 cells, 10 different radii of curvature, and two ends. Eight-channel preamplifier [7] hybrids are mounted on the drift chamber side of the motherboard, above analogous sets of PC boards for the high voltage distribution. The preamps also have discriminators on each channel driving a serial shift register to provide drift chamber trigger data, which is required since the AMU readout cycle takes 64 ms. This is the only trigger specific data channel for the detector. As indicated in Fig. 4b, the preamp hybrids also have power pulsing and charge calibration circuitry. The 8 preamp outputs go through the board to AMU hybrids containing 16 AMU chips, which provides 512 waveform samples per channel. An 8 sense wire cell with preamp and AMU hybrids occupies an area of about 25 cm^2. Pairs of AMU's are interlaced and sample every 8.4 ns. If there is a trigger, the AMU's are clocked out at 2 MHz to a pair of sample-and-holds and ADC's on the motherboard. A set of controller boards distributes write and read clock signals as well as calibration, trigger threshold, and control signals. The controller board also houses the optical drivers; 256 sense wires are multiplexed onto each fiber. The power consumption of the system on the chamber is about 60 mW per channel.

Fig. 7. Photograph of a drift chamber motherboard.

CRID

The CRID focuses Čerenkov light from liquid and gas radiators on either side of a large area photon detector. The photon detector is a quartz box filled with a carrier gas and a small concentration of TMAE, an organic molecule that is easily photo-ionized. The resulting electrons are drifted by a carefully controlled electric field to a set of proportional wire chambers that give 3 axis measurements of the photon conversion position and thus the angle of the Čerenkov radiation.

The architecture of the CRID readout is identical to the drift chamber system except that the trigger circuits are omitted. However, the preamp [8] must contend with the very large dynamic range (60 db) caused by the avalanche fluctuations from the single photo electron signals; it must have low noise to permit 1% $\Delta\ell/\ell$ charge division from a 10 cm long 7 μm diameter carbon fiber anode (about 900e referred to the input);

and it must recover quickly from the (about ×1000) overload caused by the charged particle traversing the drift box. The preamplifier has been implemented in a monolithic transistor array with a discrete JFET input transistor and discrete resistors and capacitors setting time constants. The preamp has two gain values (strappable) to accommodate varying gas gains. The CRID preamp hybrid has 42 discrete components per channel, compared to 85 for the drift chamber.

Because of different physical constraints, the CRID preamps are packaged on one set of boards, and the AMU hybrids are on another.

Liquid Argon Calorimeter

The LAC has a lead radiator structure segmented into projective towers approximately 33 mrad on a side in a fine sampling, 22 radiation length electromagnetic section and twice that angular size in a 2.2 interaction length hadronic section. Tails of hadronic showers traverse the coil and are measured in the WIC, which is approximately 5 interaction lengths thick. The calorimeter is expected to have a electromagnetic energy resolution $\sigma(E)/E$ of about $8\%/\sqrt{E}$ and hadronic resolution of about $55\%/\sqrt{E}$. The barrel LAC cryostat is being readied for final insertion of the module assembly. The first endcap LAC is loaded with its modules and the second endcap cryostat is now being prepared for module loading.

The LAC requires a low noise charge sensitive preamplifier (an equivalent noise charge of less than 5000 electrons with 1 nF at the preamp input and a 4 μsec shaping time) and a 15 bit dynamic range [9]. The LAC block diagram is shown in Fig. 8. The preamps are packaged as 8 channel hybrids, and include power pulsing and calibration circuitry. The calibration capacitors are laser trimmed in an active fixture which compares an external reference charge to the calibration charge through the preamplifier to an accuracy of 0.25%. The preamp outputs feed a CDU hybrid, which has 16 channels of dual range (×1, ×8) sampling. Diode input protection network hybrids, preamps and CDU's are mounted on daughterboards having 48 full channels. These daughterboards mount directly on the insulating vacuum signal feedthroughs, and are grouped in sets of 15 on the feedthrough flanges. The flange assembly also includes an instrumentation board for the cryogenic sensors; a power control board, a controller board, and a digitizer/optical driver board. Each assembly accommodates 792 channels in a volume 41 cm in diameter and 13 cm high. It transmits all its data on one fiber in less than 2 ms each live beam crossing. Thus there is no special hardware for the calorimetric triggers. The power dissipation is 96 mW per channel.

Warm Iron Calorimeter

The WIC utilizes limited streamer mode plastic tubes (Iarocci tubes) in the spaces between the 5 cm thick iron flux return laminates of magnet. The tubes are read out from both sides: one side has projective tower pads continuing the geometry of the hadronic section of the LAC; the other side has 1 cm wide strips for muon tracking. The pad signals are read analogously to the LAC, except that a single range system is used with a simpler preamplifier. The packaging utilizes a more conventional cable plant to gang the pad signals into two depth segments and carry them to crates mounted on the surface of the detector. A storage card holds 72 2-channel hybrid preamps and 5 CDU's. A subsequent control and digitizer card produces a data stream format analogous to the LAC.

The muon tracking system has about 110,000 channels. The system utilizes 32 channel preamp discriminator shift register boards designed and manufactured by SGS [10]. These boards use a monolithic chip with 4 channels of the basic circuit preceded by a discrete preamplifier stage to permit operation in proportional mode if necessary. Four 8-channel hybrids are the major component on the boards, which are mounted in spacer assemblies between the ends of the magnet and its doors to minimize the cable plant. The boards are daisy chained into groups of up to 12 boards and are combined on signal fan-in and power distribution boards. The combined serial data chain is transmitted by a fiber to a specifically designed WIC Digital Readout Module [11] (WICDRM) which uses a MC68020 to receive and format hit clusters. The WIC is now being commissioned.

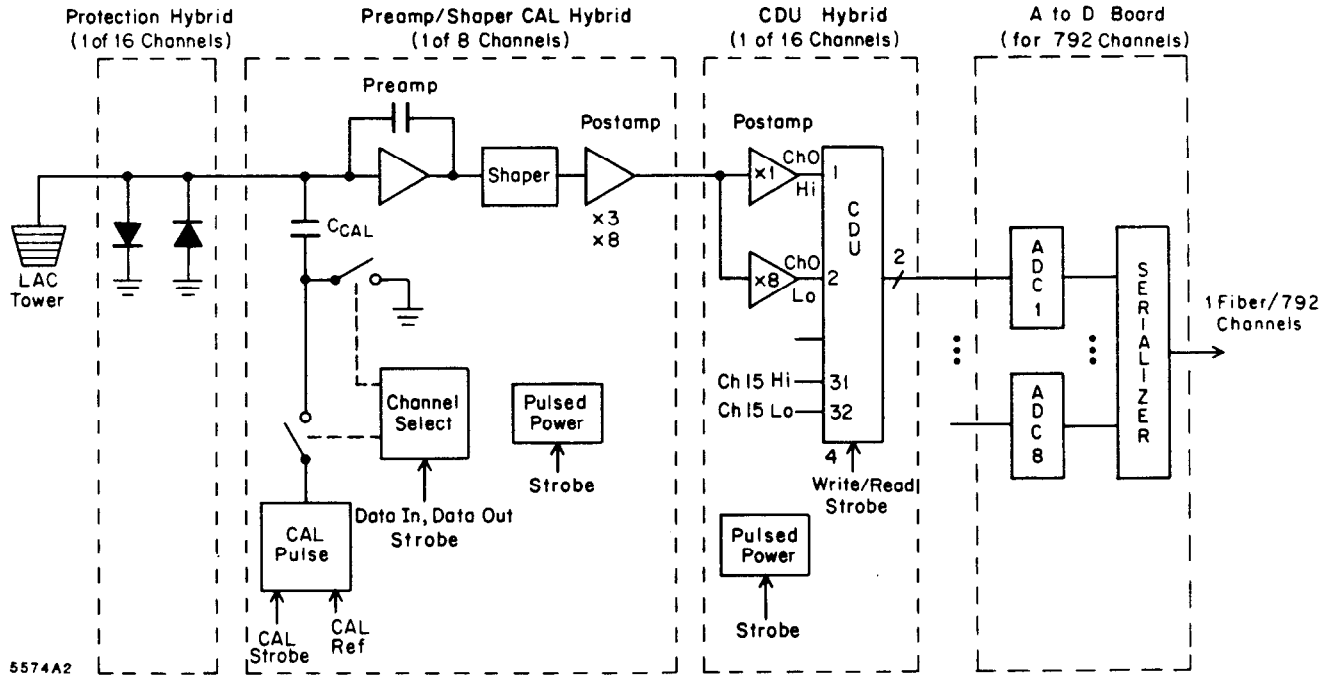

Fig. 8. Block diagram of the LAC front end electronics.

FASTBUS

The serial data streams from the drift chambers, CRID's, and calorimeters are optically received and buffered on FASTBUS auxiliary boards which feed the data processing modules [12]. Waveform Sampling Modules (WSM's) for the drift chambers and CRID's and Calorimetry Data Modules (CDM's) are actually the same board with differently programmed PAL's and with different amounts of plug in calibration memory. Each board has four data processing channels; each channel corrects and compacts the data stream using a Data Correction Unit (DCU) [13] feeding a data memory, and a MC68020 completes the data reduction. The DCU is a semi-custom CMOS VLSI part which performs a piecewise linear correction to the data with calibration constants specific to the AMU or CDU cell, and then compacts the waveform data by "snipping" pulses with their leading and trailing edges from the data stream, or, for calorimetry, selecting the appropriate gain range and subtracting the baseline. Essentially all of the calibration procedure is performed in parallel by the on board MC68020's. The prototype boards are operating and production of the 110 modules has begun.

Synchronization and control for each of the subsystems is accomplished by FASTBUS Timing and Control Modules (TCM's). These modules are themselves synchronized from the SLC control system, and generate both fast clocks (e.g., 119 MHz for the Drift System write into the AMU's) and slow clocks (e.g., 32 MHz) for synchronizing the detector systems to the WSM's and CDM's. The slow clocks are part of a 3 line protocol that controls the power pulsing, calibration, control reconfiguration, etc. The TCM outputs are distributed on optical fibers.

TRIGGER

The SLD event trigger is based on information from the drift chambers and calorimeters. As previously mentioned, the drift chamber data are reduced to one bit per sense wire and serialized in the preamp hybrids. The preamp data are daisy chained and fed by optical fibers to a FASTBUS module which reduces the data to one bit per cell in about 200 μsec. The full calorimetry readout cycle takes about 1.5 ms, and so no trigger specific hardware is needed. Various weighted energy sums are computed by the CDM's and are organized by the calorimetry AEB. These data and the drift chamber cell hit data are transmitted over FASTBUS to a trigger AEB. The AEB finds tracks by a dictionary look up technique [14] and combines track and calorimetric data to form a trigger decision in about 3 ms.

CONCLUSION

The design of the SLD electronics has taken significant advantage of the unique rate characteristic of an e^+e^- linear collider. This has involved a significant increase in the amount of electronics built into and onto the detector, which has involved the development of custom VLSI and many hybrid packages. Most of the data from the detector electronics is heavily time multiplexed and carried on optical fibers, leading to a minimal cable plant. All of the device design is complete, some system testing is still in progress, and major hybrid and board production is underway.

ACKNOWLEDGEMENTS

The design and construction of the SLD data acquisition system is a large undertaking with significant contributions from many of those listed in Reference 1 and other members of the technical staff of the collaboration. Nevertheless, special recognition should go to the engineering staff at SLAC, University of Illinois, Rutherford Appleton Laboratory, and the Universities of California at Berkeley and Santa Cruz. For reasons of time and space, this paper has not mentioned the software side of data acquisition. The influence of software considerations on the hardware design has been extremely significant in this project. The contributions of the SLD On-line Software Group to the basic design, evolution, and implementation of the data acquisition system are very gratefully acknowledged.

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