SLAC – PUB – 4780
October 1988
(I)

A FAST INTEGRATING EIGHT-BIT BILINEAR ADC*

K. A. BIERY, D. A. OUIMETTE AND J. L. RITCHIE
Department of Physics, Stanford University, Stanford, CA 94305
and
Stanford Linear Accelerator Center, Stanford University, Stanford, California 94309

ABSTRACT

A fast gated charge integrating ADC has been developed for measuring short photomultiplier pulses at very high event rates. The circuit is bilinear with 100 pC full scale and a least count of 150 fC. It features dc coupling, a minimum gate width of 20 ns, a minimum time between events of 200 ns plus gate width, a two event buffer, and front-end zero suppression with 100 ns read time per hit channel. Five hundred channels have been built and installed in the rare K_L^0 decay experiment E791 at Brookhaven National Laboratory.

INTRODUCTION

As high energy physics experiments move towards higher event rates, it is necessary to develop electronics capable of digitizing, storing and reading out signals from a detector with little or no dead time. Experiment E791 at Brookhaven National Laboratory is an experiment to search for rare $K_L^0 \rightarrow \mu e$ with a branching ratio of 10^{-12}. In this experiment individual detector channels can experience rates on the order of a megahertz and the rate of low level triggers can exceed tens of kilohertz. Figure 1 shows the readout architecture of E791 and is discussed in detail elsewhere [1]. Of interest in this report is the completely "Flash" front-end electronics and parallel pipelined readout architecture with sparse data scan. In less than 200 ns all times and charges are digitized and latched. There are two levels of event buffer including "Hit" information following digitization, thus allowing sparse readout of one event at up to 500 Mbytes per second while another event is being digitized. Events may also be discarded at either buffer stage via a level-two trigger decision by resetting a bit within the readout supervisor. We have developed a unique charge-integrating bilinear fast ADC as part of this system. The primary function of the ADC is to digitize photomultiplier signals from a large lead-glass array, but signals from a Čerenkov counter and assorted scintillation counters (about 500 channels in all) are also digitized. In this report, we describe the design and performance of this ADC.

CIRCUIT DESIGN

Several factors constrain the design of the ADC and associated readout electronics.

(1) Physics considerations dictated a dynamic range of approximately nine bits with 100 pC full scale.

(2) Since event rates are both high and random, dc coupling was necessary to prevent "pulse pile up."

(3) Some channels would eventually be used in the trigger which meant a fast 20 ns gate width would be needed. This gate must also provide better than 60 db isolation against pulses with rise times of order a few nanoseconds.

(4) As stated above, a completely "Flash" digitization on all front-end electronics was required. For the ADCs, this meant a flash ADC chip on each channel.

(5) In order to maximize throughput and minimize dead time of the overall system two levels of digital buffering are used following the analog to digital conversion. We also required front-end zero suppression since in any given event only a small fraction of all channels contain "Hits."

We have been able to meet these criteria with the circuit shown in Fig. 2. We use the Sony CX20052A 20 MHz eight-bit subranging ADC chip for the conversion [2]. Our extended dynamic range is achieved by paralleling part of the reference voltage divider with an external resistor. This provides the bilinear transfer function shown in Fig. 3. Table 1 shows the ADC specifications. A detailed circuit description follows.

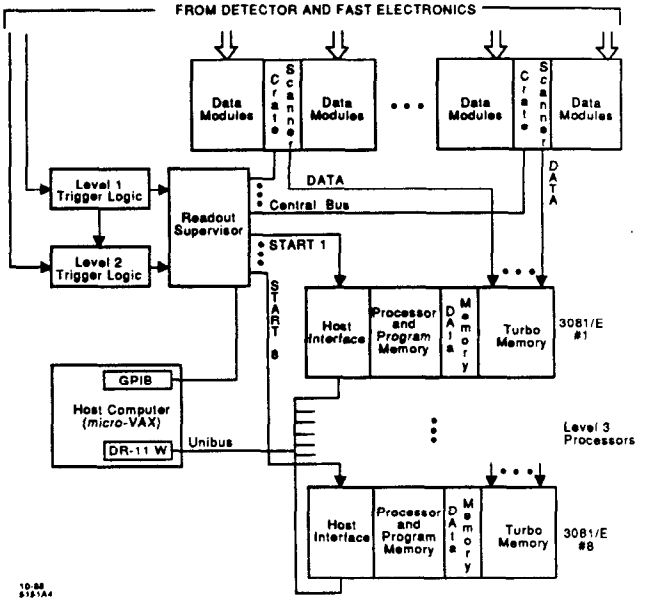

Fig. 1. E791 Readout system.

Amplifier A1 is a noninverting amplifier with a gain of ten which buffers the 50 Ω input from a four-FET gate circuit. This gate circuit provides more than 60 db holdoff for input pulse rise-times down to 2 ns. It is driven by one-half of a 10192, whose outputs are pulled up to +5.2 V. This is a very economical way to drive the SD5001 FETs directly from ECL logic. A one-time channel-to-channel gain trim is done at the output of the gate circuit. This compensates for inherent variations in FET characteristics in the gate circuit. The signal is then amplified and inverted at A2, then integrated at A3. FETs five and six keep the integrating capacitor C1 clamped to ground until the GATE signal arrives. These FETs are driven by the other half of the 10192 chip. R1 is a pedestal adjustment and is used to compensate for charge injection caused by capacitive coupling across the FETs gate-to-source and gate-to-drain junctions. A charge is injected into the summing node of the integrator which is opposite in polarity and equal in magnitude to the net charge injection from the FETs. About 20 ns after the gate period, the level at the output of A3 is digitized via the Sony A-to-D converter. The digitized data are then held in the output register of the A-to-D chip until a SHIFT pulse is received from the READOUT SUPERVISOR via the CRATE SCANNER. The input signal is also sent to amplifier A4 and comparator A5. The output of A5 is used to set the HIT FLIP FLOP, thus providing a flag for the sparse data scan as to whether this channel was hit. At this point, the READOUT SUPERVISOR either sends a SHIFT to transfer the data and "Hit" information to the second stage register, or waits until a previous event is finished being processed at the second stage. If a level-two "No" is received from the trigger logic for the previous event, then a bit representing that event is reset in the READOUT SUPERVISOR and the current event is SHIFTed to the second stage register, overwriting the previous event. If a level-two "Yes" is received, than a parallel readout of the event is initiated transferring two bytes of data per crate per 100 ns. Only channels with

*Work supported in part by the Department of Energy, contract DE-AC03-76SF00515, and by the National Science Foundation under grant PHY87-19227.

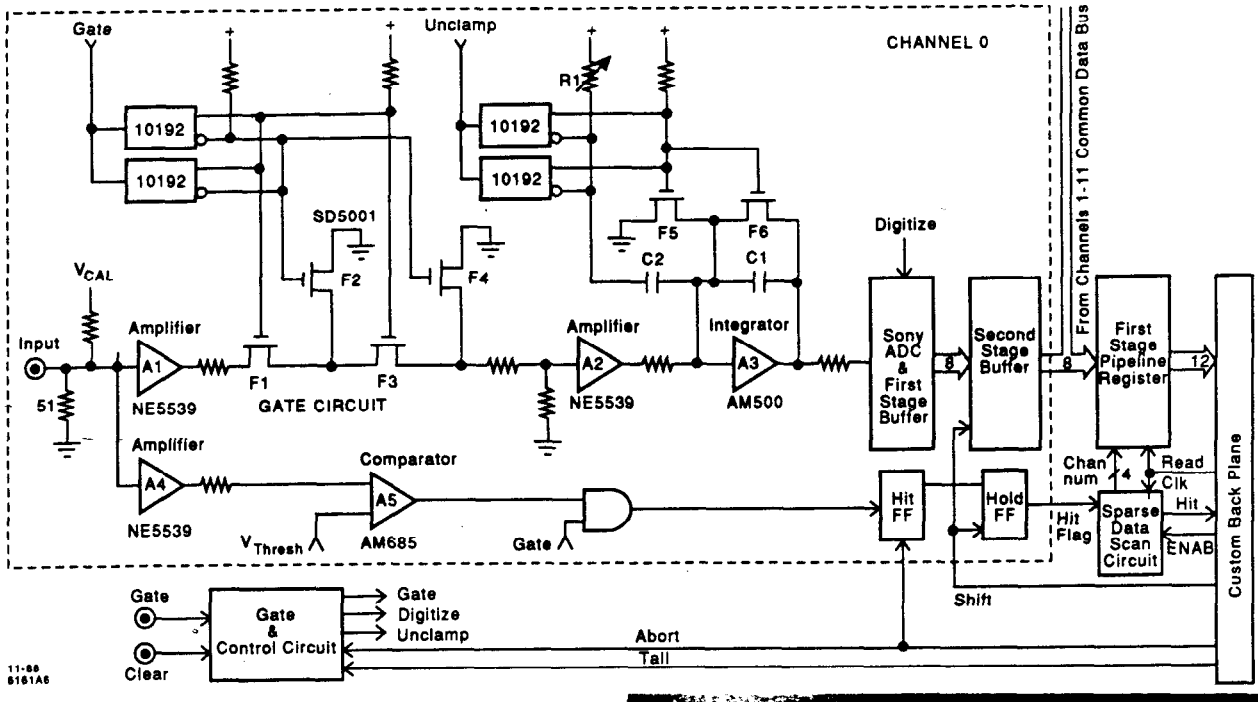

Fig. 2. E791 Fast ADC circuit.

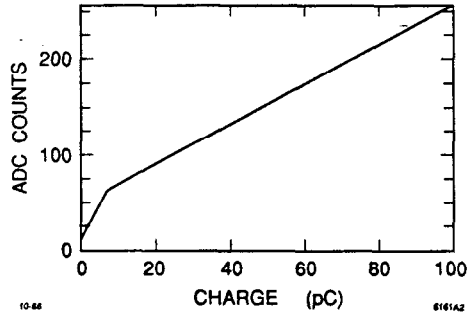

Fig. 3. Fast ADC bilinear transfer function.

TABLE 1. ADC SPECIFICATIONS

Resolution:	8 bits bilinear
Sensitivity:	150 fC/counts (0–63 counts)
	470 fC/counts (64–255 counts)
	100 pC/counts full scale
Noise (r.m.s.):	210 fC (100 ns gate)
Gate Width:	20 to 150 ns
Integral Linearity:	< 1 count
Digitizing Time:	200 ns
Readout Time:	100 ns hit
Channels/Card:	12

Fig. 4. Twelve channel fast ADC on custom format card.

"Hit" flags set are read out. It is probable that a level-two trigger decision will be made for the current event during the readout of the previous event. If the decision is to reject the current event, an ABORT is sent by the READOUT SUPER VISOR clearing the front-end and HIT FLIP FLOPs. The electronics is now ready to accept another event, independent of the previous event which may still be in a readout cycle. During the readout operation, the sparse data scan circuit sequentially steps through the channels containing data while a READ CLOCK transfers this data to the FIRST PIPELINE REGISTER. Channel information is added to the eight bits of data at this register. As data are piped to the SECOND PIPELINE REGISTER in the CRATE SCANNER, the next channel's data enter the FIRST PIPELINE REGISTER. A crate number and fine-event number are added at the SECOND PIPELINE REGISTER. The next clock tick sends the data to the TURBO MEMORY in the 3081/E. The CRATE SCANNER reads a "Hit" bit from each data card within its crate to skip empty cards, much as the card's scan circuit skips empty channels.

TEST RESULTS

The following is a brief description of some of the tests that were performed on the ADC.

1. Integral linearity

This was measured by sweeping the input pulse amplitude over the dynamic range of 100 pC and taking about

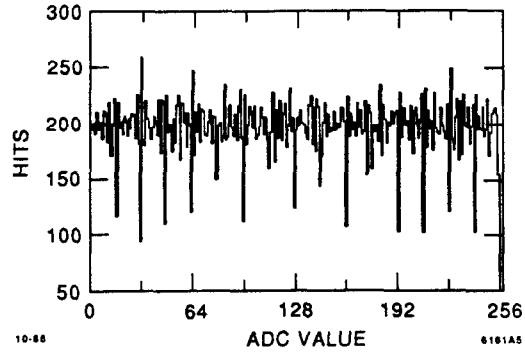

Fig. 5. Measurement of relative bin widths for 50,000 samples.

2000 random samples. A straight line is then calculated for each slope and the difference between the average output value and this line was found to be within one count.

2. Differential linearity

   The Sony CX20052A is a subranging ADC which digitizes the input in a two step process [3]. The first digitize pulse determines the high-order four bits of the output, and also selects a divider network for the low-order four bits which are digitized by the second digitize pulse. This eliminates having 256 comparators within the chip, but the bin widths are affected at every sixteenth count. Figure 5 is a histogram of a CX20052A output with a dc voltage sweeping over the dynamic range of the chip while 50,000 samples are taken. The horizontal axis represents the 256 bins of the eight-bit output, and the vertical axis is the number of hits per bin. This plot, although disturbing, is still within $\pm 1/2$ lsb differential linearity. The differential linearity of the final circuit shows a similar structure, but is slightly smeared by the r.m.s. noise.

3. The r.m.s. noise

   The r.m.s. noise was measured by pulsing the ADC with a 100 ns gate and no input. A TALL (test all) signal is generated which sets all of the HIT FLIP FLOPs so that all channels will be read out, and the standard deviation is calculated from 200 events. This was found to be about 210 fC.

4. Crosstalk

   No appreciable crosstalk was detected when adjacent channels were pulsed with large signals, and all channels were read out. Care was taken during the board design to minimize crosstalk by limiting the number of channels to twelve, providing some space between channels, and by placing all of the voltages on separate planes (six in all).

USE IN BNL EXPERIMENT 791

We built 50 modules, and 44 have been installed and operated in Experiment 791 at BNL. The modules are periodically tested in place. A dc test voltage (Vcal) is distributed to the front-end of all channels through an isolation resister. The voltage is swept over the full range of the ADC while triggers (and consequently ADC gates) are generated by a pulse generator. Data accumulated in this way is used to monitor the stability of the ADC calibrations, linearity, etc.

During normal physics data taking, two steps are taken to ensure the stability of the ADC pedestals.

(1) A continuous stream of triggers are generated with a 50 Hz frequency. This action is taken because tests have shown that if the period between events is much in excess of 20 msec, the ADC pedestal shifts slightly. This is probably due to leakage currents at the integrator that were discovered at a late date. The 50 Hz trigger prevents the period between triggers from ever exceeding.

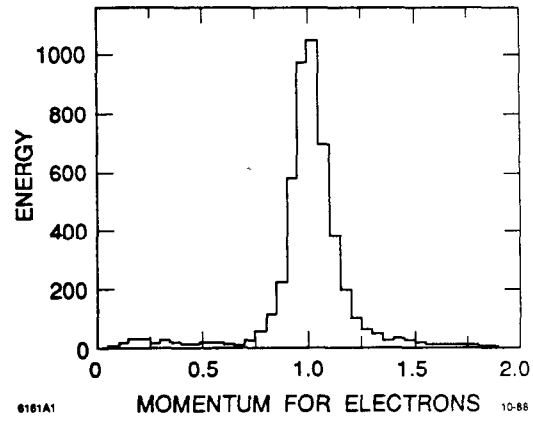

Fig. 6. Lead-glass energy divided by track momentum for particles identified as electrons by the Čerenkov counter.

20 msec and introduces only a negligible deadtime into the experiment.

(2) The ADC pedestals are continuously monitored by generating two special triggers during each beam spill. These triggers are accompanied by a signal which causes the HIT FLIP FLOP to be set on each channel and thereby causes the charge on all channels to be read out, so that the pedestals can be measured. In practice, we have found the pedestals to be stable to within a few counts over periods of several days, provided the temperature in the counting house is maintained within the nominal range.

The ADC's are used to measure pulse heights from photomultiplier tubes in the lead-glass system, a scintillation counter hodoscope, and a threshold Čerenkov counter. The lead glass-system is used in E791 to discriminate between electrons and other charged particles, and to observe photons. The energy calibration of the lead-glass is established by using momentum tagged electrons from the decay $K_L \rightarrow \pi e \nu$. The electron momentum is measured by tracking the electrons (with drift chambers) through two dipole magnets. Figure 6 shows lead-glass energy divided by track momentum for particles identified as electrons by the Čerenkov counter. A small pion contamination at low E/p is due to Čerenkov misidentification.

In summary, we have built bilinear eight-bit integrating ADC's for use in a high-rate rare K_L decay experiment at BNL. These modules are part of a system which has the feature that all front-end modules (ADC's, TDC's and latches) are digitized and the result shifted to a buffer within 200 nsec after the longest ADC gate. This system can be run with triggers rates of order 10^5 per second with low deadtime. E791 has taken data with this system, and we are satisfied that the system has met our initial design goals.

ACKNOWLEDGMENTS

We wish to express our appreciation to Dr. Karol Lang for his valuable support in the setup of this system at Brookhaven. We are also grateful for the technical support of Cameron Pierce, Maxine Roehrig and Anthony Tilghman.

REFERENCES

[1] R. D. Cousins et al., *"Fast Parallel Pipelined Readout Architecture for a Completely Flash Digitizing System with Multilevel Trigger"*, submitted to Nucl. Instrum. Methods, October 1988.

[2] See CX20052A data sheet, Sony Corporation of America, 10833 Valley View Street, Cypress, CA 90630–0016.

[3] S. K. Dhawan and K. Kondo, *"New Developments in Flash ADC's"*, IEEE Trans. Nucl. Sci. Vol. NS–31, February 1984.