SLAC – PUB – 4218
February 1987
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THE PULSED AMPLITUDE UNIT FOR THE SLC*

J. ROLFE, M.J. BROWNE, R.K. JOBE
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

1. Introduction

There is a recurring requirement in the SLC for the control of devices such as magnets, phase shifters, and attenuators on a beam-by-beam basis. The Pulsed Amplitude Unit (PAU) is a single width CAMAC module developed for this purpose. It provides digitally programmed analog output voltages on a beam-by-beam basis. Up to 32 preprogrammed values of output voltage are available from the single analog output of the module, and any of these values can be associated with any of the 256 possible SLC beam definitions. A 12-bit Analog-to-Digital Converter (ADC) digitizes an analog input signal at the appropriate beam time and stores it in a buffer memory. This feature is normally used to monitor the response of the device being controlled by the PAU at each beam time. Initial application of the PAU is as part of the system that controls the output of Klystrons in the SLC.[1]

The PAU combines several different functions in a single module. In order to accommodate these functions in a single width CAMAC module, field programmed logic is used extensively. Field Programmable Logic Arrays, Programmed Array Logic, and a Field Programmable Logic Sequencer are employed.

2. PAU Timing

Figure 1 shows the timing of PAU operation. The Fiducial signal is the timing reference for accelerator operation, and occurs at a 360 Hz rate about 1 ms before the time at which a beam is permitted in the SLC.[2,3] The Pattern information (PP codes) specifying a beam in the SLC is broadcast to the entire control system by the Master Pattern Generator for the SLC. The Patterns may be sent by the SLC Timing System and received by the PAU at any time from 1 ms before to 1 ms signal defining beam time is sent to the PAU as an SLC Timing Backplane signal from a Programmable Delay Unit (PDU).[4] It specifies action taken at the next beam time.

The Controlling of most devices is, as shown in Example A of Figure 1. The PAU output changes a fixed 1 ms after the previous beam. This insures that the required Pattern information has been received. The device being controlled by the PAU then has approximately 1.7 ms to reach a stable output before the next beam. The PAU digitizes an analog input signal, usually associated with the controlled device response, and places it in a buffer memory within the PAU . The controlled device response corresponding to each DAC output value is stored in memory.

However there are devices, such as the large magnet shown in Example B, that require more that the 1.7 ms available in one permitted beam time to stabilize. The PAU my be programmed to accommodate these devices. It is set-up initially so that the PAU DAC output value changes either two or three permitted beam times prior to the beam time when it is needed. The PAU then digitizes the device response, after waiting the required two or three permitted beam times, at the beam for which the device setting is used. The illustration shown is for a device that operates so slowly that the requested output may be changed on every third permitted beam time. In this mode, approximately 7.3 ms is available for the controlled device to stabilize. Note that the the Pattern for the beam that sets the DAC is followed by two Patterns which are associated with a special DAC output specification (DAC Address) which instructs the PAU to "do nothing." This insures that the PAU stays in synchronization.

Figure 2 shows PAU output with the output changing at a 360 Hz rate.

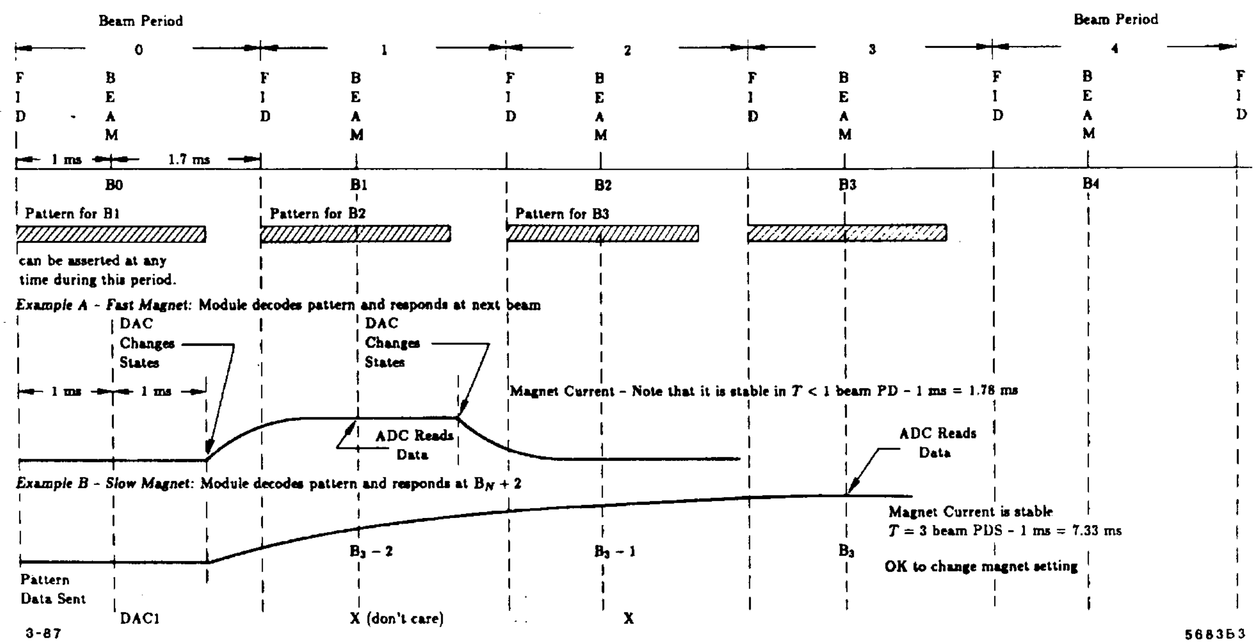

Figure 1. Timing Chart

*Work supported by the Department of Energy, contract DE-AC03-76SF00515.

Presented at the Particle Accelerator Conference, Washington, D.C., March 16–19, 1987

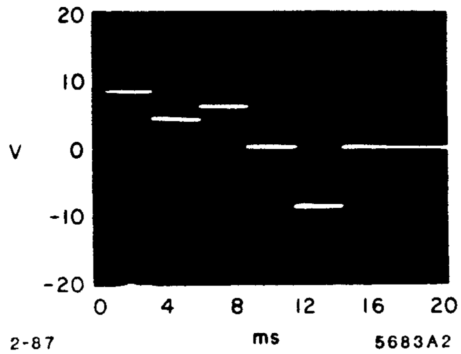

Figure 2. Typical PAU output.

3. PAU Operation

Figure 3 is a functional block diagram of the PAU. The Beam Code Mapping Table must be initially loaded to associate any of the 256 possible SLC Beam Codes with any of the 32 different values of output from the single analog output of the module. This table is loaded using the Beam Code (PP) Mapping Pointer. The value of the analog output is determined by the Digital/Analog Converter (DAC) Value Table and a 12-bit DAC. Appropriate values must also be initially loaded into the DAC Value Table. Thus a Broadcast Pattern is associated with a specific word (address) in the DAC value table, and a value of analog output is defined by each table entry. The range of analog outputs is ±10 volts.

Timing is controlled by an Input from the SLC timing backplane, generated by one PDU channel, as described above. This signal is essentially coincident with beam time and starts an Analog/Digital Converter (ADC) which measures the response of the device being controlled by the PAU at beam time and writes this value into the ADC Buffer Memory. The input to the ADC is balanced and differential with a full scale sensitivity of ±10 volts. The response corresponding to each value of DAC output is saved separately in memory so that the controlled device response to each DAC output value is available. Each DAC ouput is conventionally associated with a different beam code in the SLC. The module output normally changes to the state required for the next beam 1 ms after the backplane timing signal is received.

The ADC is read to the CAMAC Dataway as a floating point number in either standard 4-byte VAX or IEEE notation. The integer ADC output is converted to a floating point number through a mapping table that is in Programmed Read Only Memory (PROM) and output to the CAMAC Dataway when the ADC is read.

The least significant bit (LSB) of the floating point number read for ADC output is an error bit that is stored in the ADC Error Memory. The Error Bit for a particular ADC value is set when a new value corresponding that output value is written into the DAC Value Table, and it is cleared when that value is used as a PAU output. Thus this bit (if cleared) indicates that the ADC value read is a reading of current data.

A failure in the SLC timing system is detected if either the Patterns or the Timing Backplane signal to the PAU are not

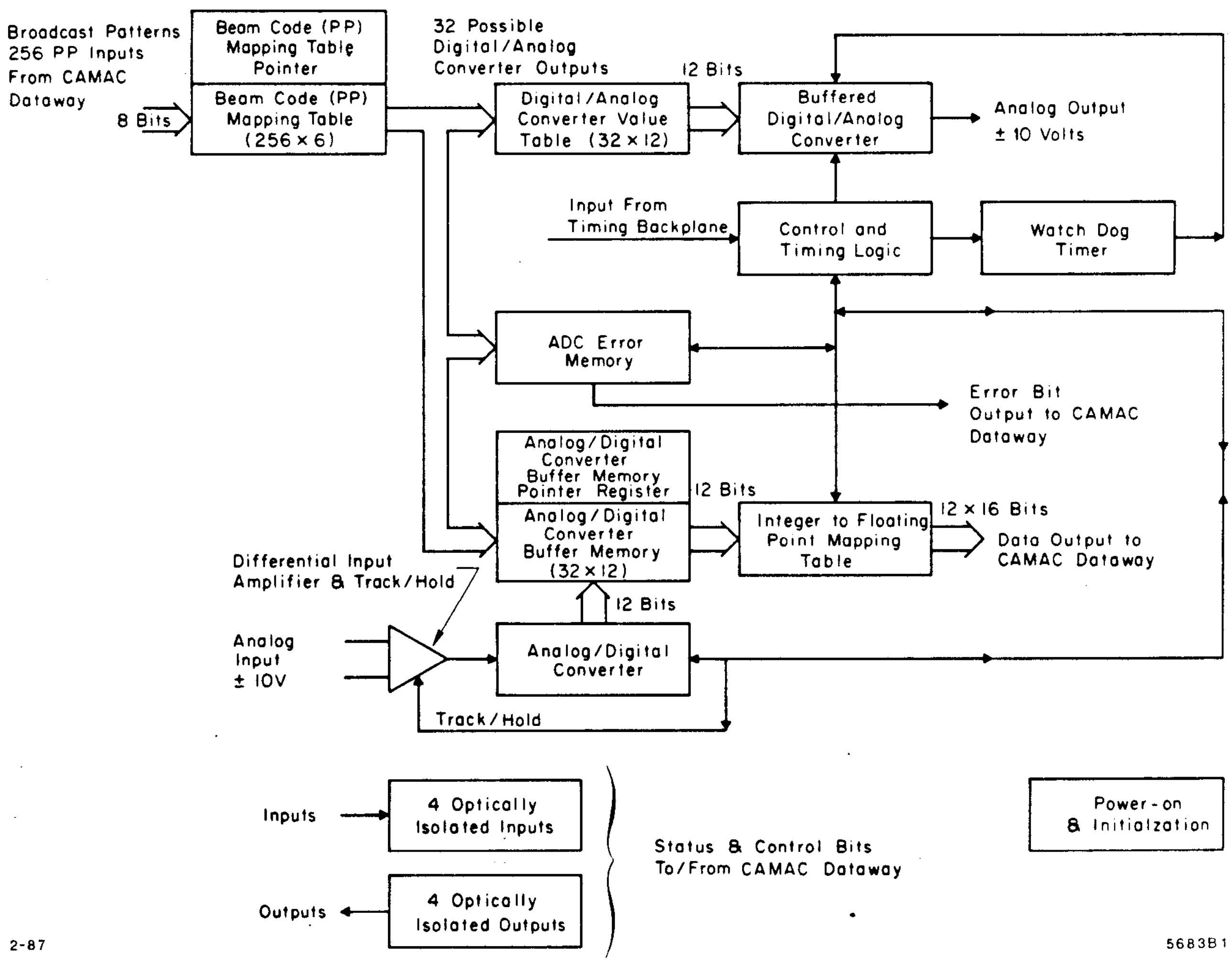

Figure 3. Fuctional Block Diagram

received for a period of 10 ms. The Watch Dog Timer then runs down and disables the PAU output, setting it to zero volts.

Status and control information may be provided in sytems using the PAU. Four optically isolated output bits for control and four optically isolated input status bits are available.

Table I is a summary of the CAMAC Function codes used in the module.

Table I. Function–Code Summary

F–Code ⋆Subaddress	Function
F0⋆A(N)	Read 1st 16 DAC settings.
F1⋆A0	Read ADC Buffer Memory.
F1⋆A1	Read Beam Code (PP) mapping Table Pointer.
F2⋆A0	Read ADC Pointer.
F2⋆A1	Read Remote Device Status.
F4⋆A0	Read Beam Code (PP) Mapping Table.
F5⋆A(N)	Read 2nd 16 DAC settings.
F9⋆A0	Clear the module.
F16⋆A(N)	Write first 16 DAC output values.
F17⋆A0	Write Options Control Register.
F17⋆A1	Write Beam Code (PP) Mapping Table Pointer.
F18⋆A0	Write ADC Pointer.
F19⋆A8	Broadcast Pattern used by PAU for devices that require 1 beam period for stability.
F19⋆A9	Broadcast Pattern used by PAU for devices that require 2 beam periods for stability.
F19⋆A10	Broadcast Pattern used by PAU for devices that require 3 beam periods for stability.
F20⋆A0	Write PP Mapping Table.
F20⋆A1	Write Remote Device Control Bits.
F21⋆A(N)	Write 2nd group of 16 DAC outputs.
F24⋆A0	Disable Analog Output.
F26⋆A0	Enables Analog Output.
F27⋆A0	Test Analog Output Enable. (Q=1 for enabled).

4. Conclusion

The PAU is proving to be a versatile and reliable source of control signals for analog devices requiring beam-by-beam control. Presently, approximately 50 units are scheduled for use as part of the control system for the SLAC Linear Accelerator and the SLC.

Acknowledgments

We would like to acknowledge the help of all of the people who worked on this project. In particular, we would like to thank the following for their contributions. Technical support was provided by D. E. Heggie during module design, development and debugging. System and software support were provided by K.A. Thompson and K. K. Underwood. Printed circuit design was done by E. H. Austin and R. Bautista , and E. L. Ferrell worked hard to make the production of modules go smoothly. J. A. Truebenbach tested and repaired modules, and C. W. Allen helped with the commissioning of units in the SLC control system.

References

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