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FASTBUS DUAL-PORT MEMORY AND DISPLAY DIAGNOSTIC MODULE*

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ABSTRACT

A dual-port FASTBUS memory module has been designed as a diagnostic tool for both Crate and Cable Segments.

INTRODUCTION

The module described here is a FASTBUS slave module with ports to Crate and to Cable Segments. It incorporates two distinct but interlaced memories: one (256 × 32 bits) is a fast memory (10 nsec access time) used for testing the busses at full FASTBUS speed; the other one is a slower, larger memory (16k × 32 bits with 100 nsec access time) for software testing purposes.

The module performs all the main FASTBUS protocol functions. It is designed using KEK's FMA601 ADI chips and SLAC's hybrid prototypes of a cable segment differential transceiver.

DESCRIPTION

The module can be subdivided in six main blocks (Fig. 1) as follows.

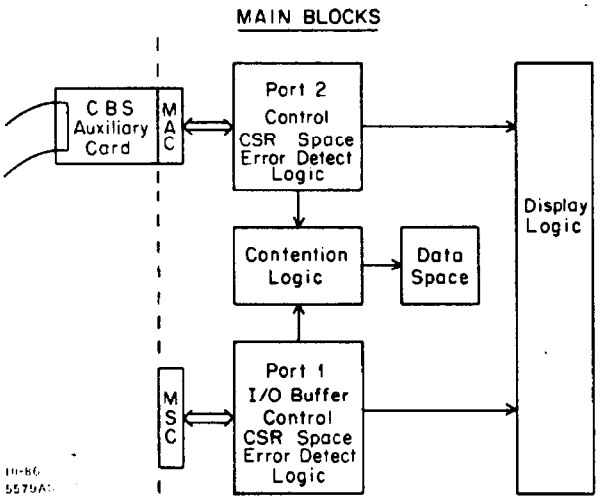

Fig. 1.

The cable segment (CBS) auxiliary card.†

The CBS Auxiliary Card (Fig. 2 and Photo A) is a $6\frac{1}{4} \times 6\frac{7}{8}$ inch card and accommodates 15 four-channel SLAC ECL Differential Transceivers, terminations for the driver input lines (LT), terminating resistors and bias current sources for the CBS differential lines (CST)[1]. Depending on the position of the module on the Cable Segment, different combinations of resistor packages can be used to terminate the cable at the passive end (100 Ω between the lines) or at the active end (two 51 Ω to V_{term} and a bias current I on the L+ line) or nothing at all at other locations. The resistor values chosen terminate a cable with a characteristic impedance of 100 Ω. A resistor of 1.3K Ω to V_{EE} provides a 4 mA current sink. For a 4 mA system the error due to the resistor type current 2.8% with a full loaded segment (32 devices). Note that, due to the common mode range of the receiver, the terminating voltage V_{term} is zero (GND).

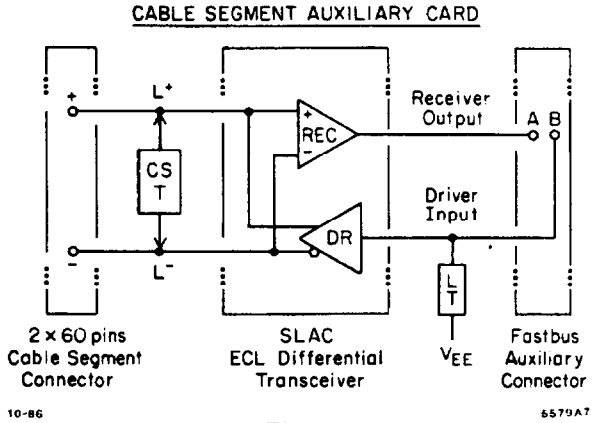

Fig. 2.

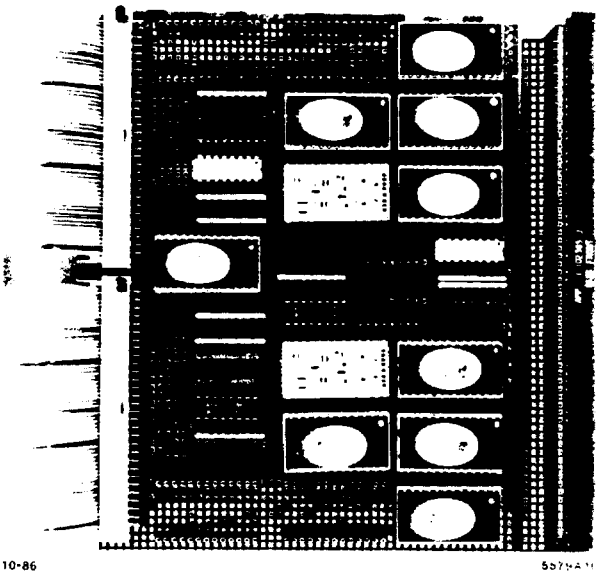

Photo A.

Figure 3 shows the implementation of the SLAC Differential Transceiver which has been described elsewhere[2].

Port 1 or crate port.

This part includes four FMA 601-ECL ADI chips, CSR Registers, error detection logic and control logic for the Crate Port. The ADI chip (Fig. 4) has bidirectional buffers for the AD lines and unidirectional buffers for the user, Parity generation logic, Logical Address Register CSR#3 and Logical and Geographic Address comparators. CSR space includes Reg.#0 (ID Reg.), Reg.#1 (Error Counter), Reg.#2 (Control Reg.), and Reg.#3 (Module Addr. (MA) Reg. in the ADI).

Port 2 or cable port.

This part is a symmetrical copy of Port 1 less the ADI chips (the I/O buffering for the AD lines is done by the transceiver) plus an external Module Address Register CSR Reg.#3, Geographical and logical Address comparators and register latches for data read.

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† The Working Group on FASTBUS Cable Segment recommended a preferred method of "outboarding" cable segment drivers and receivers on an auxiliary card so that a module can survive potential changes in Cable Segment specifications (Atlanta July 1, 1986). In this scheme, the A pins of the Auxiliary connector shall be connected to the Receiver Outputs while the B pins shall be connected to the Driver Inputs.

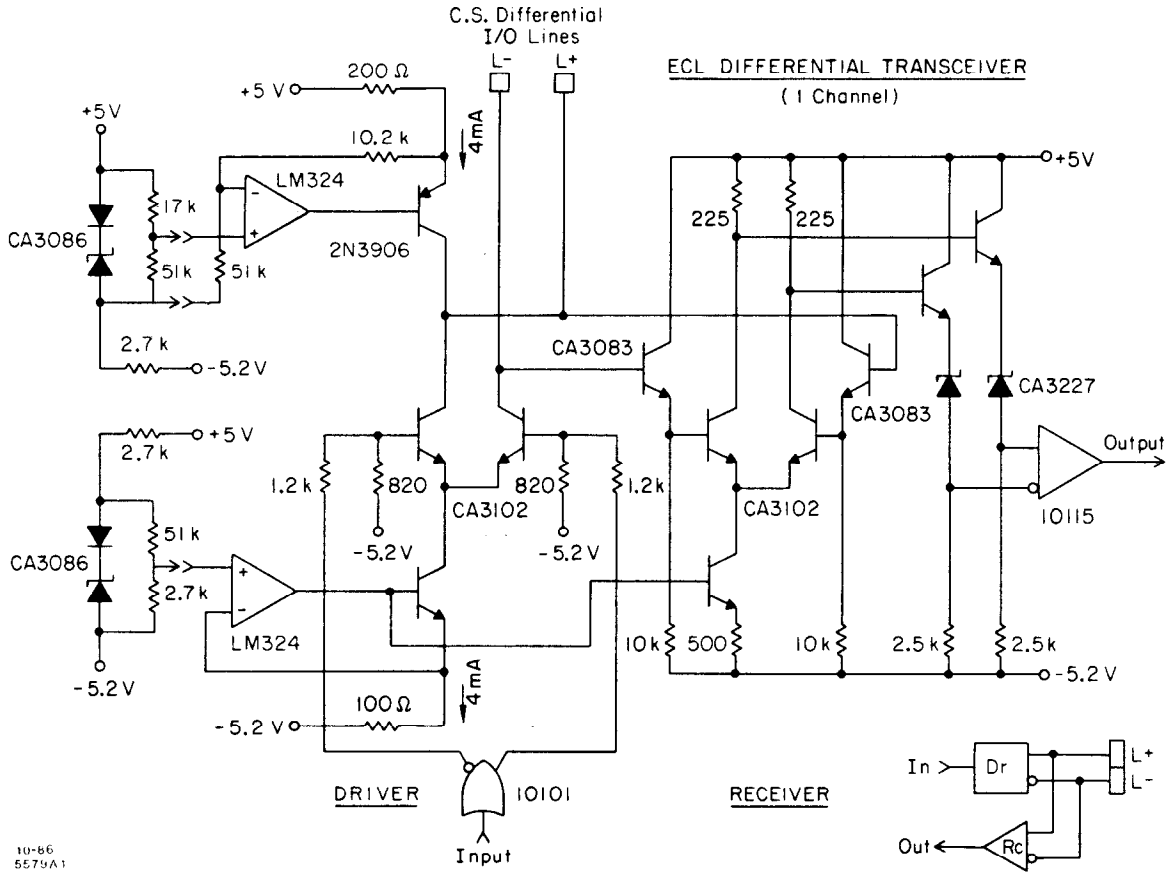


Fig. 3.

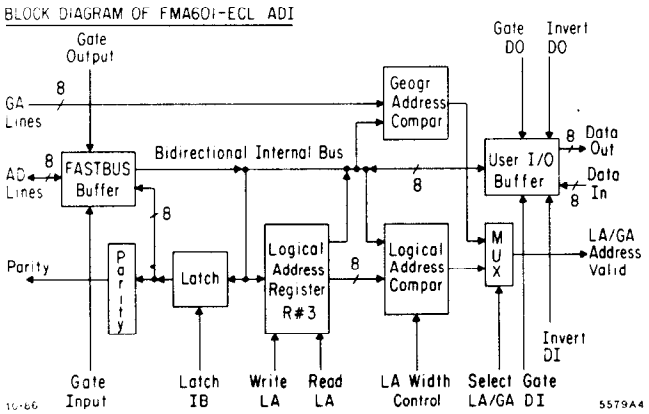


Fig. 4.

Data space.

This portion is shared by both ports. It includes a 14 bit Memory Address Register (MAR) and the two memories: a fast 256 × 32 bit memory (Fujitsu MBM 10422) with 10 nsec access time and a slow 16k × 32 bit memory with 100 nsec access time (Hitachi HM 6264LP–10).

Contention logic.

This part resolves contention between the crate port and the cable port when both try to access Data Space. When Data space has been accessed by one port, the other port is held off and a WT signal will be issued to that port by the contention logic if it tries to access this space.

Display logic (Fig. 5).

This logic can monitor either bus continuously (a switch selects crate or cable bus) or can generate WT in response to selected leading or trailing edges of the timing signals AS, AK, DS, DK and AG and at the same time latch the content of that bus into internal registers. It has manual or automatic (variable, up to 1 sec) reset capability on the WT line. Front panel LED display is switch selectable to show either the content of the internal registers or the status of the bus after the WT line has been received by the operating modules and activity has stopped.

OPERATION

Each port has always complete control of its own CSR space. It can also read all the CSR space Registers of the other port at any time with one exception: Port 2 can access Reg.#3 of Port 1 only if Port 1 is not busy. This is due to the fact that Reg.#3 (MA reg.) is inside the ADI chip. Data Space is shared by both Ports and the contention logic will permit access to this space on a first-come-first-serve basis.

Data space can be organized as one fast 256 × 32 bit memory, one slow 16K × 32 bit memory, or the combination of both. Two control bits in CSR Reg.#2 may disable access to either one of the memories or none. In the latter case the fast memory follow the slow one. Wrap-around occurs in all three cases, though a SS=2 signal is generated with overflow. A dual-width clock generator is needed to access the two memories. Figure 6 shows how this generator has been implemented. The chip used is the MC10198 retriggerable one-shot, the trigger comes from the Fastbus Data Synch (DS) line (buffered and delayed). The positive (P) and negative (N) edge control lines are driven by module select (internal AK line) and block transfer (MS0=1) signals respectively, the width control input is controlled, through a resistor divider, by the two control lines (bit 2 and 3) of CSR Reg.#2 and the Address line A14. A logical "0" at this input produces 10 nsec clock pulses, a logical "1" yields 100 nsec clock pulses.

Figure 7 shows a detailed block diagram of the module, Fig. 8 the word formats and Photo B a prototype module.

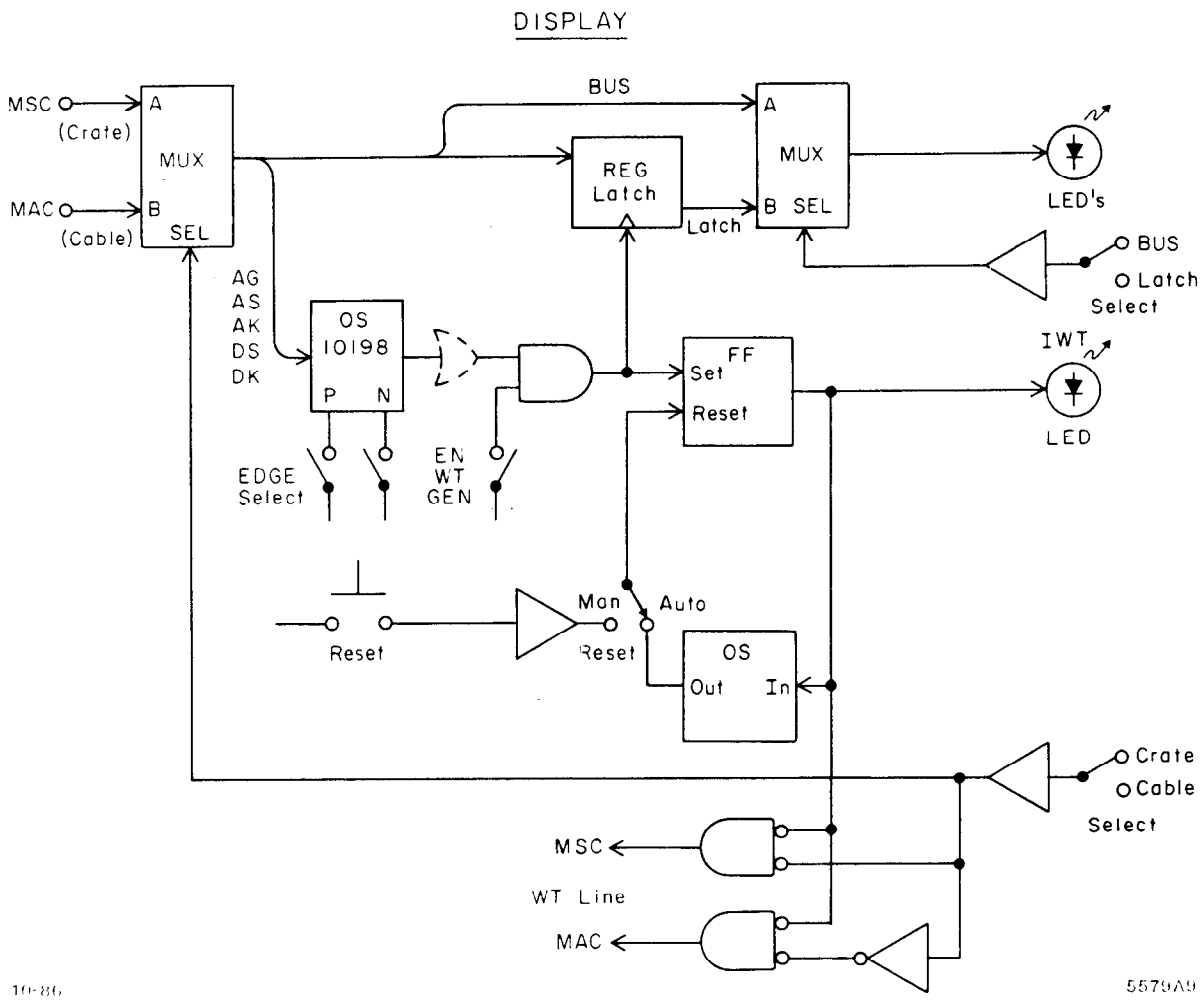
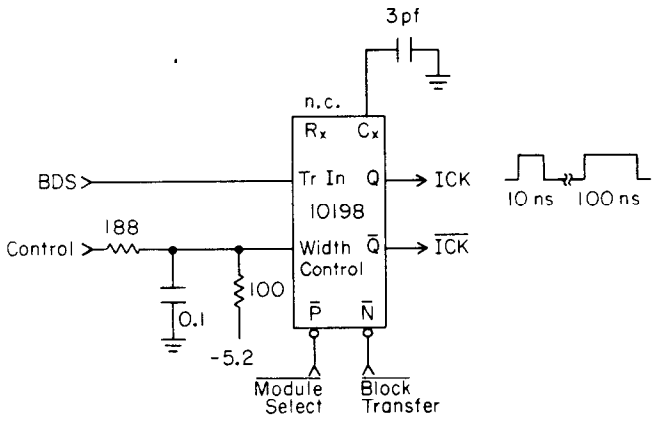


Fig. 5.



DATA SPACE	AI4	CSR R#2 BIT2	CSR R#2 BIT3	CONTROL
0	X	X	X	Fast Output
1	0	0	0	Slow Mem } Normal
1	1	0	0	Fast Mem } Operation
1	=1	0	1	Fast Mem Only
1	=0	1	X	Slow Mem Only

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Fig. 6.

This module performs all the main FASTBUS protocol functions such as logical and geographical addressing in both spaces, broadcast operations, block and pipeline transfers, parity check and generation and SS responses on parity error [(7) if in data space, (6) if in control space], on end of block transfer (2) and on an invalid IA (7).

The implementation is done in ECL eccept for the TTL 16K memory and related translators.

APPLICATIONS

This module is extremely valuable as a diagnostic tool. It can be used fo. :rror logging, general debugging including block transfers, for monitoring either segment on-line through the front panel display, and to facilitate the testing of master modules at full ECL speed.

It not only permits the detailed examination of both segments, but it also has a sufficiently large and fast memory to allow many diagnostic tests to be made, or to serve as a communication "mailbox" between segments.

ACKNOWLEDGMENTS

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BLOCK DIAGRAM

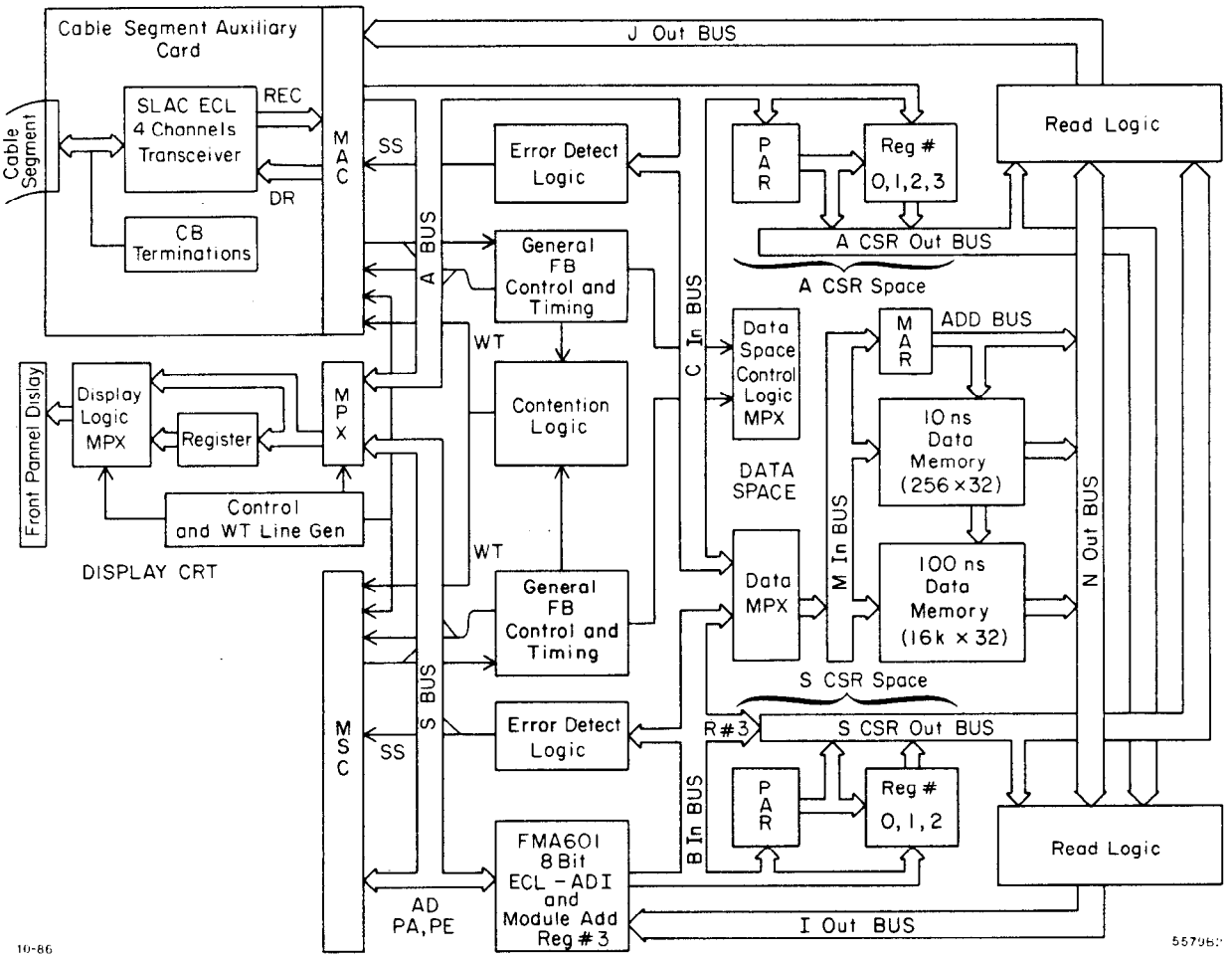

Fig. 7.

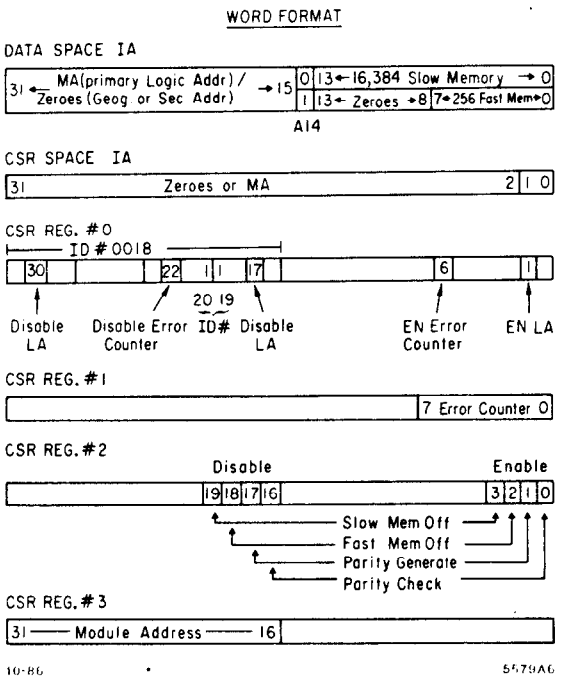

Fig. 8.

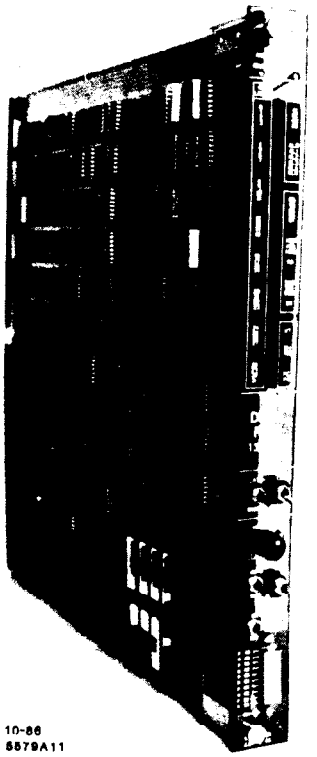

Photo B

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1. *IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control System,* ANSI/IEEE Std 960-1986 (Appendix C).
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