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THE DIGITAL CORRECTION UNIT: A DATA CORRECTION/COMPACTION CHIP

S. MACKENZIE, B. NIELSEN, L. PAFFRATH, J. RUSSELL, AND D. SHERDEN

Stanford Linear Accelerator Center, Stanford University, Stanford, California 94305

ABSTRACT

The Digital Correction Unit (DCU) is a semi-custom CMOS integrated circuit which corrects and compacts data for the SLD experiment. It performs a piece-wise linear correction to data, and implements two separate compaction algorithms. This paper describes the basic functionality of the DCU and its correction and compaction algorithms.

1. INTRODUCTION

At event time, drift chamber waveforms and calorimeter pulses are stored in analog memory cells on the SLD detector. After the event, these cells are serially read out, digitized, and passed to the Digital Correction Unit (DCU) for correction and compaction. Each analog cell has its own correction curve, which is piece-wise linearly approximated by one to 128 segments. Constants which define the segments are stored externally to the DCU in a memory.

The DCU is a semi-custom integrated circuit which performs online data correction and compaction. It performs a piece-wise linear correction to 15-bit unsigned data, and compacts the corrected data according to one of two selectable algorithms. After compaction, the corrected data is passed onto a 16-word deep fifo for temporary storage. The maximum data rate through the correction and compaction stages is 1.33 Mhz. DCU specifications are outlined in Table I. Table I. DCU Specifications

Maximum input data rate	1.33 Mhz
Maximum clock rate	21.3 Mhz
Output FIFO depth	16 words
Power dissipation	300 mW
Package	68 pin PLCC

<u>Architecture</u>

The DCU was designed to interface to two independent buses. The first is a bidirectional bus on which input data and correction constants are loaded, and through which the DCU's programmable registers can be written and read. The second bus is an output bus on which corrected and compacted data appears.

Functional Blocks

The DCU consists of four major blocks:

- Corrector
- Waveform Sampler Module (WSM) Personality Section
- Calorimetry Data Module (CDM) Personality Section
- Output Buffer

A block diagram of the DCU is shown in Fig. 1.

<u>Corrector</u>

The Corrector section performs a piece-wise linear correction to input data. Correction constants are looked up from a correction table stored in external memory. Table values are interpolated to obtain a corrected data value.



Fig. 1. Block DCU Block Diagram.

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Algorithm: The input data is considered to be divided into two fields. The first field consists of the most significant bits of the input data. These bits, external to the DCU, select a particular segment of the piece-wise linear approximation. The second field consists of the remaining bits, and is the offset into the selected segment. A left-shifter in the corrector section aligns the offset field with the most significant bit of the corrector ALU to obtain correct normalization and to insure that truncation errors at the output of the ALU are minimized. The shift value, n, is programmable between 1 and 8 to accommodate a range of correction segments and input data widths. The correction algorithm is as follows:

$$y = (2^{n-16} * x * (c2 - c1)) + c1$$

where:

x is the offset field of the input data

n is the number of bits the input data is left-shifted before being corrected

cl is the first correction constant associated with the segment that the data is on

c2 is the second correction constant associated with the segment that the data is on

y is corrected data, truncated to 15 significant bits plus sign

The corrector ALU consists of a multiplier and a signed 15bit adder/subtracter. The multiplier operates on a 15-bit unsigned multiplicand and a 15-bit signed multiplier, and yields a 30-bit signed product, of which only the most significant 15 bits plus sign are passed on to the compaction sections.

The corrector also provides timing signals to the external correction constant memory and to the input data buffers, and also contains control registers for the rest of the unit.

After correction, the data is passed to either the WSM Personality Section or the CDM Personality Section for compaction and formatting.

<u>Diagnostic Modes</u>: Several bits in the DCU control registers determine whether the ADC input register and/or the two correction constants registers are loaded on each data cycle. By loading the constants registers and then disabling the synchronous loading of them, a pass through mode can be obtained in which the corrector section has no effect on the input data. This is useful for both diagnostic and system calibration purposes.

WSM Personality Section

The WSM Personality Section (WPS) performs formatting and compaction of corrected data according to an algorithm required for the Waveform Sampler Module (WSM). The WSM analyzes digitized drift chamber pulses which have been sampled and stored in analog memory units (AMU) on the SLD detector. The information in the AMUs is serially read out, digitized, and passed to the DCU on the WSM for correction and compaction. After correction and compaction, the data is passed to another processor on the WSM board for further reduction before being sent a host computer.

WSM Compaction Algorithm: Figure 2 shows a typical data pulse processed by the WSM Personality Section. It is desired to pass the entire data pulse, including the complete rising and falling edge, to the WSM processing section. By comparing the data stream against a threshold, noise between pulses can be filtered out; however, it is desirable to start recording several words before the trigger, in order to record the entire leading edge of the pulse. The WPS has a programmable depth fifo which is used to provide a short history of the corrected data stream. A maximum FIFO depth of 64 permits use of a relatively high trigger threshold, thus ensuring that all zero data and typical noise is filtered out. When a data word over a trigger threshold is detected, a unique tag is output signifying the start of an output data stream, followed by an address and a series of data words. The address is a unique identifier of the nth datum preceding the one which caused the trigger, where n is the FIFO depth. Data are output, starting with the nth one before that which caused the trigger. Subsequent data are output until a programmable number of data words below a second (trailing) threshold are detected. Thus, when a trigger occurs, several data words before the trigger are recorded along with the pulse itself. Trigger and trailing thresholds, FIFO depth, and trail count are programmable.



Fig. 2. WSM Compaction.

Double-pulse waveforms are handled in the following way: If, while recording, the data dips below trailing threshold and then goes above it, the trail count is reset so that the entire double-pulse waveform is recorded.

Recording is forced on by several other conditions. When used in a system where many wires are time-multiplexed into the DCU, recording is forced on at each wire boundary. The wire boundary interval is programmable to be 512 or 1024 buckets. Also, a "Pass through" mode is supplied to disable compaction for calibration or diagnostic purposes.

CDM Personality Section

The CDM Personality Section (CPS) performs compaction of corrected data according to an algorithm required for the Calorimetry Data Module (CDM). It performs baseline subtraction and gain selection, thereby reducing the data per channel from four to one.

To accommodate the wide dynamic range of calorimeter data, pulses are fed to the inputs of two amplifiers at the detector which have different gain. The two data signals, plus two baseline signals from each calorimeter channel, are stored in an analog memory device called a Calorimetry Data Unit (CDU). The CDUs are serially read out, digitized, and then sent to the DCU. The sequence of CDM signals to the DCU are shown in Fig. 3. The baseline signals have been sampled immediately before the event, and the data signals have been sampled during the event.

It is desired to select the optimum data signal—if the highgain signal is above a certain threshold, its amplifier may be near saturation and the other signal should be selected. Conversely, if the low-gain signal is below a certain threshold, better dynamic range can be obtained by using the high-gain signal. The CPS section of the DCU selects the optimum signal, and optionally, subtracts out the signal's corresponding baseline.

CDM Compaction Algorithm: The signals are presented to the DCU in the sequence base0, data0, base1, data1.

The CPS compares data0's uncorrected value against a programmable threshold. Based on that decision, either data0's or data1's corrected value are passed to the DCU output buffer. A programmable control bit determines the "sense" of the decision; i.e., whether the uncorrected data value must be greater



Fig. 3. CDM Data Source and Sequence.

than or less than the threshold to be considered optimal. The output data word's most significant bit indicates whether data0 or data1 was selected.

In addition, the threshold comparison and decision can be overridden so that any or all elements of the group can be output for diagnostic or calibration purposes.

2. OUTPUT BUFFER

Compacted data from the personality sections are stored temporarily in a 16-word deep FIFO. The FIFO is intended to moderate the data rate out of the DCU to facilitate interface of the DCU to external processors or memory.

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3. IMPLEMENTATION

The DCU is a semi-custom integrated circuit, implemented in 2 micron double-metal CMOS. It was designed using standard cells, compiled cells, and full custom layout. The DCU is comprised of approximately 42000 transistors on a die 277 x 225 mils in size. It is packaged in a 68-pin plastic leaded chip carrier (PLCC).

4. STATUS

At this time, prototype chips have been received and are currently being analyzed. A tester has been built to assist in chip characterization and to perform incoming inspection of production units.

5. CONCLUSIONS

A semi-custom integrated circuit has been designed to perform data correction and compaction. It performs the function of approximately 50 discrete TTL chips, and is useful in at least two FASTBUS modules—the Waveform Sampler Module and the Calorimetry Data Module.

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