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Front-End Data Processing in the SLD Data Acquisition System*

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ABSTRACT

The data acquisition system for the SLD detector will make extensive use of parallel processing at the front-end level. Fastbus acquisition modules are being built with powerful processing capabilities for calibration, data reduction and further pre-processing of the large amount of analog data handled by each module. This paper describes the read-out electronics chain and data pre-processing system adapted for most of the detector channels, exemplified by the central drift chamber waveform digitization and processing system.

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1. Introduction

The SLD detector[1] is being constructed to study e^+e^- collisions at energies up to 100 GeV in the centre-of-mass at the Stanford Linear Collider (SLC). It is a large solenoidal detector designed to cover 97% of the full solid angle with good tracking resolution, extensive particle identification, and finely segmented electromagnetic and hadronic calorimetry. A cross section of a quadrant of the detector is shown schematically in Fig. 1. The main components are

- A vertex detector consisting of 220 CCD chips arranged in two cylinders around the beam, with a total of 50 million pixels of data.
- A drift chamber system with approximately 8000 wires arranged in a cylindrical central chamber and two sets of planar end-cap chambers. Each wire of the end-cap chambers and the two ends of each wire in the central chamber will be equipped with analog read-out, a total of about 12,000 channels.
- A Čerenkov Ring Imaging Detector (CRID) system with liquid and gas radiators. Three coordinates for each converted photon are obtained from wire position, time of arrival of the photo-electrons, and charge division measurements on an array of highly resistive carbon fibres. The total number of analog read-out channels is around 32,000.
- A lead-liquid argon calorimeter with two electromagnetic and two hadronic sections arranged in projective towers, containing approximately 45,000 channels.
- An iron calorimeter with streamer tube read-out to supplement the liquid argon calorimeter and for muon identification. The electronics consists of about 10,000 channels of analog pad read-out and 100,000 channels of digital strip read-out.
- A tungsten calorimeter with 1280 channels of Si read-out at small polar angles for luminosity measurement.

The task of the data acquisition system is to collect and record the data from the entire detector with the precision required by the performance of the detector components, and within a time consistent with an overall low system dead-time. With a total of about 100,000 analog read-out channels, online calibration procedures and data pre-processing become important system design considerations. In addition, the trigger logic is considered an integral part of the SLD data acquisition system.

When compared to colliding ring experiments, the low 180 Hz repetition rate of the SLC allows different approaches to be taken to the whole data acquisition task. Thus, with 5.5 $msec$ between beam crossings, a relatively slow read-out of the data used by the trigger is acceptable, and the trigger decision can be implemented exclusively in microprocessor based software. Furthermore, with an expected average rate of events accepted by the trigger of $1-2$ Hz, read-out times as long as 50 $msec$ for accepted events give an acceptable system dead-time below 10%. The solutions adapted by SLD for the detector read-out reflect this low repetition rate. They are characterized by

- analog data storage directly at the individual detector components,
- a very high degree of multiplexing of data transfer into the data acquisition modules outside the detector,
- very powerful calibration and data reduction logic on each data acquisition module, and
- higher level processing for *e.g.* trigger algorithms, data formatting, and further online event processing.

This paper will concentrate on the data acquisition modules as seen in the context of the above points. The discussion will be restricted to the central drift chamber read-out, but the scheme is with only minor variations valid for the analog channels of all detector components and will all be summarized at the end.

2. System Design

The data acquisition system[2] is implemented in Fastbus, with the overall architecture shown in Fig. 2. The leveling reflects the degree of parallel processing at each stage of the read-out sequence and calibration procedure, with each level having enough microprocessor based power to do a considerable amount of pre-processing before sending the data on to the next higher level.

At the lowest level, a major branch (Fastbus segment) is dedicated to each detector component. This level contains crates with data acquisition modules which are individually responsible for digitization, calibration and data reduction of the raw data. Semi-custom designed integrated circuits and Digital Signal micro-Processors (DSP) perform these functions. Each acquisition module also has sufficient memory to hold data from several events, in order to buffer data until processing has finished in all modules, before transfer of the event to the next higher level. At the crate level, one fast programmable processor, SSP,[3] is responsible for data formatting, mastership of the crate, and communication with the trigger level.

The trigger level uses several SSPs to determine whether full read-out should continue after the initial 5 *msec*. For this decision, fully digitized and calibrated data from the calorimeters is available through Fastbus from the lowest level, and separate latched data is provided from the drift chambers. The trigger level also serves as traffic manager for the read-out of triggered events. Finally, the highest level of micro-VAXen and host computer serve to further refine the trigger decision, to record the event, and as processors for online analysis.

3. The Central Drift Chamber Data Acquisition

3.1 PERFORMANCE GOALS

The Central Drift Chamber is the main tracking device in the SLD detector. The cylindrical volume has an inner radius of 0.2 m, outer radius 1.0 m, and a length of 1.8 m. Sense wires are grouped in cells of 8 wires, and the cells are in turn organized in 10 cylindrical super-layers, 4 axial and 6 at small stereo angles, such that an outgoing particle will have 80 measurements along its trajectory.

Drift times and third coordinate by charge division will be measured for each of the about 5,000 sense wires. In the drift coordinate, a precision of 100 μm is required, or about 10 $nsec$ in drift time (the drift velocity is 9 $\mu m/nsec$). For charge division, the goal is a resolution of 1% of the wire length which translates into a similar relative precision on each of the two charge measurements. In order to handle the high cell occupancy that will occur in narrow jets, the electronics is being designed to measure tracks with spatial separation in excess of 1 mm, corresponding to pulses about 100 $nsec$ apart.

3.2 SYSTEM OVERVIEW

The requirements for both timing and charge resolution in a multi-hit situation has led to a read-out scheme using waveform sampling, shown schematically in Fig. 3. Data from each of the analog channels is sampled 512 times at 8 $nsec$ intervals. Rather than transmitting every signal on individual cables to an external digitizer, the data is stored in an Analog Memory Unit[4] (AMU), positioned directly on the end-plate of the drift chamber. The AMU is a custom VLSI chip containing 256 sample and hold circuits. To obtain the necessary dense packing, the AMU chips have been placed in a 16-chip hybrid with circuitry for the read and write clock. For the purpose of the central drift chamber the AMU chips inside the hybrid can be configured in pairs to serve 8 sense-wire channels (one cell) with 512 samples each.

In addition to the analog storage, the signals are passed through an analog comparator and latched for each beam crossing. This condensed information is passed to an SSP at the trigger level which uses the data from the whole drift chamber to identify candidate tracks. A trigger reject decision will be taken in time to be ready to accept the next beam crossing 5.5 $msec$ later. Full digitization is only done for events accepted by the trigger, and for these events a total of 64 channels (32 K samples) are multiplexed out at a rate of 1.5 μsec/sample via an analog optical fibre to the Waveform Sampling Module (WSM) and digitized sequentially by a 12-bit ADC. The total read-out and digitization time is about 50 $msec$, after which the system is ready to accept a new event.

Waveform Sampling Modules reside in Fastbus crates shown at the lowest level in Fig. 2. To facilitate further data processing both ends of the same wire are read out by the same WSM, and four sets of data streams will be handled in parallel by the same module. As a result, each acquisition module can process 512 analog channels (256 double-ended wires), and the whole system for the central drift chamber will occupy only two Fastbus crates. The WSM modules will perform full calibration corrections and data reduction at the acquisition rate of 1.5 μsec/sample and do further waveform processing to determine hit times and charges at a slower rate compatible with the average $1-2$ Hz trigger rate. On-board memory will allow buffering of several events at each stage of processing.

3.3 WAVEFORM PROCESSING

Fig. 4 shows waveforms on a single wire for a single pulse (a) and a multi-hit event (b) as recorded by a proto-type chamber, using the AMU hybrid in a Camac module.[5] As the AMU consists of individual analog storage for each sample, the samples must be corrected individually for pedestal and gain variations and small non-linearities. In Fig. 4 these corrections were applied offline. The Fastbus Waveform Sampling Module is designed to perform the following tasks in normal data acquisition mode:

- receive and digitize the samples at a rate of 1.5 μsec/sample,
- multiplex two data streams, originating from two ends of the same wire, into one stream of digitized data flowing at 0.75 μsec/sample,
- apply individual corrections to each sample synchronously with the digitization rate,
- suppress data samples close to nominal zero and store the calibrated and compressed data in memory; this is also performed at the digitization rate,
- process the waveforms to extract leading edge timing and charge integrals in a multi-hit environment; store times and charges in memory, and
- communicate via Fastbus to the crate SSP.

A block diagram of the module is shown in Fig. 5. The figure shows the components to handle two optical fibres (one from each end of the drift chamber). The actual module will contain four such streams in parallel, serving a total of 8 optical fibres. Optical fibre receivers, sample and hold circuits and the 12-bit ADCs are mounted on an auxiliary Fastbus card in the rear of the crate, and the digitized data is multiplexed into four parallel streams entering the Fastbus module at a rate of 0.75 μsec/sample.

The Digital Correction Unit (DCU) is a semi-custom CMOS integrated circuit. In conjunction with the external memory of calibration constants it is designed to perform the calibration corrections and in addition to do the zero-suppression on the calibrated data. The latter function can be turned off by externally accessible registers, and an alternative function can be activated such that the same circuit can be used also for the calorimeter read-out; in this case the zero-suppression logic is replaced by subtraction of consecutive samples for base-line adjustments and a selection of one out of two separate gain settings available for each channel in order to extend the dynamic range.

A piece-wise linear interpolation algorithm is implemented for the calibration corrections. The ADC range is divided into a binary number (4, 8 or 16)

of equidistant intervals, and for each interval end-point the corresponding corrected value is stored in the calibration constants memory. Separate constants are needed for each AMU sample. Logic external to the DCU uses a sample counter together with the most significant bits of the ADC value to select from memory those two end-point values, c_0 and c_1, which bracket the current ADC reading. Using these two constants, the DCU then calculates the corrected value by a simple linear interpolation. The logic implemented in the DCU is shown in Fig. 6a. Preliminary results show that 4 or 8 segments are necessary to meet the 1% charge division requirement. The constants memory corresponding to one DCU chip for an 8 segment correction is 1.2 Mbytes.

The second function of the DCU chip is logically shown in Fig. 6b. Only samples which are part of a continuous pulse are transmitted to the output port of the DCU. A continuous pulse is here defined as starting at a fixed number of samples before the signal reaches a leading threshold and ending after a number of samples has been below a trailing threshold. At this stage advantage is taken of the fact that the data from two ends of the same drift chamber wire are interleaved in the data stream so as to ensure a one-to-one correspondence between the two wire ends in the transmitted data. Preceding each pulse train out of the DCU is a tag and a starting address. The values of leading and trailing thresholds, and the number of samples to transmit before leading threshold (FIFO depth) and after trailing threshold are all loadable registers in the DCU.

Further data processing is performed in the Digital Signal Processor (DSP) which has access to the same memory in which the corrected and reduced data is stored by the DCU. The DSP is a Texas Instrument TMS32020 (TMS320C25) fast programmable processor with a 200 (100) *nsec* instruction executing cycle. Each DSP is supported by 128 Kbytes of program memory. Since the DSP can normally only access 128 Kbytes of data memory, a special memory mapping scheme is implemented for the 320 Kbytes of buffer memory. The DSP will be programmed to detect leading edges of possibly overlapping drift chamber pulses by requiring threshold crossings of the first derivative of the signal, determine the

drift time by a leading edge algorithm, and integrate the signal to form the total charge. The results will again be stored in the buffer memory in a format readily usable as part of the complete event. The memory is sufficiently large that a number of events, both reduced waveforms and calculated times and charges, can be stored. This allows the DSPs to operate asynchronously and to achieve a good utilization of the parallel processing power. Through Fastbus the DSP will signal the end of processing of an event, and it is up to the crate master (SSP) to read the processed data from memory through Fastbus whenever all DSPs in the system have responded. The system is as such characterized by a very large amount of parallel processing power in DSPs combined with a distributed event buffering on the data acquisition boards.

3.4 SYSTEM CALIBRATION

Because each sample in the AMUs must be separately calibrated, a very large amount of calibration constants need to be determined (each WSM board holds 4.6 Mbytes of constants). An essential ingredient of the calibration system is therefore to exploit the parallelism in processing power obtained by the distributed system of DSPs and SSPs. By applying known DC levels to the inputs of the AMUs, the complete electronics chain from AMUs to ADCs can be calibrated simultaneously for all AMU samples. It is the task of the DSPs to record the data from the calibration events and to calculate the calibration constants and diagnostics relevant for its own set of electronics channels. Having obtained the constants, they are copied into the calibration memory through Fastbus under control of the crate SSP. Diagnostic information is directed to the host computer. Additionally, a calibration pulser system will be used in order to calibrate the individual channels through the preamplifiers.

4. Summary

The data acquisition system being built for the central drift chamber of the SLD detector has been described. Key elements are analog storage of data in Analog Memory Units mounted on the detector and a highly multiplexed read-out via analog optical fibres. Emphasis is put on highly distributed data processing power for calibration and waveform analysis, residing in Fastbus data acquisition modules (Waveform Sampling Modules). This front-end processing allows higher level processors to operate under a very reduced data load.

Analog channels in the other detector components will be handled in essentially the same way. Indeed, both the end-cap drift chamber system and the Čerenkov Ring Imaging Detector will use the identical AMU hybrid and WSM data acquisition modules. For the calorimeters (lead-liquid argon, iron and tungsten-silicon), no waveform analysis is performed and the amount of data is considerably smaller. In this case the analog storage is in the Calorimeter Data Unit[6] (CDU), a chip analog to the AMU, which is arranged to sample the signal twice: once at signal maximum and once just prior to beam crossing, in order to measure the signal base line. To gain dynamic range, each signal is split and measured with two different gains, thus resulting in a total of four analog readings per calorimeter channel. In the data acquisition module, the Digital Correction Unit (DCU) will calibrate all four readings, subtract the base-lines, and select the appropriate gain based on the signal size. During data acquisition, the DSP will in this case work synchronously at the acquisition rate and form energy sums and bit maps of energy depositions. Because of the smaller amount of data in this case, the total acquisition will finish in about 1 *msec* and the digitized and pre-processed data will be used in the trigger decision. For the vertex detector, the analog storage is provided by the detector CCD chips themselves, and the read-out is done serially for each chip through a flash ADC into the data acquisition modules. Subsequent data reduction is performed to exclude empty pixels and remove background induced high amplitude signals.

Due to the large amount of data, the reduction in this case will rely primarily on specialized hardware.

Table 1 shows estimates of the amount of data at each level of processing for all detector components. Also shown is the number of analog sampling cells which need to be calibrated.

Extensive proto-type testing of all main detector components, including their read-out systems, is planned for autumn 1986. The AMU hybrids were tested in a Camac module in connection with a proto-type drift chamber in early 1986. Optical fibre link, DCU chip and WSM acquisition module have been designed and are scheduled to be used for the up-coming tests.

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REFERENCES

1. SLD Design Report. SLAC-Report-273, May 1984.

2. D. J. Sherden, SLAC-PUB-3695, invited paper at the 4th Real Time Conference on Computer Applications in Nuclear and Particle Physics, Chicago, Illinois, May 20-24, 1985.

3. H. Brafman, T. Glanzman, A. Lankford, J. Olsen, L. Praffrath, *IEEE Trans. Nucl. Sci.* **NS-32** (1985) 336.

4. D. R. Freytag, J. T. Walker, *IEEE Trans. Nucl. Sci.* **NS-32** (1985) 622. D. R. Freytag, G. M. Haller, H. Kang, J. Wang, *IEEE Trans. Nucl. Sci.* **NS-33** (1986) 81.

5. W. B. Atwood et al., SLAC-PUB-3910 (1986) and Proc. of Wire Chamber Conference, Vienna, Feb 1986.

6. G. M. Haller, D. R. Freytag, J. T. Walker, S. I. Chae, *IEEE Trans. Nucl. Sci.* **NS-33** (1986) 221.

Table 1. Event lengths at various processing levels, and the number of analog sampling channels to calibrate.

Subsystem	Raw (Mbytes)	DSP (Kbytes)	SSP (Kbytes)	Host (Kbytes)	Calibrated samples
Vertex	50	-	130	?	-
Drift Chambers	12	500	40	40	6 M
CRID	16	50	20	20	8 M
Calorimeters	0.5	120	120	20	240 K

FIGURE CAPTIONS

1. Cross-section view of one quadrant of the SLD detector.
2. Fastbus configuration.
3. Drift chamber basic read-out scheme, showing sense wires with analog storage and multiplexed transfer through optical fibres to the WSM module.
4. A typical drift chamber waveform for a) a single pulse event and b) a multi-pulse event.
5. Block diagram of a quarter of a Waveform Sampling Module.
6. Logic implemented in the Digital Correction Unit for a) piece-wise linear correction and b) zero suppression of waveforms.

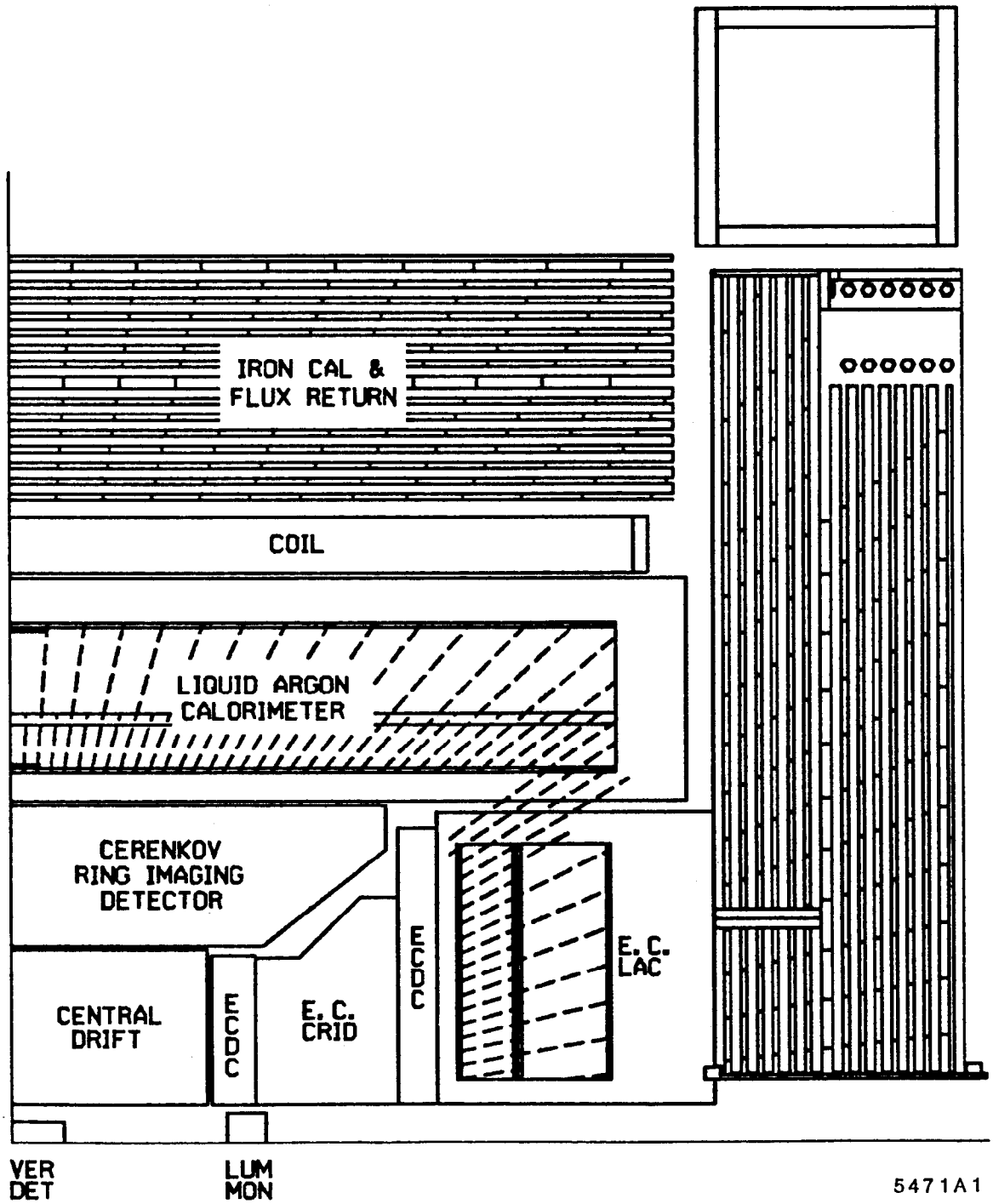
IRON CAL &
FLUX RETURN
COIL
LIQUID ARGON
CALORIMETER
CERENKOV
RING IMAGING
DETECTOR
CENTRAL
DRIFT
ECDC
E. C.
CRID
ECDC
E. C.
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Fig. 1

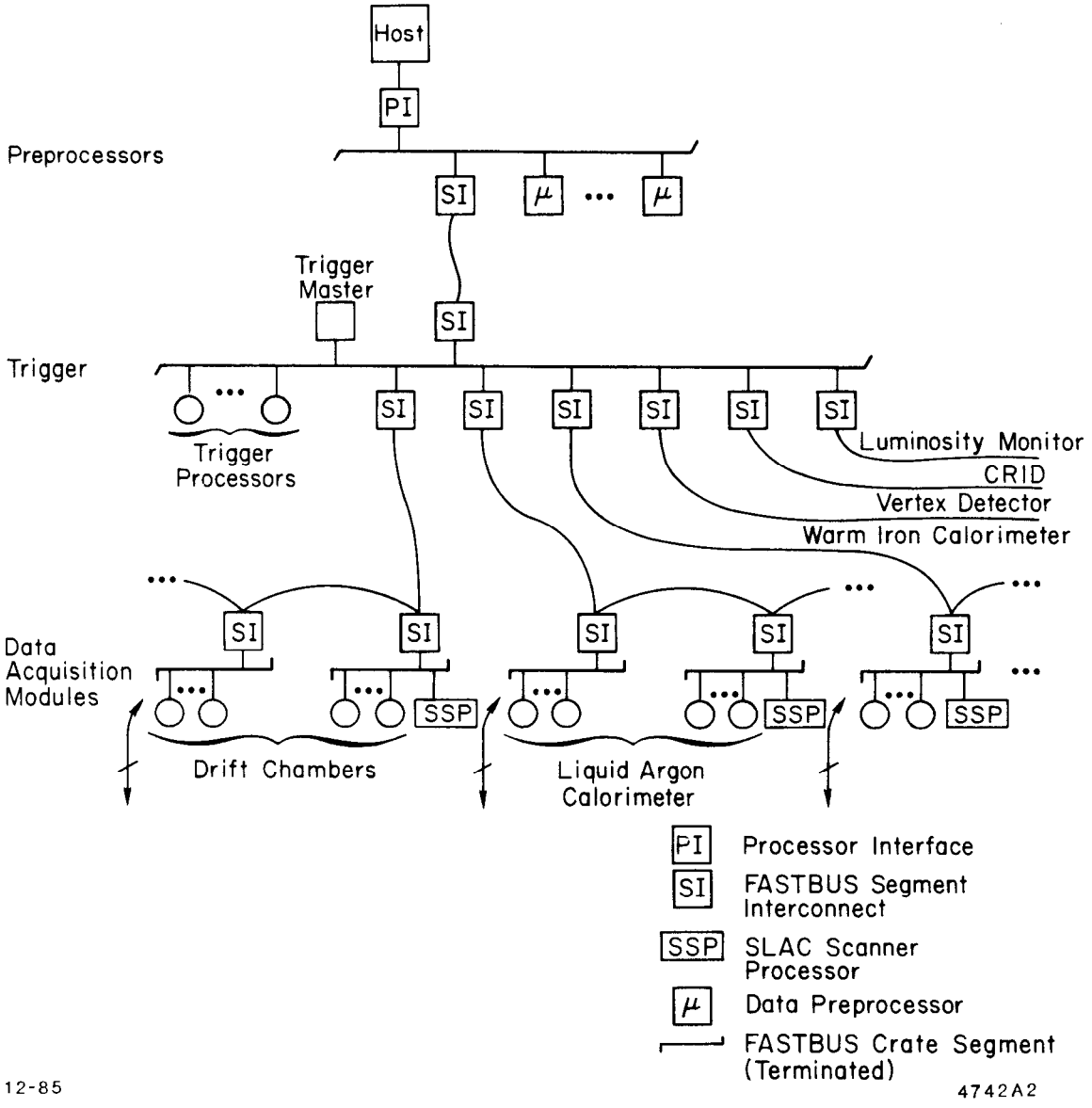
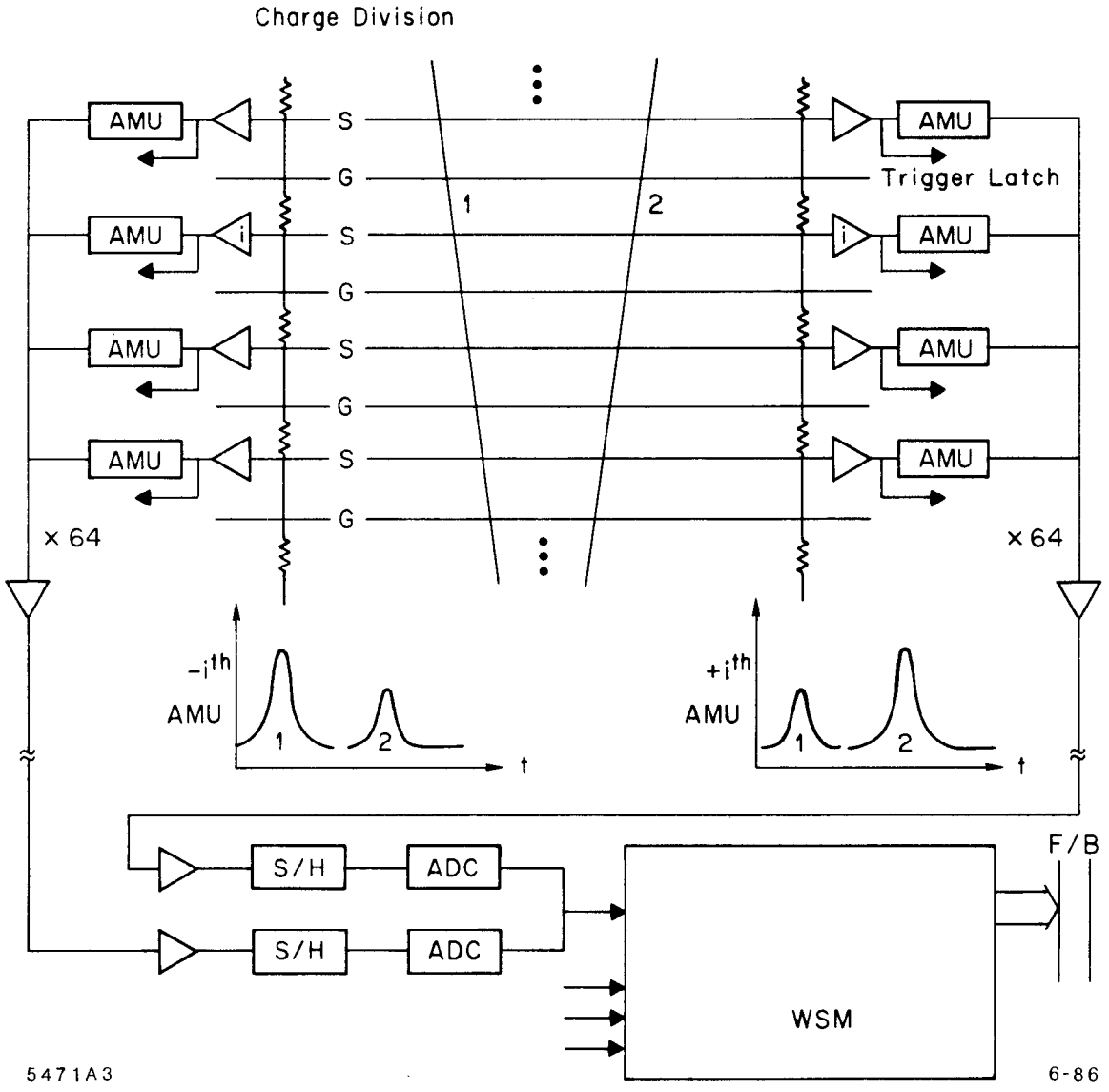

Host
PI
Preprocessors
SI
μ
Trigger Master
Trigger
Trigger Processors
Luminosity Monitor
CRID
Vertex Detector
Warm Iron Calorimeter
Data Acquisition Modules
SSP
Drift Chambers
Liquid Argon Calorimeter
Processor Interface
FASTBUS Segment Interconnect
SLAC Scanner Processor
Data Preprocessor
FASTBUS Crate Segment (Terminated)
12-85
4742A2

Fig. 2


Charge Division
AMU
S
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1
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Trigger Latch
i
× 64
-i th AMU
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t
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ADC
WSM
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5471A3
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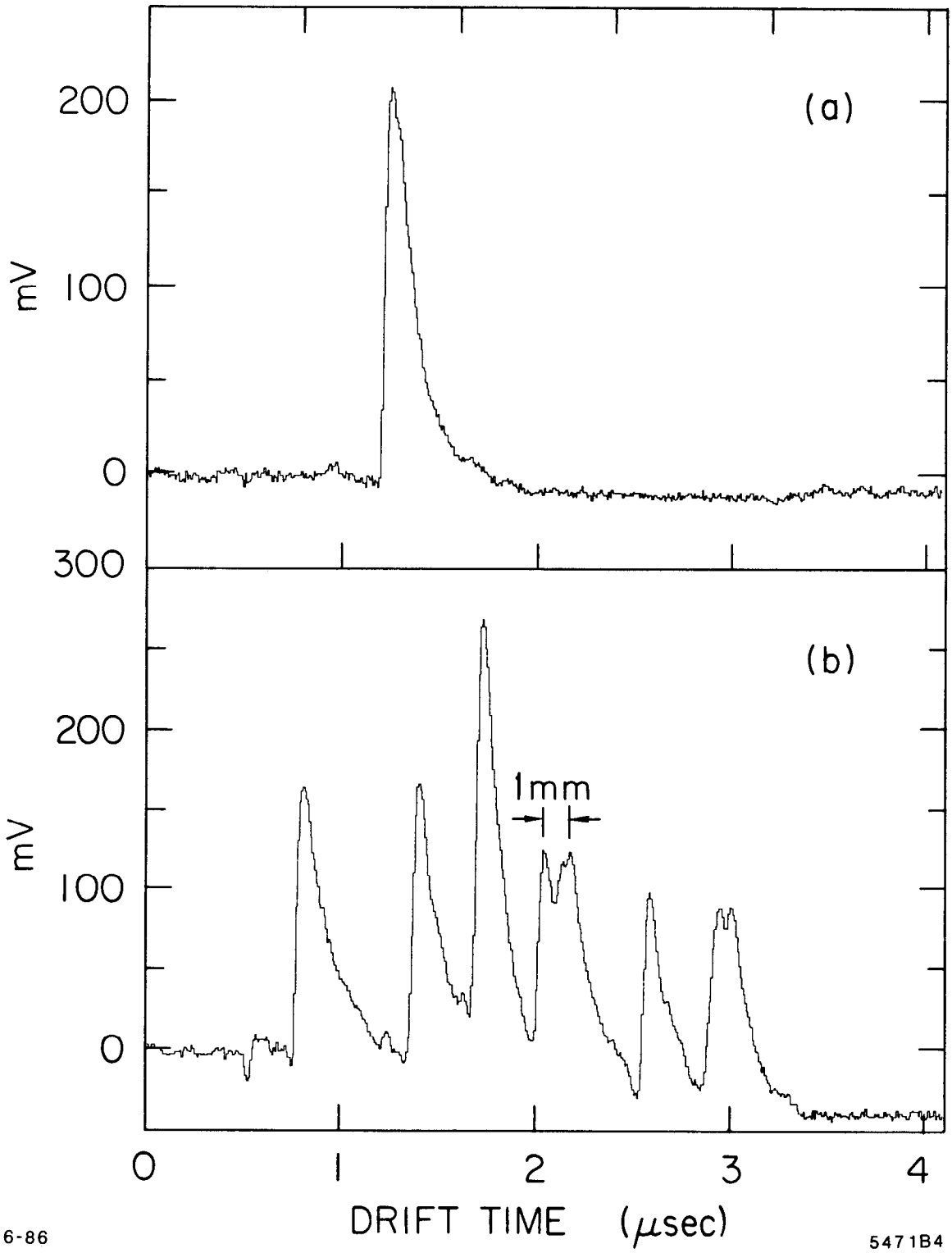
Fig. 3


200
100
0
mV
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200
100
0
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1mm
0
1
2
3
4
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Fig. 4

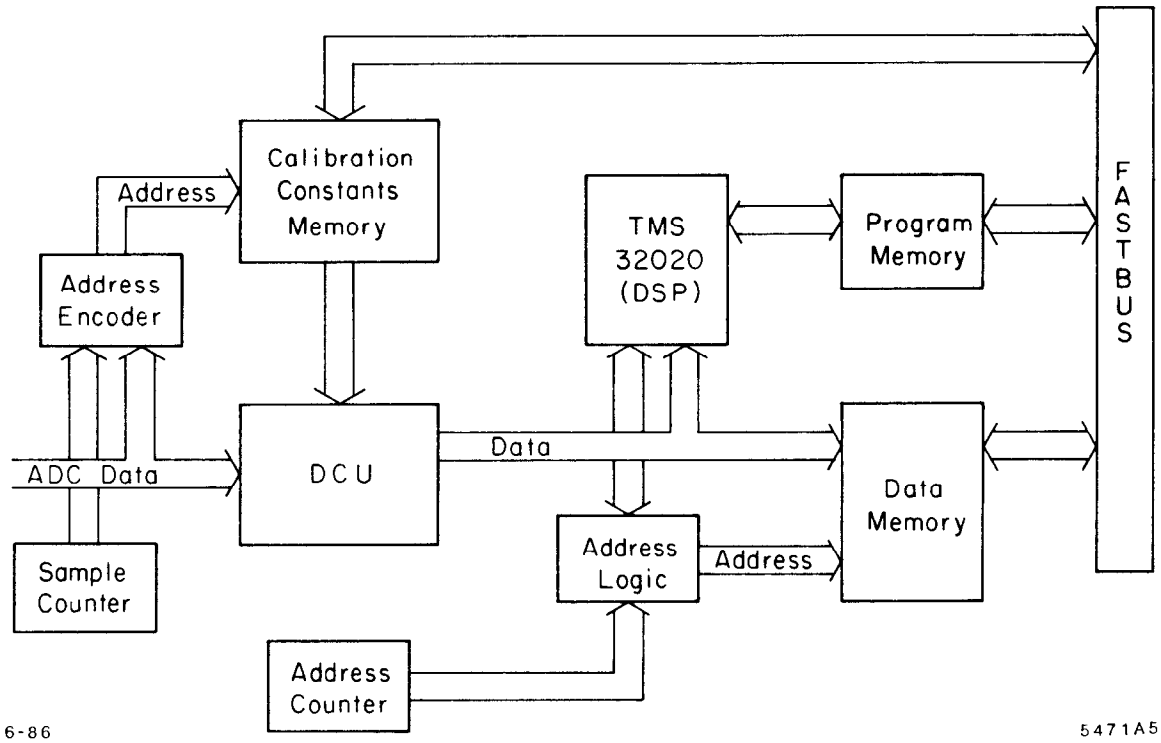
Calibration
Constants
Memory
Address
Address
Encoder
TMS
32020
(DSP)
Program
Memory
FASTBUS
ADC Data
DCU
Data
Data
Memory
Address
Logic
Address
Sample
Counter
Address
Counter
6-86
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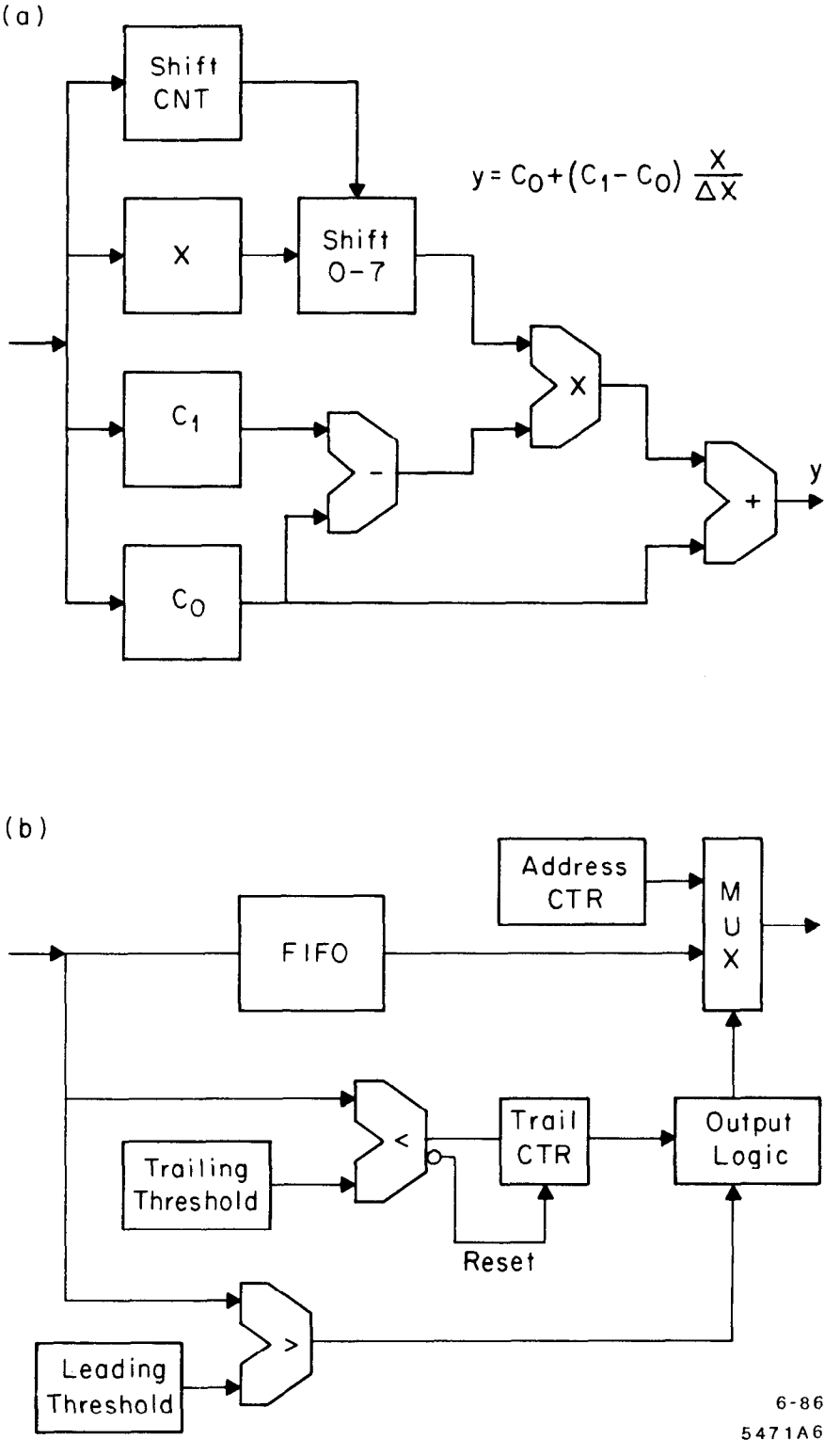
Fig. 5


(a)
Shift CNT
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$y = C_0 + (C_1 - C_0)\frac{X}{\Delta X}$
(b)
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Fig. 6