SLAC-PUB-3241
October 1983
(I)

DATA ACQUISITION AND FASTBUS FOR THE MARK II DETECTOR*

A. J. Lankford and T. Glanzman
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

The architecture of the data acquisition system for the upgraded MARK II Detector is sketched. FASTBUS electronics planned for the system are discussed.

Introduction

The MARK II Detector, built by the SLAC-LBL collaboration for studies of e^+e^- collisions in the SPEAR and PEP storage rings at the Stanford Linear Accelerator Center, is being upgraded for studies of Z^0 production and decay at the new SLAC Linear Collider (SLC). Figure 1 illustrates the major detector components, and Table I outlines these components and some general characteristics of their data acquisition electronics. Test runs with the upgraded detector at PEP will start in October 1984. Physics studies with the upgraded detector at SLC are expected to start by January 1987. The upgrade

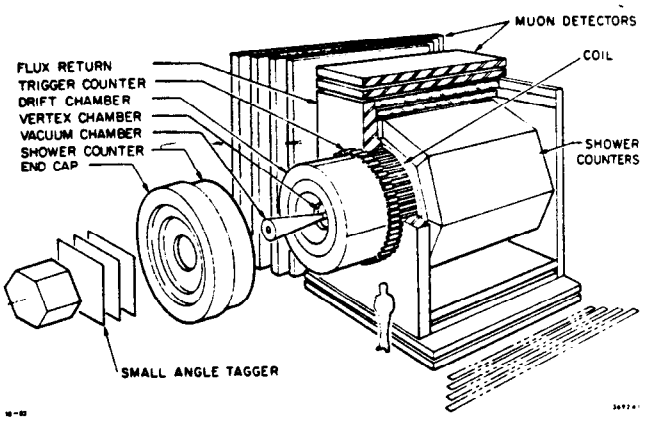

Fig. 1. Isometric view of the MARK II detector showing some of the major detector components.

Table I. Summary of MARK II detector components and readout characteristics.

Detector Component	Variables Measured		Module type
Total # Channels	Channels/Module	# Crates	Subsystem Standard
Central Drift Chamber	Drift Time		TDC
6000 ch	96 ch/mod	3 cr	FASTBUS
Central Drift Chamber	Energy Loss, Drift Time		FADC
6000 ch	18-24 ch/mod	12-16 cr	FASTBUS
Central Drift Chamber	Trigger Logic		FPLA + RAM
6000 ch	96 ch/mod	—	FASTBUS auxiliary*
Trigger Counters	Time of Flight		TAC + ADC
200 ch	8 ch/mod	2 cr	CAMAC
Trigger Counters	Energy Loss		Sample & Hold + ADC
100 ch	4 ch/mod	—	CAMAC*
Shower Counters	Energy Loss		Sample & Hold + ADC
6600 ch	32 ch/mod	12 cr	CAMAC
	(32-96 ch/mod)	(4-12 cr)	(FASTBUS)†
Muon System	Latched Hits		Latches + Shift Registers
3000 ch	32 ch/mod	4 cr	CAMAC
Trigger Chamber	Drift Time		TAC + ADC
600 ch	32 ch/mod	2 cr	CAMAC
Small Angle Monitor	Drift Time		TAC + ADC
300 ch	32 ch/mod	1 cr	CAMAC
Small Angle Monitor	Energy Loss		Sample & Hold + ADC
32 ch	32 ch/mod	—	CAMAC*
Secondary Vertex Detector	Drift Time		Waveform Sampling
500 ch	18-64 ch/mod	1-2 cr	FASTBUS†

* System shared with previous measurement.
† Possible system.

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

Invited talk presented at the Nuclear Science Symposium, San Francisco, California, October 19-21, 1983.

involves an increase in the electronic channel count by more than a factor of two, and the new physics to be studied involves a further increase of nearly a factor of five in the number of particle trajectories measured per trigger. Consequently, although the trigger rate for the detector is not expected to increase from its current value of $\sim$ 2 Hz, the data rate will increase by an order of magnitude. This increase requires substantial changes in the data acquisition system; however, the overall data rate of approximately 80K Bytes per second is not large.

Features of the data acquisition system, as currently planned, are shown in Fig. 2. We have chosen to incorporate new data acquisition modules into a FASTBUS system while retaining existing data acquisition modules in a CAMAC system. Readout of FASTBUS modules will be via SLAC Scanner-Processor (SSP) modules; readout of CAMAC modules via BADC's.[1] The FASTBUS data acquisition crates will be arranged on cable segments connected to a FASTBUS system crate. CAMAC data will eventually be read into this FASTBUS system crate as well. The system crate segment will be connected to an interface to the host computer as well as to a segment containing preprocessors which are in turn interfaced to the host computer via FASTBUS. The upgrade nature and the schedule of the project dictate that the system architecture be initially simple, but flexible and capable of evolution. This paper sketches the architecture of the upgraded MARK II data acquisition system, placing some emphasis on the constraints upon the system and on the evolutionary aspects of the system.

Data Acquisition Modules

The detector subsystems and the data acquisition modules which will read out the detector signals are summarized in Table II. Most of these subsystems are currently readout by CAMAC electronics[2] or will be suited to these existing designs. However, the new central drift chamber will require approximately 6000 channels each of time digitization and of waveform sampling, as well as inputs from these channels to the CAMAC-based charged particle trigger processor.[3] These electronic subsystems are being built in FASTBUS. The time digitization, which digitizes drift time in 2 nsec bins and is capable of digitizing multiple hits on the same wire, will be performed by commercially available TDC modules.[4] The trigger logic which is FPLA and RAM-based will connect to the FASTBUS auxiliary connector behind the TDC's and will be controlled and down-loaded through fourteen CSR locations in the TDC modules. The waveform sampling will be performed by SLAC-designed 6-bit 100 MHz FADC modules, possibly utilizing a compressed scale. The electromagnetic shower counters will require analog-to-digital conversion with a dynamic range of between 12 and 14 bits for about 6600 channels. This range may be provided by existing SLAC-designed CAMAC modules, or it could be provided more comfortably by a new design, which would be in FASTBUS. Early tests of the shower counters will determine which ADC system is chosen. Finally, a high-precision secondary vertex detector of drift chamber design would require waveform sampling, possibly with higher sampling speeds than the system described above. Electronics for this detector component, which would be approximately 500 channels, would probably be built in FASTBUS.

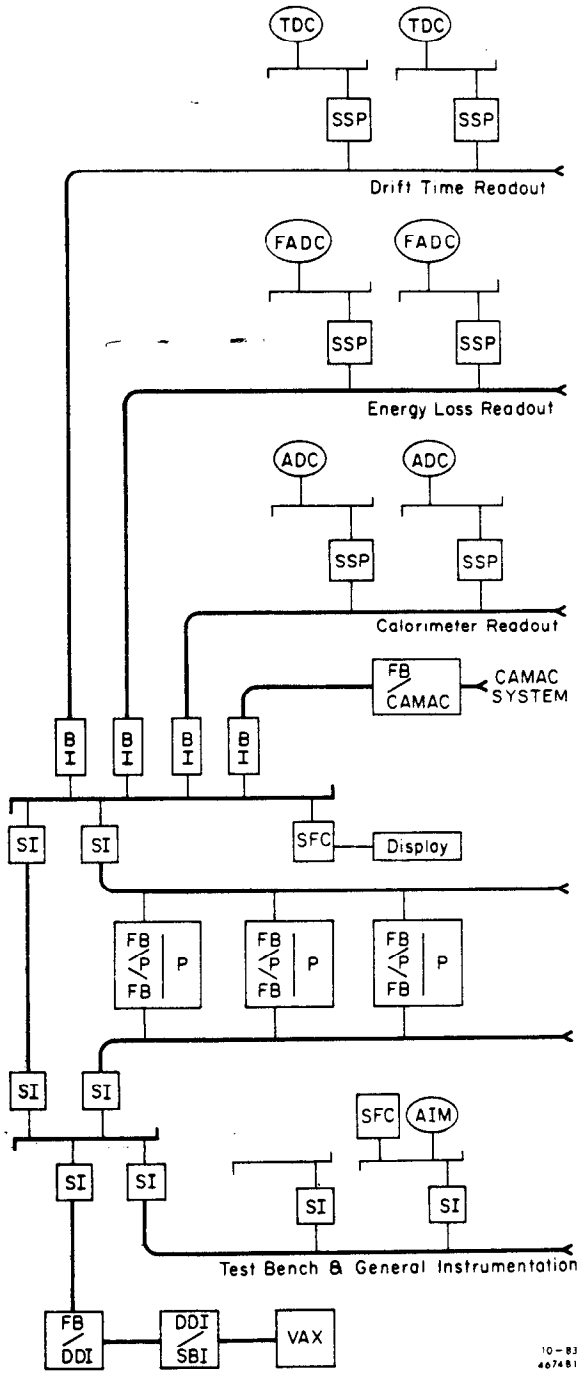

Fig. 2. Block diagram of FASTBUS system architecture for the MARK II Detector.

Table II. Summary of FASTBUS modules shown in Fig. 2.

Symbol	Description	Design/Status	References
Data Acquisition Modules			
TDC	Time-to-digital converter	LeCroy 1879	Ref. 4
ADC	Analog-to-digital converter	possible system	see text
FADC	Flash ADC module	SLAC design	in progress
AIM	Scanning ADC	Transiac FB2064	Ref. 8
Triac	Digital I/O module (not shown in Fig. 2)	Kinetics F400	Ref. 9
Processors and FB Support Modules			
SSP	SLAC Scanner-Processor	SLAC design	see text
SFC	SLAC FASTBUS controller	SLAC design	Ref. 7
P	3081/E Processor	SLAC-CERN design	Ref. 6
FB/P/FB	Dual-port FB-3081/E Interface	concept only	—
FB/CAMAC	Interface	concept only	—
BI	Buffered Interconnect	concept only	see text
SI	Segment Interconnect	—	Ref. 11
FB/DDI, DDI/SBI	FASTBUS-VAX interface	—	Ref. 5

SLAC Scanner-Processor Modules

Readout of FASTBUS data acquisition modules will be via SLAC Scanner-Processor (SSP) modules. These scanner-processors will be involved in several data acquisition activities:

1. Readout of data acquisition modules.
2. Detector subsystem calibration.
3. Segment verification.
4. System test procedures.
5. Other FASTBUS activities, such as system initialization.
6. Self-test procedures.

The SLAC Scanner-Processor is being designed with the following general FASTBUS characteristics:

1. Double-width FASTBUS module with capability to be physically connected to both a crate segment and a cable segment.
2. Capability to be attached as a device to either the crate segment or the cable segment, but not simultaneously to both. However, the scanner-processor can be addressed and return a BUSY on one segment while it is attached to the other segment. Addressing is geographical only.
3. Capability to be a master or a slave on either segment.
4. Support of block transfers of 32-bit data. Maximum transfer speed will be between 120 ns to 150 ns per 32-bit word.
5. Support for other ordinary FASTBUS I/O operations at reasonable speeds (faster than CAMAC).
6. Allow full FASTBUS access from one segment to all modules on the other segment. However, such operations are accomplished by requesting that the scanner-processor perform the operations.
7. Proper FASTBUS response to WAIT to allow single-step through I/O operations.

In addition, the SSP's have the following processor characteristics:

8. 32-bit CPU (8 × AM2901C).
9. Prom implementation of as many as 256 instructions.
10. 4K × 32-bit program memory.
11. 32K × 32-bit data memory, full-word or half-word addressable.
12. Support of full set of IBM Assembler integer instructions (no byte manipulation) plus an extensive set of microcoded FASTBUS I/O primitives.
13. Support of subroutine instructions and provision of macros for optimized FASTBUS I/O operations.
14. Support software for handling of error and I/O conditions.
15. Support of breakpoints and single-stepping for debugging.

Source code for the scanner-processor can be written in IBM Assembler or in FORTRAN followed by a compilation into Assembler. The Assembler code is then translated and linked on a host computer into an executable image which is downloaded to the scanner-processor via FASTBUS. A symbolic debugger running on the host computer is also expected.

The procedure for readout of data, which is the principal function of the scanner-processors, will be:

1. Initiate readout via FASTBUS or via START pulse.
2. Block transfer data from data acquisition modules to local scanner-processor memory.
   (a) In the case of TDC readout, the data will already be sparse-scanned.
   (b) In the case of FADC readout, the data will not already be completely sparse-scanned. The SSP will first interrogate the FADC module as to which channels have been hit and then will readout those channels.
3. Preprocess the data, restoring it in local memory.
   (a) In the case of TDC data, preprocessing consists of (i) reordering the data, (ii) applying channel-by-channel pedestal corrections and gain corrections, if necessary, (iii) relabeling the data with logical addresses, and (iv) computing pointers for output of the data in a logical record.
   (b) In the case of FADC data, reordering is unnecessary; however, sparse-scanning of the samples of each channel must be done. In addition, some quantities such as pulse height and drift time may be derived at this stage.
4. Signal completion via FASTBUS or via an output level.

Readout of other FASTBUS data acquisition subsystems for shower counters or vertex detector would follow similar procedures.

The design of the SLAC Scanner-Processor is nearing completion and prototype work has begun. Production modules are required by the experiment by October 1984. Future versions of the scanner-processor (perhaps even the first production version) may include some of the following features: increased program memory size, increased data memory size, dedicated multiplier, response to broadcast operations, FASTBUS look-through between segments.

System Readout

Data collected from acquisition modules by scanner-processors will be read out via a FASTBUS system crate (see Fig. 2). The capability of connecting a cable segment directly to the scanner-processor eliminates the need for separate segment interconnects (SI's) to the data acquisition crate segments; however, the capability of the scanner-processors to be slaves on the crate segments allows read out via SI's as well. The architecture shown in Fig. 2 without SI's in the data acquisition crates is the configuration expected.

Interconnection to the FB system crate segment may be through buffered interconnects (BI's), as shown in Fig. 2. Buffered interconnects are devices which implement segment interconnection without synchronized FASTBUS protocol on the two segments. They would allow matching of different data transfer rates on the two segments. For instance, if the transfer rates on each long cable segment to the FB system crate from data acquisition crates are about 600 ns/word and the transfer rates from the FB system crate are about 200 ns/word, then three BI's on three long cable segments would allow maximum transfer rates through the system crate. Each BI would read out its cable segment into a local buffer and would compete for mastership with the other BI's in order to transfer its buffer contents onto the FB system crate segment.

The SLAC Scanner-Processor is a candidate BI device; however, BI functions could be provided by a more simple device. An SI could be used in parallel with a simple BI in order to provide more efficient execution of random FASTBUS operations – the BI being used for block transfers only. In the MARK II application, the increased transfer efficiency afforded by BI's will not be a requirement; consequently, SI's could be substituted since the scanner-processors in the data acquisition crates could then exercise mastership on the FB system crate segment.

The FASTBUS system crate will allow several processors access to an entire event. In order that data acquired by existing CAMAC electronics will be available to each of these processors, a FASTBUS-to-CAMAC interface incorporates the CAMAC system into the FASTBUS system. This interface will allow all CAMAC instructions to be issued via the FASTBUS system and will be compatible with existing SLAC CAMAC hardware and software.

The FASTBUS system crate will be connected via a VAX-FB system crate to the interface to the host computer. This interface is described in detail in Ref. 5. Basically, it consists of an interface from FASTBUS to DDI (VAX DR-32 Device Interconnect), which is a 32-bit wide bus provided by a DEC DR-780 channel to the VAX SBI (Synchronous Backplane Interconnect). This interface allows block transfer rates of 700 nsec per 32-bit word and is currently operating on the existing VAX-11/780 computer. This VAX may be replaced by a more powerful VAX in the future.

On-Line Processor Subsystem

A set of on-line processors will be connected to the FASTBUS system crate. This connection is currently thought of as a FASTBUS cable segment. The processors are expected to be emulators of the IBM 3081K. These 3081/E's[6] will be connected to FASTBUS by a quasi-dual-port interface which will act as a FASTBUS slave on either of two cable segments. The 3081/E is currently being designed and built at SLAC and CERN. Availability is expected for later 1984. The FASTBUS-to-3081/E interface has yet to be designed. Since data transfer rates will not be critical, the MARK II FASTBUS architecture could be modified to accommodate a single-port interface.

The 3081/E's will be used to further preprocess data from the FADC system, to associate and merge the data from the TDC and FADC systems which will all originate from the central drift chamber, and to place all data in the final format for tape. In addition, the 3081/E's could preprocess each event, flagging interesting events. Memory capacity (3.5 MB initially, and 14 MB perhaps in 1985) and the emulator structure will permit on-line execution by a 3081/E of virtually any program developed to run off line on the 3081K. Full off-line event reconstruction will be run on line in order to monitor detector performance.

Although the entire acquisition system will be fully operational under direct control by the VAX, a SLAC FASTBUS Controller (SFC)[7] located in the FASTBUS system crate has been included in the system architecture to more efficiently supervise data transfer from the acquisition segments to the processor segment. The SFC might supervise as follows after

having been informed of a trigger:

1. Select next target 3081/E. Set up target 3081/E data memory addresses for each buffered interconnect. Initiate parallel readout of cable segments by BI's.
2. Pause, allowing BI's to gain mastership of system crate and processor cable segments for data transfer.
3. Periodically awaken. Gain bus mastership, poll BI's and processors to check status, and update status display. Release segment if readout is incomplete.

Production SFC modules and support software currently exist with both 68000 and 8086 microprocessors. The greater speed of the 68000 is better suited to the supervisor application. Such a dedicated supervisor with status display should provide superior monitor and diagnostic facilities for the multiprocessor system. The supervisor could also perform some initialization and calibration tasks.

General Instrumentation

The VAX-FB system crate segment will also interconnect to a cable segment which will in turn interconnect to a crate segment containing general instrumentation electronics and to a FASTBUS crate at a test bench. The general instrumentation electronics will consist of readout of DC voltages, such as thermocouple responses, and output of control signals. Analog Input Modules (AIM's),[8] which are 64-channel microprocessor-controlled scanning ADC's, and Digital Input Output Modules[9] are currently being tested. This instrumentation will be monitored in parallel by the VAX host computer and by a SLAC FASTBUS Controller which will provide back-up for each other. The SFC applications program will be written in FORTRAN in order to share code with the more complex VAX monitor program.

Staging

The schedule for the MARK II upgrade, starting with some data-taking in 1984 and continuing into 1987, allows and requires that development of the data acquisition system be staged. The first stage will consist of the CAMAC system being read out directly into the VAX via the existing VAX CAMAC Channel (VCC)[10] and the addition of a much simplified FASTBUS system. The simplified FASTBUS system could consist of a single cable segment with interconnects to each of four data acquisition crates via SLAC Scanner-Processors and to test bench and general instrumentation crates when segment interconnects become available. As more data acquisition crates are added to the system, the first 3081/E preprocessor and its FASTBUS interface will be needed. Finally, as all data acquisition crates and preprocessors are added to the system, the FASTBUS system crate, buffered interconnects, supervisor, and the FASTBUS/CAMAC interface will be incorporated into the system.

Acknowledgements

The authors would like to acknowledge the support of the MARK II collaboration (Caltech-Colorado-U.C. Santa Cruz-Hawaii-Johns Hopkins-LBL-Michigan-SLAC), the contributions of H. Brafman, B. Bertolucci, S. Deiss, H. Kang, L. Paffrath, and other members of the SLAC Electronics Department to the FASTBUS architecture and hardware, and the significant contributions of J. T. Carroll to the conception of the system and its components and of E. J. Siskind to the hardware and software of the FASTBUS interface.

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