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REVIEW OF RECENT FASTBUS DEVELOPMENTS*

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Abstract

The status of the FASTBUS Specification for modular data acquisition and control systems is reviewed. Recent developments at research laboratories and available support from commercial manufacturers are highlighted. Covered are hardware developments and system implementations in the U.S.A., Canada and Japan. FASTBUS in Europe and software efforts are described in separate papers at this Conference.[1,2]

Introduction

FASTBUS is a standardized modular data bus system for data acquisition, processing and control. A typical system (Fig. 1) consists of crate segments, cable segments, modules and host computers. Basic categories of modules are processor interfaces, segment interconnects, masters, slaves and diagnostic modules. FASTBUS segments utilize a 32-bit wide bus for multiplexed address and data, asynchronous transfers with handshake protocol (AS-AK, DS-DK), several addressing and data transfer modes, arbitration with priority levels to resolve bus contention between master modules on the same segment and autonomous operation of individual segments. The evolution of the FASTBUS Specification has been reported on at previous Nuclear Science Symposia[3] and a basic introduction has been published.[4]

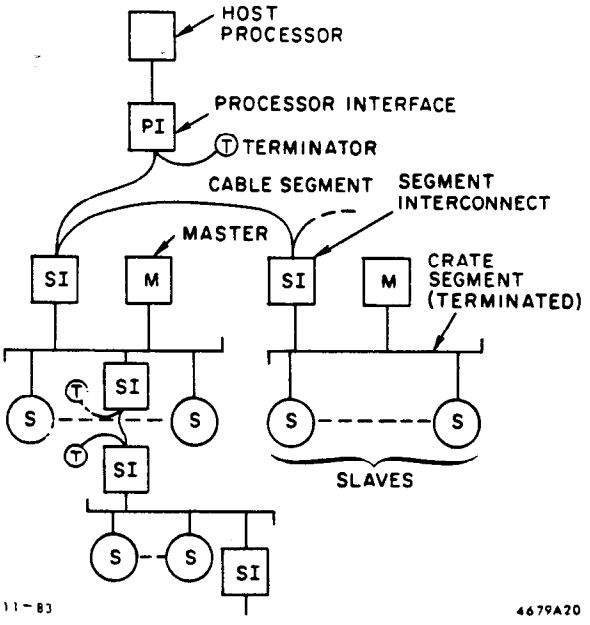

Fig. 1. Example of FASTBUS system topology.

FASTBUS Specification Update

Specifications have been distributed in the form of a U.S. NIM Committee document dated November 1982 with two Addenda and Errata dated 15 July 1983 and 27 September 1983.[5] They have been submitted to the U.S. Department of Energy for processing and printing and have been listed as project P960 by the IEEE Standards Board. A European version has been published.[6]

Major updates contained in the Addenda and Errata are, in summary:

Page 4-11	:	All devices shall implement a NTA except if only geographically addressable and only with CSR#0.
Page 6-7	:	A Master shall generate AR only if both CSR#0⟨01⟩ (ENABLE) and CSR#0⟨02⟩ (RUN) are set.
Page 7-3	:	GAC generates SS = 0, 6 or 7.
Page 8-7	:	New description of CSR#0 bits S01 and S02 concerning AR generation by Masters.
Page 10-16	:	New SS = 7 for data failure.
Page 13-3,-4	:	Module circuit board outline and details clarified in Figs. 13.1(a) and (b).
Page 13-5	:	Box connectors without guide notches deleted.
Page 13-11	:	Die temperature reduced to 85°C.
Page 13-12	:	Module air cooling specifications revised.
Page A-5	:	Table A.1.2 timing specifications for ECL revised.
Sec. C	:	Cable segment specifications and details revised.

FASTBUS Developments at Research Laboratories

Current hardware development efforts and system implementation proposals at research laboratories and universities are summarized.

1. Fermi National Accelerator Laboratory – FNAL

(a) General Hardware. Prototypes or small production quantities have been completed of a wire-wrap kluge card, an Active Extender, the Unibus Processor Interface (UPI), IORFI2 interface, FDM display and Test Memory modules. The latter three are shown in Fig. 2.

In collaboration with University of Illinois (UI) the development of a PC version of the Segment Interconnect (SI) module and a self-contained rack cooling system for three FB crates is in progress. A prototype crate segment backplane is being fabricated with increased trace inductance with the aim of achieving a characteristic impedance of 50Ω for a fully loaded crate.

(b) Custom Interface Integrated Circuits. A collaboration of FNAL, CERN, SLAC, UI, TRIUMF and KEK is working on the design of interface circuitry for master and slave modules utilizing macrocell gate array logic. The proposed interface is shown in Fig. 3. It consists of a Protocol (PCL) chip, two Address Data Interface (ADI) chips and ECL transceivers to

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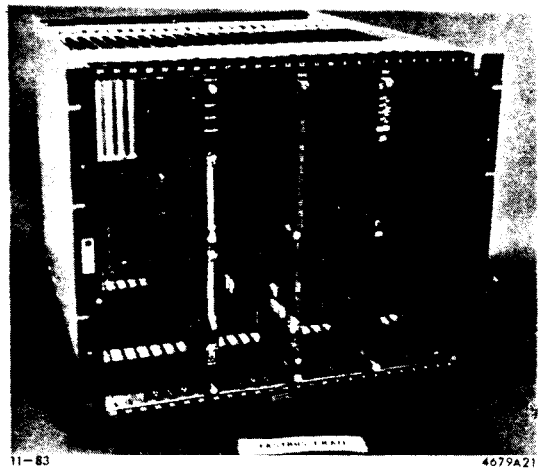

Fig. 2. Crate with IORFI, display and test memory modules.

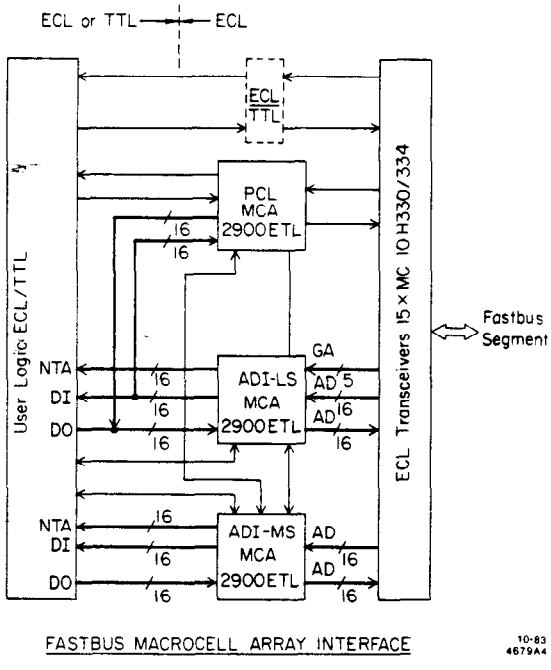

Fig. 3. FASTBUS macrocell gate array interface.

attach to the FB segment. The PCL chip will contain master arbitration logic with two arbitration level registers, broadcast CSR#7 register with decoding and compare logic, MS decoding, AS-AK and DS-DK generation with user handshake, parity control, SS handling with latches and ADI control.

The ADI chip is of 16-bit width with data bus input and output latches and buffers, CSR#3 logical address register and compare logic, NTA register with counter and decoding logic, address word width control for CSR#3 and NTA, parity checking and geographic address comparator. An ECL chip set and an ECL/TTL mixed IO chip set are being planned. Gate array integrated circuits in production quantities are hoped for in one year.

(c) Experiment E401, 400. Collaboration with UI utilizing a single segment FB system (see description under UI).

(d) Collider Detector Facility – CDF. This detector facility for the 2 TeV antiproton-proton collider will utilize a FASTBUS data acquisition and control system.[7]

The detector will have 75K signal channels and utilize 42 crate segments linked by 3 cable segments and 44 SI modules. Front-end electronics are housed in 130 Rabbit crates (non-FB) which are interfaced to FB crates. One VAX 780 host computer and 8 each VAX 730 secondary control computers are planned. Several FB modules are under development: Clock Generator, Trigger ID, MEB/P Multi-Event Buffer/Port, TS Trigger Supervisor, C&S Clear and Strobe Crosspoint, Done Crosspoint, Event Builder - Reformatter, Buffer Manager and FSM Segment Monitor.

The schedule calls for a phased installation over two years starting in 1984.

(e) Experiment E653. This experiment will have 11 crate segments with LeCroy 1800 series TDC and ADC modules and several UPI interfaces. Operation is expected by late 1984.

(f) Experiment E706. This experiment is also considering the use of several FB crate segments with LeCroy ADC modules and a UPI . Implementation is scheduled in 1985.

2. University of Illinois – UI

(a) General Hardware. Collaboration with FNAL on a self-contained rack cooling system for 3 FB crates utilizing 3 air-water heat exchangers. Each crate will handle 3 KW of power dissipation. A prototype rack assembly will be ready for testing by December 1983. Participation in the design review and generation of user information for the custom interface chips. Study of a buffered interconnect module with an Ethernet or fiber-optic link.

(b) Segment Interconnect – SI. UI is completing more than 20 wirewrap modules of the Type S-1 design (FB Specification Appendix E).[8] These units will be equipped with the cable segment interface described in part (c) below. Jointly with FNAL a PC version will be built in early 1984.

(c) Cable Segment Implementation. An interface design utilizing a custom hybrid quad differential ECL driver has been developed with CERN.[9] Details are also given in Appendix C of the FB Specification. Compatible cable segment ancillary logic hardware is being designed.

(d) Experiment E401, 400. The high-speed data acquisition system[10] used for these experiments employs a single crate segment with a UPI interface. The original prototype system has been upgraded to 4 each memory modules of 2 MByte capacity paired with 4 channel controller modules.

3. Brookhaven Nationa Laboratory – BNL

(a) Experiment E749. This BNL-Yale collaboration uses an early prototype version of FASTBUS and is incompatible with the present specification. The system consists of three water-cooled crate segments linked by one cable segment, a Unibus cable interface, 4 SIs and a complement of application modules.[11]

(b) MPS – Multi – Particle Spectrometer. A single segment system with TDC digitizer modules has been operated since February 1982. A new replacement system is in prepara-

tion. The VAX 750 host computer will be interfaced with the LeCroy 1821 and the use of 1878/79 TDC modules is contemplated. Specially designed modules will be used to connect the existing detector hardware. The MPS II system is expected to be operational by $\sim$ 1/85.

4. Los Alamos National Laboratory – LANL

A general-purpose development of a master module based on a 32-bit microprocessor is in the conceptual design stage.

(a) Weapons Neutron Research Facility – WNR. Single crate data acquisition stations are under development. The crate segment will be interfaced with a LeCroy 1821 to the VAX host computer. Special modules being designed at LANL include master clock, TOF, memory and processor units. The project envisions the first data acquisition station by 10/84; six stations by 1986; a total of 10 to 12 stations in the future. For this effort a development crate with a CERN IORFI is being assembled.

5. Lawrence Berkeley Laboratory – LBL

A single crate segment development system with a PDP11/23 and an IORFI interface will be available in a few month. In a collaboration with the University of Tokyo design work for the TPC of the TOPAZ detector at KEK is in progress. The work includes detector FASTBUS data acquisition configuration, Digitizer CCD module, Sequencer module and control modules for amplifiers and test pulsers.

6. Cornell University Medical College

A data acquisition system with one FB crate has been operated for imaging coronary arteries.[12] The VAX 780 computer is connected with a prototype DDI-FB interface. A master module and a memory controller module transfer image data from a VICOM digital image processing system via the FB segment to the Intel 64 MByte bulk memory crate at a 37 MHz word rate. Presently the addition of three memory crates and controller modules is in progress.

7. TRIUMF Laboratory, Canada

Technical editing of the FASTBUS Specification is being carried out at TRIUMF. Some prototype hardware utilizing FB packaging has been built for the TPC detector. TRIUMF will be participating in the development of custom interface chips with design review, generation of typical PC artwork for PCL, ADI and transceiver chips and cooling tests for prototype 2900 ETL chips.

8. KEK National Laboratory for High Energy Physics, Japan

(a) General Hardware. In collaboration with Japanese commercial manufacturers KEK is developing several general-purpose modules: four-layer universal PC board, bus display module, switch and display module, CCP-FPI interface module[13] for NEC PC-8000, 68K-FPI master module with 68000 CPU,[14] crate and cable segment ancillary logic modules (ATC and GAC), SSI simplex segment interconnect module[15] and memory module. Most of these modules are in the PC layout stage, some are already commercially available.

(b) VAX – FPI Interface. Commercial version of DDI-FB interface[16] developed by DEC Japan and KEK.[17] Prototype is in testing; production units will be available in Spring 1984.

(c) Protocol IC FMA601. Custom interface integrated circuit for AD lines implemented with Motorola MCA 600 macrocell array. Design provides 8-bit data path, CSR#3 logical address register and compare logic, parity checker and IO buffers and latches. Chip samples are expected by November 1983. KEK will participate in the design review of the FERMILAB chip set described earlier.

(d) TRISTAN Intersecting Storage Ring. This e^+e^- storage ring for colliding beam experiments at 60 GeV center-of-mass energy will use a FASTBUS accelerator control system. Construction of the ring is in progress with completion scheduled by 1986.

(e) TOPAZ and VENUS Detectors for TRISTAN. Both detectors will utilize a FB data acquisition system. Configuration design and module developments are in progress. For the TOPAZ TPC a Digitizer CCD module, a Sequencer module with 8088 microprocessor and bit slice sequencer and several control modules are under design (see LBL collaboration). For the VENUS detector a TDC system composed of TAC modules and an ADC module (similar to CAMAC BADC at SLAC) is under development. The TOPAZ system will have approximately 100 crates, of which 50 crates are used for front-end amplifiers and the balance to accommodate $\sim$ 800 FB modules. The VENUS data acquisition system will entail 25 crates with approximately 400 FB modules.

9. Stanford Linear Accelerator Center – SLAC

(a) General Hardware. The SFC controller with multibus MPU[18] has been tested as a PC prototype with 8086 and 68000 processor boards. Fabrication of 16 modules is in progress. The SNOOP diagnostic module[19] has been tested as a prototype and is undergoing PC artwork corrections. This will add the 68000 control processor to the ECL section PC board. In early 1984 a small production run of modules is being planned. High-speed multisegment tests are scheduled with the SLAC sequencer and memory modules and prototype SI units.

An improved bench test box, FASTBOX2, for module checkout has been completed (Fig. 4). A revised lightbar bus display is partially complete. Several units of a compact power supply for FB crates have been assembled. These are used for development stations where only small amounts of current are required. A passive extender module is currently in PC layout.

SLAC is participating in the custom interface chip development effort with design review and the CAD processing coordination of one of the macrocell array integrated circuits with Motorola.

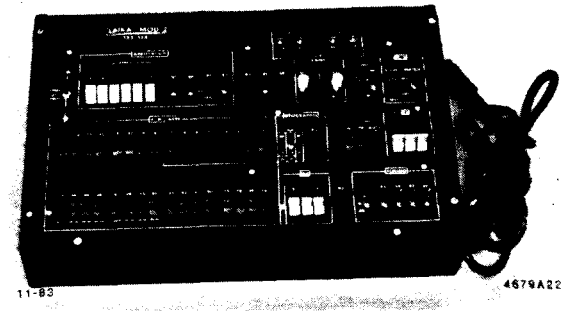

Fig. 4. Manual test box.

(b) MARK II Detector Liquid Argon Control System. This is the first FASTBUS application system at SLAC. The single crate segment system (Fig. 5) consists of the prototype VAX DDI-FB interface[16] with simple buffer and terminator modules to connect to the crate segment,[20] a SFC master module, Transiac FB2064 DVM modules (Fig. 10) and KSC F400 Triac modules (Fig. 7). All hardware for this system is available and will be installed by December 1983. Later in 1984 this system will be connected with a SI unit to the new MARK II/SLC data acquisition system.

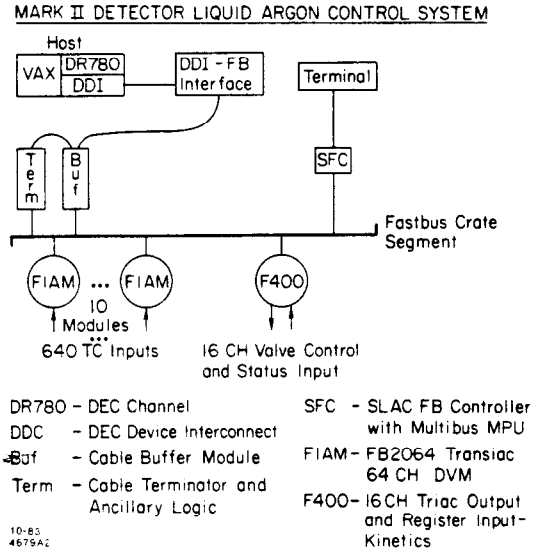

Fig. 5. MARK II detector liquid argon control system.

(c) MARK II/SLC Detector FASTBUS Data Acquisition. Upgrading of the MARK II detector for use at the SLAC Linear Collider (SLC) will entail a new data acquisition system.[21] There will be approximately 20K signal channels requiring 25 to 30 crate segments. Present system configuration plans utilize nine cable segments. The VAX host computer will be connected with the DDI-FB interface. Major modules on order or under development are LeCroy 1879 TDC, SSP SLAC Scanner-Processor, FADC Flash ADC, and SI units. By Fall 1984 a six crate segment system linked by one cable segment is planned. Completion of the full system configuration is expected by the end of 1986.

(d) SLD Detector Proposal for SLC. This is a proposal for the construction of a new detector for the SLAC Linear Collider. There are approximately 100K signal channels involved. Plans are calling for a FASTBUS data acquisition system of 50 to 100 crate segments. Contingent on final approval, FB development work will commence next year with detector operation expected by 1988.

FASTBUS Products from Commercial Manufacturers

FASTBUS products available now or in the active planning and development stage are summarized. Detailed information is available from each individual manufacturer.

(1) Kinetic Systems Corporation (KSC), Lockport, Illinois

Products available now to two months are: F010 two-layer kluge card, F011 four-layer kluge card, F050 26-position air-cooled crate, F150 crate segment terminator, F151, 152 crate segment ATC, GAC modules, F210 active extender (Fig. 6) and F400 triac output/status input register module (Fig. 7). The F400 module was developed for SLAC. Future products expected in three to nine months are: passive extender card, LSI-11 interface, VAX interface, F290 segment display and F800 front-end processor.

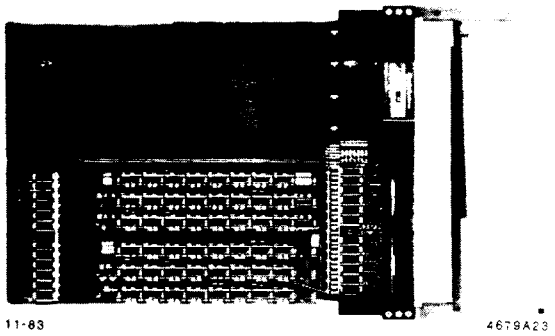

Fig. 6. F210 active extender module.

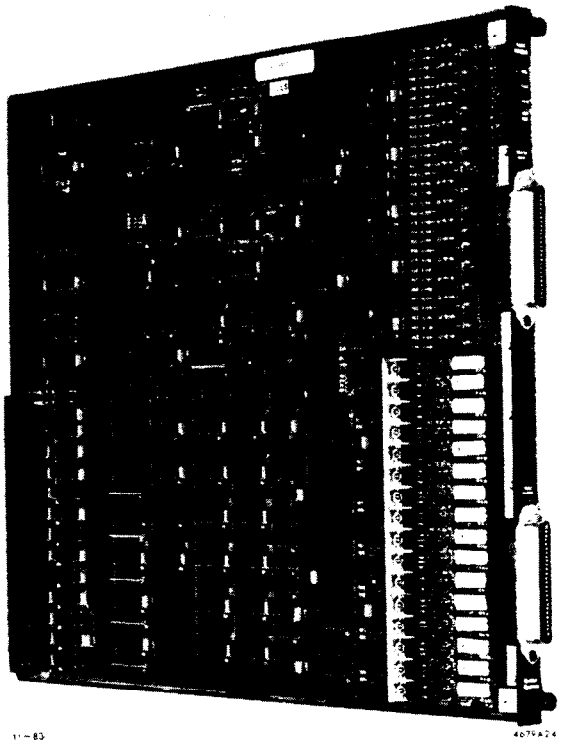

Fig. 7. F400 TRIAC module.

(2) LeCroy Research Systems Corp., Spring Valley, New York

1800 system products available or under development are: 1801 active extender module, 1805 FB starter kit with CAMAC IO register module, FB IO register module and software, 1810 CAT calibration and timing module, 1821 segment management and interface with CAMAC personality card, 1861 ICA 64 channel image chamber analyzer, 1878-79 pipeline TDC with 96 channels, 1882-85 ADC module with 96 channels and 1891 dual port memory.

Figure 8 shows a crate with several 1800 system modules. Figure 9 shows an 1821 SMI prototype.[22]

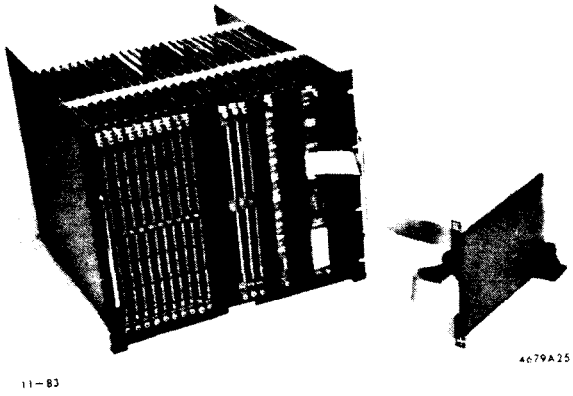

Fig. 8. LeCroy 1800 system.

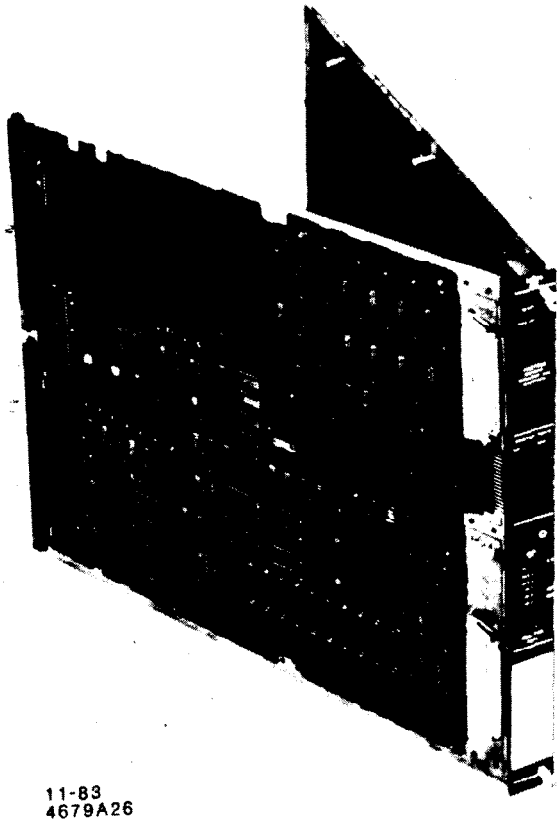

Fig. 9. 1821 segment interface module.

(3) White Data Systems (WDS), Union, Oregon

Products available now to two months are: Type A FASTBUS crate (see Fig. 2), Type W (water-cooled) FASTBUS crate, power supply assemblies, 8152 blower module, 8182 crate status bit module, 8183 crate ancillary logic (ATC, GAC), two-layer kluge board.

Future products expected in three to six months are: passive extender, active extender, lightbar display, diagnostic module.

(4) Transiac, Mountain View, California

FB2064 auto-ranging DVM with 64 channels. This module is based on a SLAC CAMAC design and was developed for SLAC (Fig. 10).

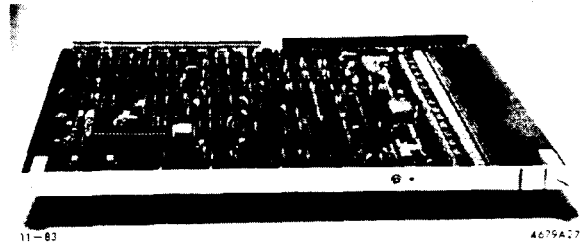

Fig. 10. FB2064 DVM module.

(5) BiRa Systems, Albuquerque, NewMexico

FERMILAB IORFI2 module (Fig. 2) will be available in two months.

(6) Other Manufacturers

Joerger Enterprises, East Northport, New York: scalar modules for BNL (nonstandard protocol).

Jorway Corp., Westbury, New York: Unibus board for FERMILAB UPI.

Todd Products, Brentwood, New York: power supply assemblies for SLAC.

DEC Japan: VAX-FPI for KEK.

Housin Electronics Co., Japan: bus display module, switch and display module, CCP-FPI interface for KEK.

Maruei Shoji Co., Japan: 68K-FPI interface, FMA601 custom IC for KEK.

Toshiba Electronics Co., Japan: digitizer CCD module for KEK.

Summary

Major commitments to the use of FASTBUS as a data acquisition standard for demanding applications have been made to data by several laboratories. Commercial manufacturers have started to supply some hardward and are planning more for the coming year. The increasing momentum appears promising. Printing of the FASTBUS Specification document by the U.S. Department of Energy is expected in early 1984. Processing and publication as IEEE and IEC standards will follow later in 1984 and 1985.

Acknowledgements

Credit for the contents of this report belongs to representatives from all the laboratories and to spokespersons for the manufacturers who kindly provided all the information. Special mention deserve the encouragement and support by R. S. Larsen, L. Costrell and E. Barsotti.

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