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PHASE AND AMPLITUDE DETECTION SYSTEM FOR THE STANFORD LINEAR ACCELERATOR*

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Summary

A computer controlled phase and amplitude detection system to measure and stabilize the RF power sources in the Stanford Linear Accelerator is described. This system measures the instantaneous phase and amplitude of a 1 microsecond 2856 MHz RF pulse and will be used for phase feedback control and for amplitude and phase jitter detection. This paper discusses the measurement system performance requirements for the operation of the Stanford Linear Collider, and the design and implementation of the phase and amplitude detection system. The fundamental software algorithms used in the measurement are described, as is the performance of the prototype phase and amplitude detector system.

Introduction

This paper describes an RF phase and amplitude measurement system being developed for the Stanford Linear Collider (SLC) project. This system measures the amplitude of a 1 μs 2856 MHz pulse used to provide accelerating fields in the linac structure, and measures phase differences between this 1 μs klystron pulse and a distributed cw phase reference line at the same frequency.

The amplitude measurement uses an RF diode as a linear amplitude detector, and the phase measurement uses a double balanced mixer and electronic phase shifter as a nulling detector. The system hardware components consist of a Detector Head physically close to the signal sources (containing microwave and video analog circuitry, digitizing electronics and control logic), and a CAMAC packaged input-output processor module which controls the measurement system and reports calculated results to the SLC control computer system.

Figure 1 is a block diagram of the system and shows the integration of the phase and amplitude detectors into the accelerator RF system. Two phase and amplitude heads are shown in the figure; the actual RF control system uses 240 detector heads to measure the 240 35 MW klystrons of the accelerator RF system.

Readers interested in the principle of the phase measurement technique are referred to an explanation in Reference 1.

System Performance Requirements

The linear collider project under development at SLAC forces very severe constraints on the accelerator RF system. To achieve the SLC design energy, emittance, and luminosity, the RF accelerating fields must be stabilized to prevent possible fluctuating transverse fields which would destabilize the SLC beam. A phase and amplitude detection system is required to measure average phase and amplitude values as well as instantaneous values used for pulse-to-pulse jitter measurement. These measurements are used by the SLC control computer to stabilize the RF system and optimize the beam parameters.

Collider Note 181 specifies the required phase and amplitude detector system performance requirements. Table I summarizes the required jitter detection sensitivity; the requirements are more stringent in earlier linac sectors as any error is multiplied by the gain of the remaining linac sectors.

Table I. Jitter Detection Specification

Sector	Phase Jitter	Amplitude Jitter
2	0.1 degrees	0.1 %
3	0.2 degrees	0.2 %
4-5	0.3 degrees	0.4 %
6-30	0.5 degrees	0.5 %

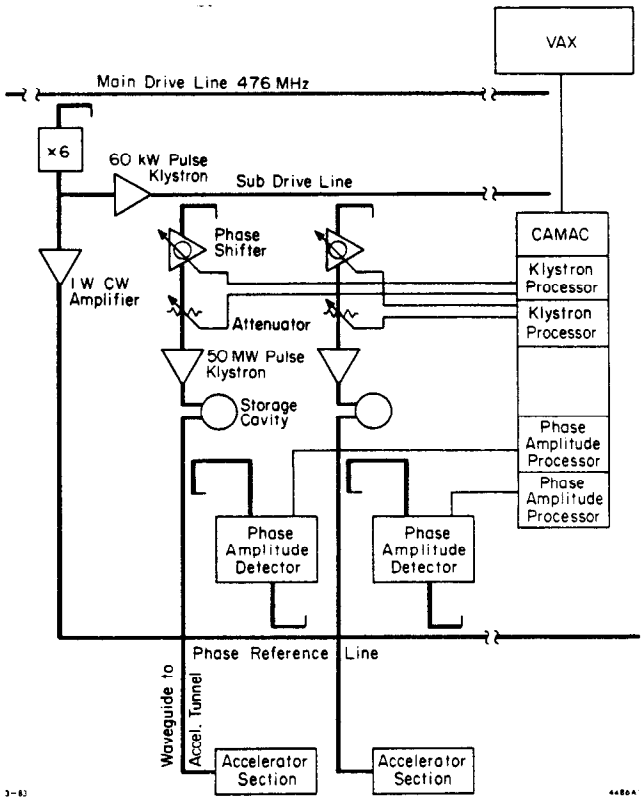

Fig. 1. Detection system integration into accelerator RF system.

An additional system requirement is time stability of the phase measurement, which is required to maintain the proper klystron-to-beam phase relationship. The design goal for this time stability is that the rms phase measurement error of the 240 klystron ensemble be less than 3.6° over a six month time period.[2]

Description of RF Components

Of major importance to the measurement of phase is a stable phase reference signal. This signal has to be available at 13 m intervals for 240 klystron stations along the 3 km accelerator. To accommodate these frequent drop-out points a reference line in an ultra-stable environment was chosen over the option of an electronically measured and controlled line. The coax cable used is a foam dielectric cable insensitive to changes in humidity or atmospheric pressure with a temperature coefficient of ±9 ppm/°C.* Between each drop-out point the cable is coaxially surrounded by a water jacket which is operated at 45°C ± .1°C. This allows a 100 m length of reference line to be stable to <1° in electrical length for ambient temperature changes of 30°C. Each 100 m reference line segment is driven from the SLAC Main Drive Line,[3] which was originally built as a phase stable line with 30 couplers along the 3 km accelerator. Development work is under way to improve the phase stability of this line.[4]

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The RF head of the phase-amplitude detector combines the following circuits or components on a single stripline board: a large signal detector circuit, a drop-in mixer as nulling phase detector, a 180° electronic phase shifter, a ±90° wobbler, DC block capacitors, pill attenuators and directional couplers (Figure 2).

The amplitude detector works on the principle of a large signal detector. A RF signal level as high as 1 watt drives a hot carrier diode which charges a capacitor to the peak RF voltage level. This provides essentially a linear detector mostly insensitive to variations of diode parameters. The dynamic range is about 20 dB with deviations from linearity of less than ±5%.

A double balanced mixer is used as a phase detecting element. It is commercially available as a drop-in package suitable for incorporation into stripline.† High isolation in the order of 40 dB between the LO and RF ports is desirable to reduce errors in the phase measurement. Sepcific error tests also indicate that conventional power levels applied to the mixer ports achieve best results as a phase detector, i.e., constant LO power of 5-15 mW (supplied by the cw reference signal) and RF port levels up to 100 μW maximum. To assure the latter condition the pulsed RF signal is accordingly attenuated with directional couplers and attenuators. The IF port is terminated into 50 Ω for the operating frequency and higher harmonics. A stop band filter is added to prevent the operating frequency from traveling into the phase detection electronics.

The variable electronic phase shifter and ±90° wobbler circuits were described in an earlier paper.[1] The phase shifter uses varactor diodes to achieve a phase shift of 0-180° for a 0-10 V control voltage and deviates only ±5° from the ideal linear response. A 10 dB pill attenuator is inserted between the phase shifter and the mixer to isolate the two circuits from each other.

Figure 3 shows a photograph of the lower half of the stripline circuit board containing all the microwave circuitry. Variable capacitors are part of the upper half of the stripline board in the form of tuning slugs. Plated through holes are provided in the upper and lower half of the circuit boards to create channels to prevent propagation of waveguide modes.

Function Description—Signal Processing System

Figure 4 is a block diagram of the signal processing components, and helps to illustrate the signal paths and control elements of the phase and amplitude detector. The microwave components operate at 2856 MHz and accept as inputs the klystron pulse and the phase reference signals, and produce as outputs analog signals with frequency content that is related to the time structure of the RF pulse's phase and amplitude.

The amplifiers and track/hold functions are implemented with 10 MHz analog bandwidth, which allows a 5 MHz bandwidth for the amplitude vs time and phase vs time measurements of the RF pulse.

A digital-to-analog converter is used to control the voltage variable phase shifter and an analog multiplexer and analog-to-digital converter are used to digitize the amplitude and phase measurements, as well as to monitor the system performance via a temperature measurement, readback of the DAC, and diagnostic measurement of the system power supplies.

The digital control logic is provided to allow control of the timing of the track and hold gates and the phase modulation of the reference signal. These digital functions, as well as the A/D and D/A are controlled through a 256 byte control block via the control processor. This architecture centralizes the analog functions at the signal sources, and uses digital techniques to communicate between the control processor and the measurement head. This noise isolation is significant for system operation in the electrically noisy linac gallery.

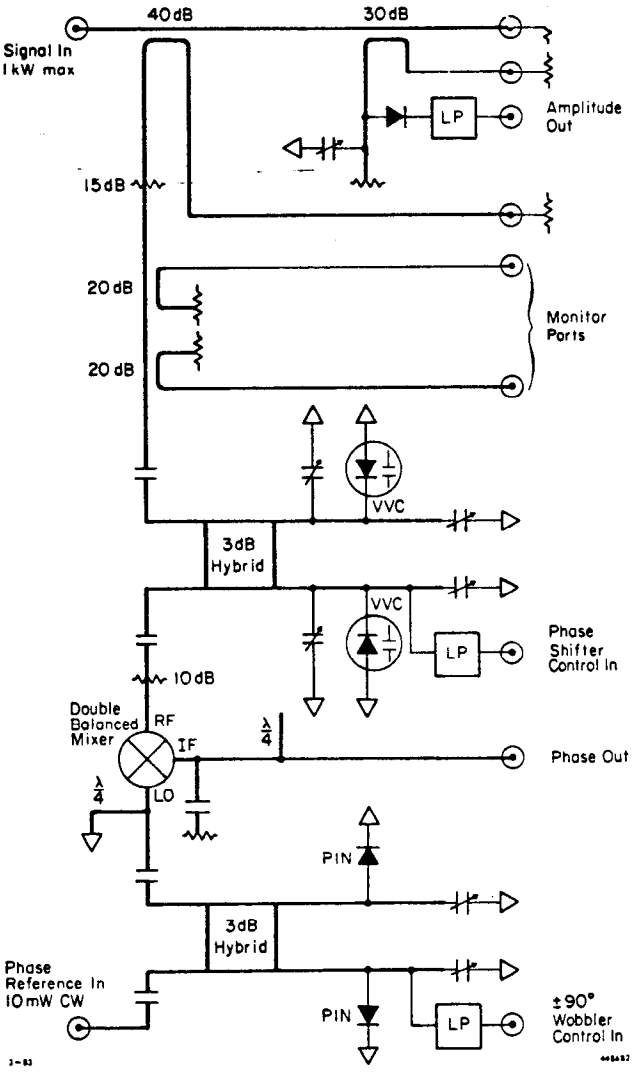

Fig. 2. RF head circuit diagram.

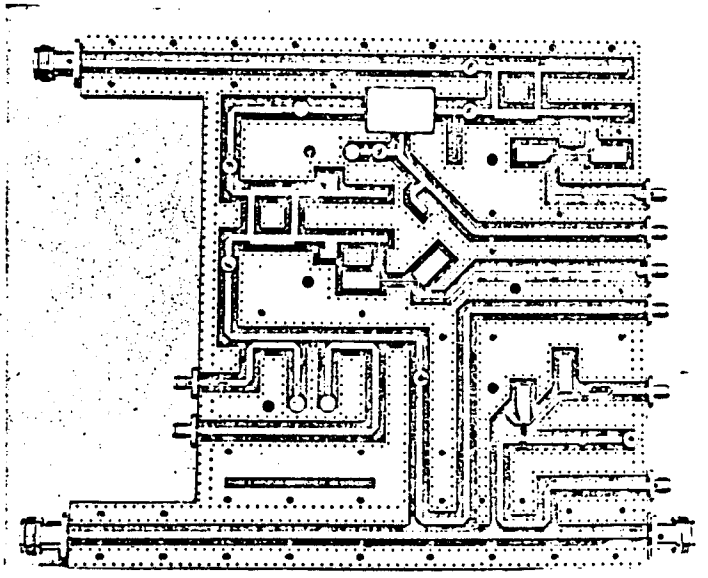

Fig. 3. RF head stripline circuit board

†Watkins & Johnson: M63; Magnum Microwave Corp.: MC24M-3.

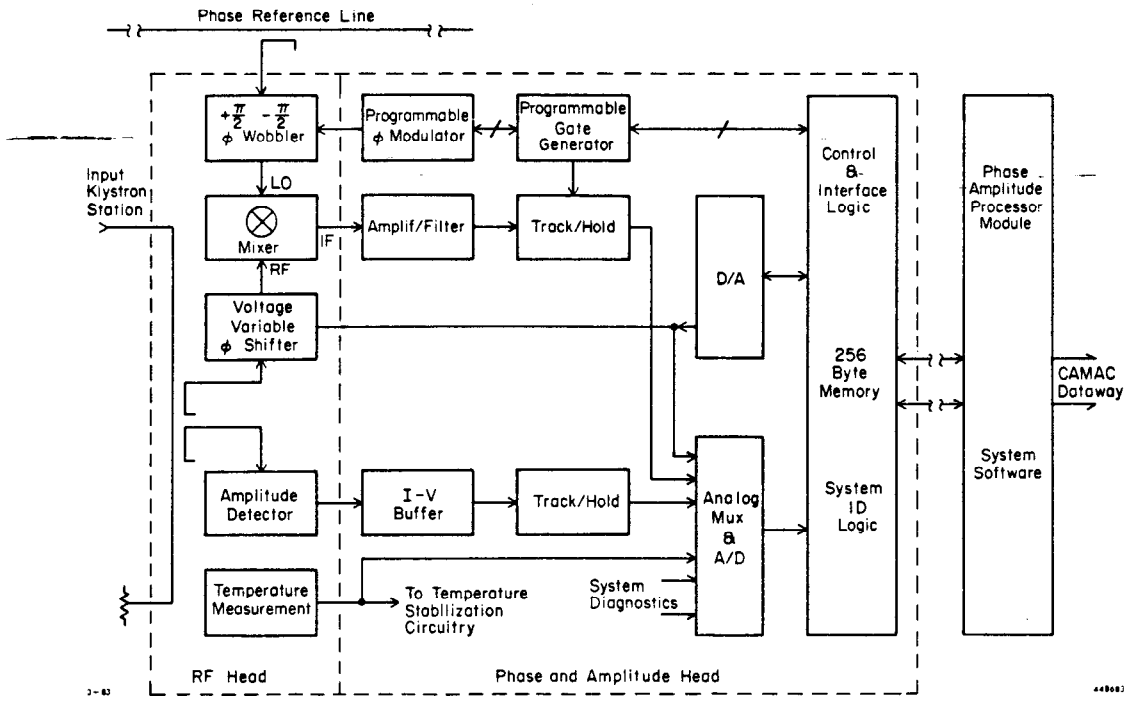

Fig. 4. Phase and amplitude detector system block diagram.

The control processor is an 8088 based microcomputer packaged as a CAMAC module, and is a SLAC standardized general purpose I/O controller.[5] The software in this processor specifies the operating modes of the RF head and the specific measurement technique, and this control software is an integral component of the phase and amplitude system.

Software Description

The system components for the amplitude and phase measurements can be operated in several distinct measurement modes. A distinction can be made between modes that measure the signal phase independently of signal amplitude, and those modes that use the amplitude information in the phase calculation. An additional distinction can be made regarding the system measurement bandwidth, as pulse-to-pulse jitter measurement is part of the SLC system specification.

Measurement of phase on a single pulse basis requires an adaptive algorithm that uses the past phase and amplitude measurements to predict the slowly varying mixer offset and system phase sensitivity. If we model the mixer response as

$$V_{mix} = \alpha|\vec{S}| \cos(\phi_s - \phi_r \pm \pi/2) + V_{offset}$$

[where α = a gain coefficient, $|\vec{S}|$ = the magnitude of a signal voltage, V_{offset} = the mixer dc offset, and $(\phi_s - \phi_r \pm \pi/2)$ = the phase difference between the signal and the phase modulated reference] and model the amplitude detector response as

$$V_{amp} = \beta|\vec{S}| \quad ,$$

we can measure instantaneous phase and amplitude by use of the following algorithm.

Step 1—Adjust system to linear range by nulling the phase detector, i.e.,

$$|V_{mix}|_{+\pi/2} - |V_{mix}|_{-\pi/2} = 0 \quad .$$

We calculate

$$V_{offset} = \tfrac{1}{2}\left(|V_{mix}|_{+\pi/2} + |V_{mix}|_{-\pi/2}\right) \quad .$$

Step 2—Calculate the phase sensitivity of the system by adjusting the phase shifter an increment $\delta\phi$. Then

$$\Delta V_{mix} = V_{mix}(\phi_r) - V_{mix}(\phi_r + \delta\phi) \quad ,$$

$\alpha|\vec{S}|$ is found for small $\delta\phi$ as

$$\alpha|\vec{S}| = \frac{\Delta V_{mix}}{\delta\phi}$$

and using the amplitude detector

$$\frac{\alpha}{\beta} = \frac{\Delta V_{mix}}{\delta\phi V_{amp}} \quad .$$

By calculating this ratio, the system can now measure an instantaneous pulse-to-pulse phase measurement.

Step 3—Each pulse calculate ϕ_s, for $\phi_s - \phi_r < 10^o$ the cosine may be linearized, and

$$\phi_s = \pm\frac{\beta}{\alpha} \times \frac{V_{max} - V_{offset}}{V_{amp}} + \phi_r$$

where $\pm = \mp\,\pi/2$ modulation.

Step 4—Each pulse an instantaneous jitter can be calculated from the calculated ϕ_s,

$$\text{JITTER} = |\phi_s - \langle\phi_s\rangle_n|$$

where $\langle\phi_s\rangle_n$ is the average value of the last n in tolerance readings. The control processor performs steps 3 and 4 for each klystron pulse, and performs steps 1 and 2 at a slower rate, calculating slowly varying average values for the quantities α, β, and V_{offset}.

System Performance

The prototype detector head has been fabricated, and the prototype system software developed. As of this writing the prototype system measures in the laboratory 1 μs 2856 MHz pulses at a 180 Hz repetition rate with $<.1^o$ of phase resolution, with an average measurement jitter of approximately .05%. The amplitude jitter measurement sensitivity under the same conditions is found to be approximately .05%. Field testing of this prototype is underway, and it is hoped that the real-world performance will be reported at the March 1983 Accelerator Conference.

Acknowledgments

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