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STATUS OF THE SLAC SNOOP DIAGNOSTIC MODULE FOR FASTBUS*

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Abstract

A SNOOP Diagnostic Module for FASTBUS is under development at SLAC. The SNOOP Module resides on a FASTBUS crate segment and provides diagnostic monitoring and testing capability. It consists of a high-speed ECL front-end to monitor and single-step segment operations, a simple master interface, and a control processor with two serial communication ports. Module features and specifications are summarized, and prototype hardware is shown.

I. Introduction

Data acquisition and control systems based on the proposed FASTBUS Specifications [1,2] are designed to permit monitoring and control for diagnostic purposes by means of a SNOOP Module which can observe and delay bus operations. The SNOOP Module has access to all signals involved in operations, since they are bussed to all module positions. Thus a history can be kept of all operations on a segment, no matter what the locations of the master and slave modules may be relative to the SNOOP Module.

The SNOOP Module can delay operations by asserting the Wait signal. This inhibits transitions of all handshake timing lines so that all bus signals involved in the current bus cycle remain static until Wait is removed. The system can thus be single-stepped by asserting Wait. Similarly, comparison logic in a SNOOP Module can be used to detect a particular address or data transfer, and then assert Wait to halt the segment.

The serial bus lines in each crate segment may be used as an independent communication path between diagnostic modules and system host computers, when connected to a serial network which bypasses segment interconnect units.

A prototype SNOOP Module has been developed with programmable Wait generation logic, address and data traps, a history silo memory and interface logic for master and slave operations. These functions are implemented with high-speed 100 K ECL parts to optimize response capability. Control and supervision of the fast front-end section are handled by a compact microprocessor section based on a powerful 16-bit CPU (MC 68000). The processor section includes interface ports to the FASTBUS serial diagnostic network, and to a general-purpose, UART-type serial connection for a terminal which provides floppy disk storage for diagnostic programs and data.

The design for this module and supporting software have been described in previous papers[3,4,5] and are summarized in Fig. 1 and Tab. 1.

Table I. Features and Basic Specifications

- Fast front-end implemented with 100 K ECL devices in 24-pin flatpaks.
- Programmable wait-step logic with 5 ns response time.
- Address and address-data combination traps with 8 ns response time.
- Parity-error trap with 15 ns response time.
- Activity history silo with 56-bit × 256-word RAM; 100 MHz recording speed; programmable recording modes; FB or real-time synchronized; logic analyzer mode with internal or external clock source.
- Simple master and slave capabilities with geographical address recognition, bus arbitration, IO register programmed protocol control, and software emulation of CSR registers.
- MC 68000 CPU (12 MHz).
- 25 level programmable priority interrupt structure (Z8530A and Z8536A peripherals).
- 48 K-word × 16-bit memory with variable configuration of RAM/ROM sizes.
- 24 K-word × 16-bit maximum size static RAM (100 ns access and cycle time).

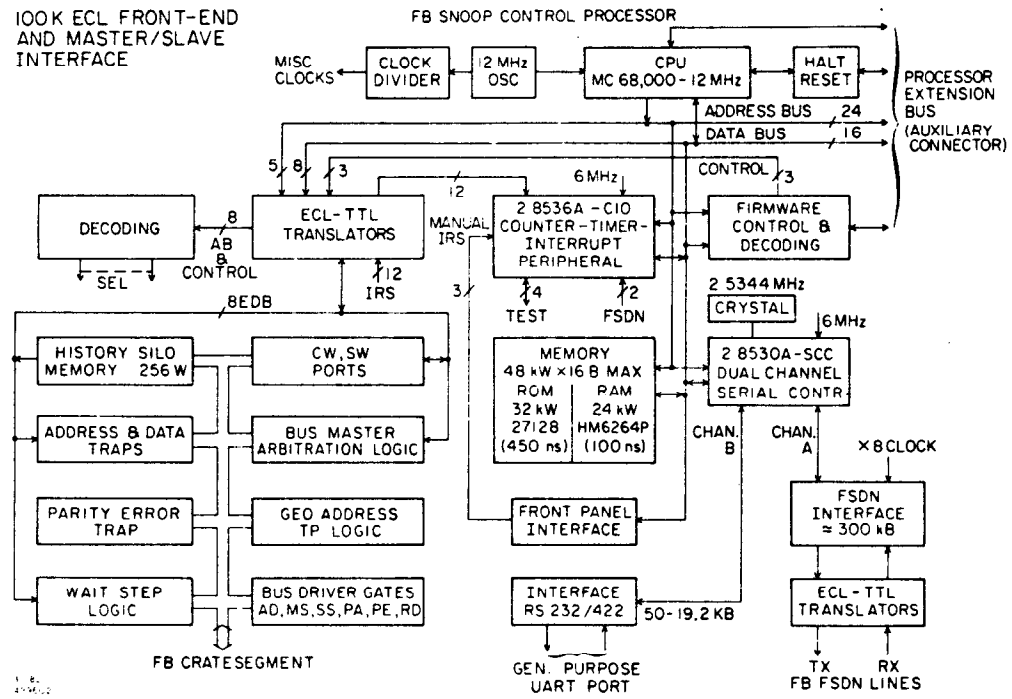

Fig. 1. SNOOP Module Block Diagram

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- 32 K-word × 16-bit maximum size EPROM (250 ns).
- 3-channel counter-timer with programmable inputs and modes (Z8536A).
- Dual channel serial Communication Controller peripheral (Z8530A) with baud rate generators.
- RS232/422 asynchronous serial port with selectable baud rate (50 to 19.2 K baud).
- Synchronous serial interface for FSDN port (300 K baud).
- Processor driven front panel with status display, manual WAIT execution switch, interrupt sense switch for processor selftest, CPU reset switch; NIM level test outputs from wait-step logic, and external clock input for silo memory recording.
- One unit wide FB module type A with 210 IC packages on a six-layer PC board; estimated 85 watt power dissipation.

II. Prototype Development and Testing

A. Control Processor Section

A wirewrap prototype of the control processor section with 35 IC packages is shown in Fig. 2. The 68000 CPU is located on the left side of the board. The memory with 64 K bytes of EPROM and 32 K bytes of static RAM is seen next to the CPU. The center part of the board contains firmware control and decoding logic. Next, to the right we have the counter-timer-interrupt circuit, the two serial interface ports, and front panel interface hardware. The two flat cable connectors provide the link to the SNOOP ECL section prototype board. The processor section was implemented on a separate board in wirewrap to allow convenient checkout and testing independent from the ECL section.

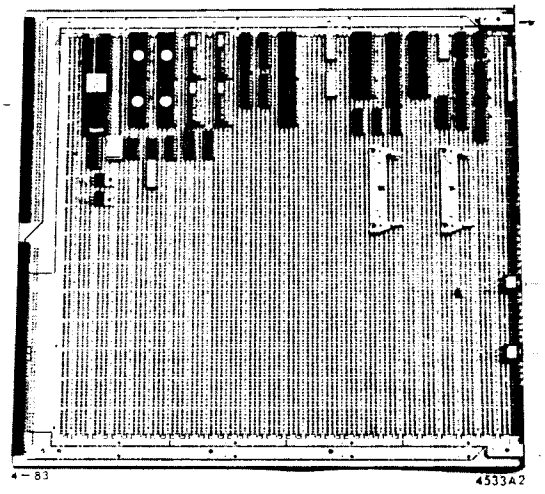

Fig. 2. Control Processor Section Prototype Board

B. ECL Section Prototype

A prototype printed circuit board of the SNOOP ECL section is shown in Fig. 3. The six-layer PC board contains the high-speed emitter-coupled logic with 84 flatpack IC's and ECL RAMs, 90 DIP IC packages, 100 Ω SIP terminating resistor packages, and miscellaneous discrete devices. The top area of the board with several temporary DIP patterns and two cable connectors will accommodate the processor section in the future. The PC board dimensions are 400 × 366.7 mm (15.748 × 14.437 in). The power dissipation is 74 watts. The printed circuit artwork is based on a pencil layout design drawn at 4:1 scale. The pencil layout was then digitized and computer plotted to generate the photo artwork. The flatpack IC's with 50 mil lead spacing use 20 mil-wide surface pads for mounting. This requires traces of 10 mil width with 10 mil clearance for routing between pads. A scale of 4:1 is mandatory. The layout had to be processed in several parts. The data was then merged for the final 1:1 photo plots Manual verification of checkout plots for six layers with each layer split into two plots was extremely difficult and time consuming Also the flatpack IC's with surface pads for mounting require a substantially different layout technique as compared to the customary dual-inline hardware with feed holes for each IC connection, if circuit density is to be maintained. Finally the special requirements of high-speed ECL logic on interconnection design and line termination had to be taken into account. The utilization of the six metal layers of the PC board is as follows, starting on the component side: 1) primary signal layer; 2) ±5 V power plane (the control processor area utilizes +5 V on this layer); 3) inner signal layer and ground plane; 4) primary ground plane; 5) -2 V power plane; and 6) primary signal layer (solder side).

Three prototype PC boards were commercially fabricated. Board loading was done inhouse. Flatpack lead forming and cutting was done with a simple jig; flatpacks were manually soldered. These loading steps for flatpacks were found to be inadequate. A proper lead forming and trimming tool will be required and reflow-soldering will have to be used for future board production.

The ECL section photo in Fig. 3 shows the FASTBUS interface on the left side. This includes comparator circuits for address and data traps. Next we see the parity checkers and the history silo memory. The block of DIP ICs in the center contains the address and data trap registers. The balance of hardware represents wait-step logic, control, decoding and processor section interface.

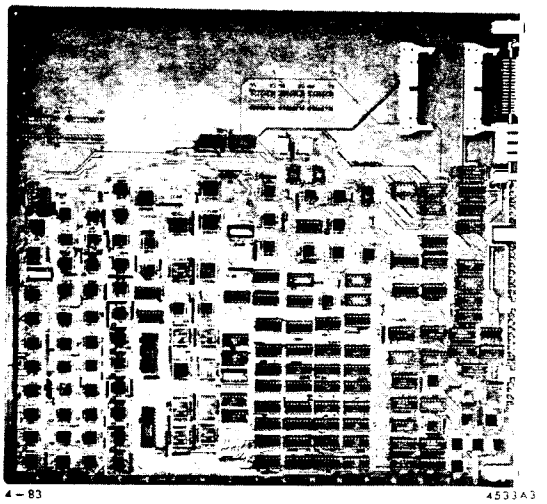

Fig. 3. ECL Section Prototype Board

C. Processor and Serial Network Testing

Three wirewrap prototype modules of the first SNOOP processor design[3] are used for software and serial network development[4] (Fig. 4). A Zenith Z89 smart terminal with disk drive and attached printer is connected to one SNOOP processor module via the RS232 terminal port. All three processor modules are linked by the FASTBUS Serial Diagnostic Network (FSDN). The SNOOP FORTH operating system has been installed on these 68000 processor modules. Low-speed network tests similar to earlier ones with a Z80 prototype system have been repeated, and the system hardware appears to be fully operational. Full-speed tests await integration of the serial network into the operating system

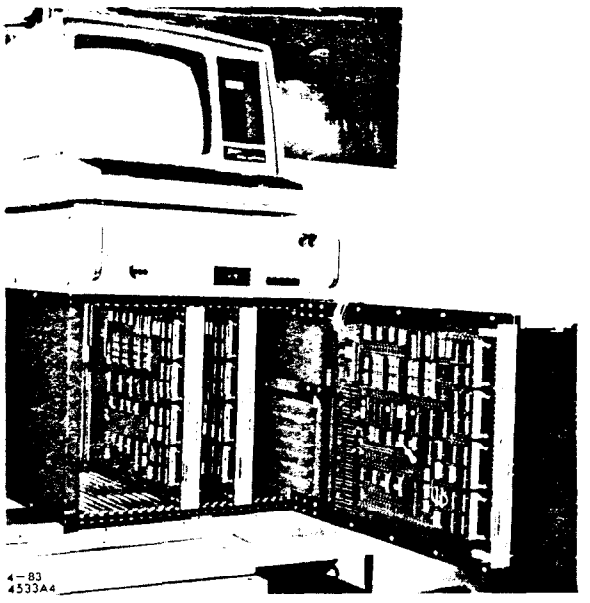

Fig. 4. Processor and Serial Network Development.

structure, as the true speed limits will be determined by the level of interference with other system functions during network message handling. This integration is nearly completed, and one Z89 terminal has now successfully controlled several SNOOP Modules through the network connection. One of these original processor modules has also been fitted with connectors for cables to the SNOOP ECL section prototype and to the SLAC IORFI FASTBUS interface module.[6] This allows one CPU to generate signals on the FASTBUS segment and also to observe their effects in the SNOOP front end, and vice versa, which simplifies the ECL hardware checkout and testing. The entire IORFI Support Software,[7] which was written in FORTH for an LSI-11 system, was easily moved to the 68000 FORTH system, and has been used extensively for the SNOOP ECL section testing. Once the checkout of the new control processor section (Sect. A., above) has been completed, the operating system will be moved to this processor with necessary changes to accommodate the new Zilog SCC and CIO peripheral chips, and to take full advantage of the larger and faster memory and faster 68000 CPU (12 MHz).

D. ECL Section Prototype Testing

Checkout and testing of the ECL section board is being pursued at three levels:

- a basic static bench checkout at the level of individual ICs;
- static subsystem testing with simulator boxes;
- dynamic computer testing in a FASTBUS crate.

Due to the high-speed ECL logic the first prototype implementation of the SNOOP design had to be a PC board. It was decided to load and bench check the board one IC package at a time. This procedure helped to pinpoint PC board interconnect faults and shorts, defective integrated circuits, and logic design problems. Inner layer faults were successfully repaired by means of high current pulse discharges or precise drilling.

The next level of checkout utilizes a FASTBUS manual testbox[8] to simulate a segment and master and slave responses. Also a simple simulator box replaces the SNOOP processor and provides control and display of the processor data, address, and control lines from and to the ECL section. These tests perform a slow, manual checkout of complete subsystems such as the address trap, by means of a limited sample of test conditions.

Finally, computer tests are being used for dynamic and exhaustive checkout. A SNOOP processor module linked to an IORFI interface module and the ECL section board by special cables resides in a FASTBUS crate (see Fig. 4 and Sect. C, above). Program loading and control is done from the Z89 terminal. A memory module[8] is also used as a slave in the crate.

The ECL section PC board has been fully loaded and bench checked. We have also successfully completed simulator box and computer tests of the processor interface and decoding hardware, the programmable wait-step logic, and the address and data traps. Checkout and testing of the history silo memory is in progress at present.

III. Conclusion

Testing of the SLAC FASTBUS SNOOP prototype system is expected to continue for the next several months. Based on the experience and results gained from this development program, it is planned to produce an updated PC board layout including the 68000 processor section.

Acknowledgments

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