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A New ATLAS Muon CSC Readout System with System on Chip Technology on ATCA Platform

R. Claus, on behalf of the ATLAS Muon Collaboration[a,1,*]

[a]SLAC National Accelerator Laboratory, 2575 Sand Hill Rd, Menlo Park, CA 94025

Abstract

The ATLAS muon Cathode Strip Chamber (CSC) back-end readout system has been upgraded during the LHC 2013-2015 shutdown to be able to handle the higher Level-1 trigger rate of 100 kHz and the higher occupancy at Run 2 luminosity. The readout design is based on the Reconfiguration Cluster Element (RCE) concept for high bandwidth generic DAQ implemented on the ATCA platform. The RCE design is based on the new System on Chip Xilinx Zynq series with a processor-centric architecture with ARM processor embedded in FPGA fabric and high speed I/O resources together with auxiliary memories to form a versatile DAQ building block that can host applications tapping into both software and firmware resources. The Cluster on Board (COB) ATCA carrier hosts RCE mezzanines and an embedded Fulcrum network switch to form an online DAQ processing cluster. More compact firmware solutions on the Zynq for G-link, S-link and TTC allowed the full system of 320 G-links from the 32 chambers to be processed by 6 COBs in one ATCA shelf through software waveform feature extraction to output 32 S-links. The full system was installed in Sept. 2014. We will present the RCE/COB design concept, the firmware and software processing architecture, and the experience from the intense commissioning towards LHC Run 2.

Keywords: ATLAS, Cathode Strip Chamber, Data Acquisition, DAQ

1. ATLAS Cathode Strip Chambers (CSC)

The ATLAS [1] Cathode Strip Chambers are composed of multiwire proportional chambers designed to detect muons in the high pseudorapidity region of $2.0 < |\eta| < 2.7$. The detector consists of two end-caps with 16 chambers each. There are two variants of the chambers to provide seamless coverage. Each chamber has 4 precision (η) and 4 transverse (φ) layers. There are 768 η and 192 φ strips per chamber. η strips have a pitch of 5.31 and 5.56 mm on the two chamber variants, respectively.

The Front-End-Electronics consists of 4 η and 1 φ readout boards per chamber, each with 192 channels per board. Preamplifiers and shapers convert strip signals to bipolar waveforms with 70 ns shaping time. Pulses are sampled every 50 ns and stored on 144 cell Switched Capacitor Array (SCA) analog memories. Samples tagged for reading are digitized (12 bits) and transferred to off-detector ReadOut Drivers (RODs) over high speed fiber-optic G-Links.

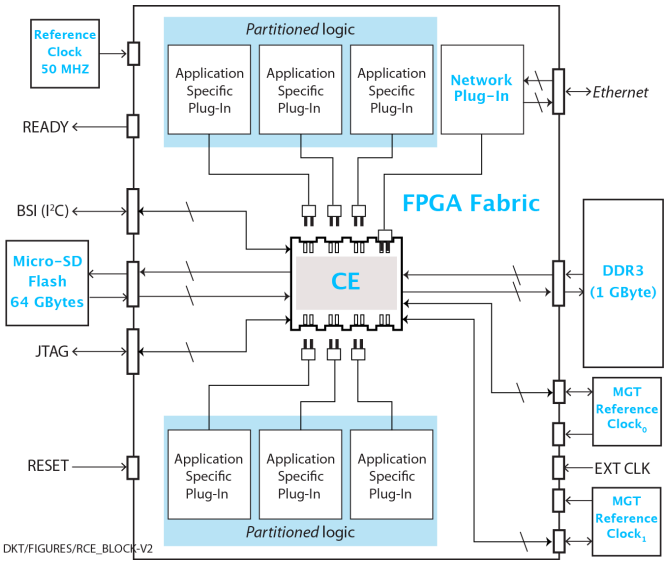

Figure 1: Block diagram of the RCE

2. ATCA-Based Generic Data Acquisition System

A modular data acquisition architecture has been developed at SLAC: the Reconfigurable Cluster Element (RCE) (fig. 1). It is based on Zynq-7000 System-On-Chip (SoC) technology from Xilinx, which provides processing components that include both firmware and software. The Zynq has a large FPGA fabric and a dual core ARM Cortex-A9 processor. A plug-in architecture (fig. 2) is defined for performing on or off-chip input/output. Operating system choices are RTEMS and LINUX.

The host platform is the Advanced Telecommunications Computing Architecture (ATCA) PICMG 3.0 standard. An ATCA carrier board called Cluster-On-Board (COB) was developed to hold 8 + 1 RCEs. The COB has a Cluster Interconnect (CI) consisting of an on-board low latency 10-Gigabit

*Corresponding author
Email address: claus@SLAC.Stanford.edu (R. Claus, on behalf of the ATLAS Muon Collaboration)

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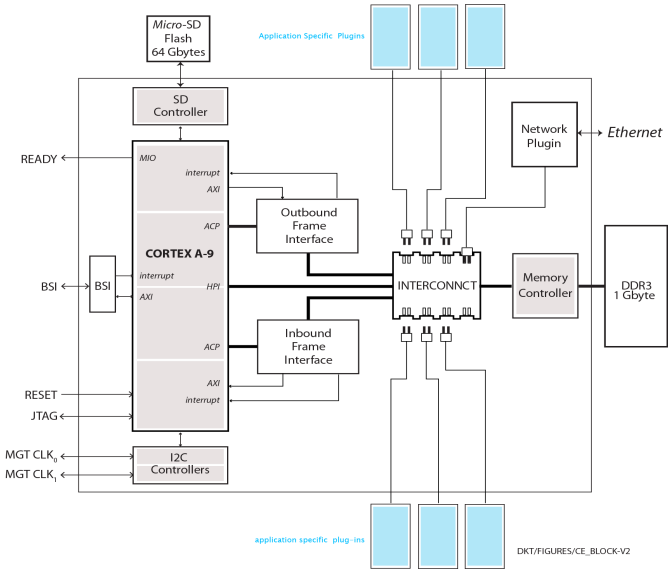

Figure 2: The structure of the Cluster Element

Ethernet switch (Fulcrum FM4224) that provides connectivity between RCEs, the backplane, and the front panel. A Pigeon Point Systems-based Integrated Platform Management (IPM) controller is embedded on the COBs to provide board-level management. A high density "zone 3" connector provides 96 channels of connectivity to a Rear Transition Module (RTM). A Rear Mezzanine Board (RMB) is defined for RTMs to provide Timing, Trigger and Control (TTC) I/O.

RCEs are implemented in two forms: the Data Transfer Module (DTM), which has an RCE that is shared with the application, and the Data Processing Module (DPM), containing 2 RCEs for the application's use. The DTM configures the CI and manages the fast timing signals from the RTM, which it can distribute to the DPMs. It is constructed using the smaller XC7Z030-2FBG484E Zynq chip as it has no access to the main data-flow traffic. Conversely, DPMs consist of XC7Z045-2FFG900E Zynqs to provide high speed links (16 MGTs) and FPGA processing resources for heavy duty processing.

3. Application of RCEs to CSC

A standard 6-slot ATCA shelf is used in the CSC system. Each slot contains a COB and an RTM. The COB hosts RCEs that provide Feature EXtraction (FEX) and data formatting capabilities, and the RTM provides the physical interface to the chambers and the central TDAQ system via MPO fibers.

The DTM RCE receives the TTC information from the LTP and distributes it to the DPMs. It also provides configuration and monitoring access to TTC and Busy functions.

Each DPM RCE supports a single chamber. These RCEs typically process 4 time samples of raw Front-End ADC data from all channels for each event. The ~5.8 kBytes of input raw waveform data per event is reduced by a factor of 20 or more by FEX cluster processing on each RCE. Data taking with more time samples is also supported. These clusters are, in turn, formatted into event fragments and sent downstream.

Several traditional hardware solutions are implemented in the firmware of the SoC, causing smaller footprint and lower power consumption. The TTC interface functionality resides in both DTM and DPM firmware. The front-end G-link, and back-end S-Link modules are implemented in firmware on the DPMs.

4. Integration with ATLAS TDAQ

A Control Processor is used to interact with the TDAQ infrastructure. This machine (and its redundant spare), is a standard COTS rack mountable PC running standard issue Scientific Linux as installed by the TDAQ sysadmins. It serves the interface for configuring all RCEs in parallel via Ethernet.

In order to recover the system during an ATLAS data taking session, the so-called "TTC Restart" procedure has been deployed. In a few minutes the system is reconfigured and the ATLAS trigger can be resumed. Finer grained diagnosis and recovery of issues appearing during runs is being prepared.

The shelf manager manages the shelf's housekeeping with input from the Detector Control System (DCS). An SNMP-based interface was developed to interact with the shelf's and COBs' IPM controllers.

5. Performance and Data Quality

The full CSC readout chain can run at 100 kHz with low dead time ($< 1\%$). This was achieved with high performance FEX code that works in conjunction with firmware support. Additional downstream bandwidth needed to cope with the expected Run 2 data volume was accommodated by doubling the number of S-links compared to Run 1. Tests done with simulated occupancy verified that the system has sufficient throughput.

Pedestal measurements performed with the new system are observed to be compatible with those collected during Run 1. Cosmic tracks were first seen in November 2014. The system operated smoothly during the first colliding beam pilot physics runs. Detector timing uniformity between chambers was observed to be within 10 ns. Offline analysis shows high muon track linking efficiency to other detectors.

6. Conclusion

The CSC is ready for the higher Level-1 trigger rate of 100 kHz and the higher occupancy at Run 2 luminosities. Initial operations with and without beams are very stable.

Acknowledgments

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References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 (2008) S08003.