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Flip Chip Assembly of Thin Substrates, Fine Bump Pitch, and Small Prototype Die

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Bump bond assembly of sensors and circuit chips is often a critical step for detector projects, and yet it can be expensive, time consuming, and carry high technical risk. In particular bump formation on singulated die, as obtained on multi-project wafer runs, is difficult due to the hydrodynamics of resist coating and handling of small parts. An increasing number of science applications need thin substrates for reasons such as increased speed of charge collection or reduction of mass to reduce multiple scattering, and there is always a demand for finer bump pitches. SLAC is involved in many challenging detector development efforts for particle physics, astrophysics, and the photon sciences and most of these require hybridization of small, prototype dies from multi-project wafer runs. Results on process development on bump deposition and bonding of thin substrates, small area chips, and chips with small bump-to-bump spacing will be described.

INTRODUCTION

Experiments conducted at the LINAC Coherent Light Source (LCLS) facility use different X-Ray detectors, most of which have hybrid integration. SLAC is developing new X-Ray camera chips and being able to prototype in-house is a key element for testing and qualification of the new chips.

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Successfully bump-bonded prototypes were used to perform preliminary tests on the new ePix family of Application-Specific Integrated Circuits (ASICs) as well as studies on small area sensor prototypes. Small area sensors have been studied to explore different guard ring designs and fabrication to evaluate radiation hardness.

These samples have 100 µm and 50 µm pitch and bump size of 20 µm in diameter.

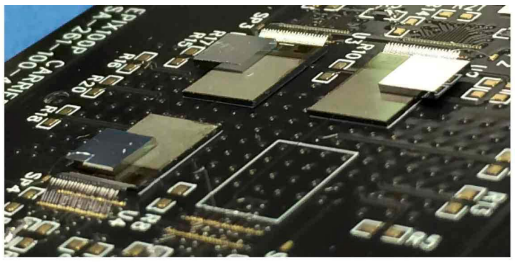

Figure 2: Samples of 96x96 array 50 µm pitch ASIC: small area 16x16 pixels sensor array 50µm pitch bump-bonded on ASIC used for radiation damages studies.

Camera prototypes chips of 5 mm x 5 mm and 20 mm x 20 mm in size have been bump-bonded. The smaller size chips have an array of 96x96 or 48x48 bumps depending on the pitch, while the bigger size have an array of 352x384. Multiple small sensors (96x96 pixel) have been placed on single ASIC (352x384).

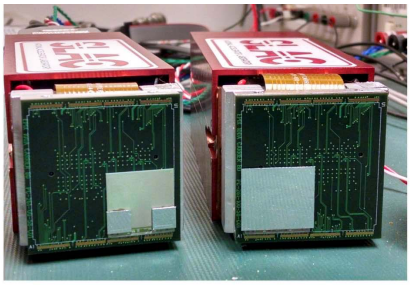

Figure 1: Fully integrated camera prototypes chips. On the center-left are two 96x96 sensors bump-bonded to a single 352x384 ASIC; on the center-right is a full 352x384 Sensor bump-bonded to matching ASIC.

In particular, for the prototype camera samples the Indium bumps are fabricated on single chips. Using single chip versus whole wafers causes the photolithography steps to be quite challenging and usually results in missing bumps around the edges of the ASIC chip. Improvements in the lithographic steps help to reduce this effect but not extinguish it.

The ASIC noise map below shows some of the missing bumps areas.

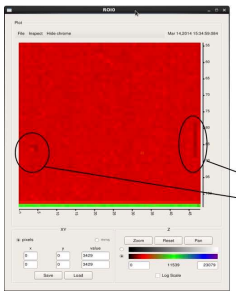

Figure 3: Noise map read-out of a 48x48 ASIC bump-bonded to a sensor, both of 5mmx5mm size chip.

Indium Bumps

The bumps for these camera prototypes and test structures on quartz and silicon substrates were fabricated at the Stanford Nanofabrication (SNF) Facility. These test devices have varying pitch (from 10µm to 50µm), and Indium bumps ranging from 4µm to 20µm in diameter. An Electron-Beam evaporator machine is used to deposit the under metal bump as well as the Indium films and by lift-off, approximately 4µm tall bumps are fabricated. This process has been mastered on both full size wafers and on more challenging single chips [1].

To explore and expand the capability on Indium bump-bonding, test structure arrays with different diameters and pitch of bumps has been designed and fabricated. Indium micro-bumps of 4 µm diameter with a pitch of 10 µm were resolved.

Figure 4: Picture of test structure partial (one chip) daisy-chains with 4µm diameter bumps at 10µm pitch taken with a Moticam Digital Microscope camera.

Below are few examples of bumps' characterization sizes and uniformity. Note that the ridge on top of the bumps is caused by the hole in the oxide layer being smaller diameter than the indium bump. In figure 5a) is such ridge is almost inexistence as the bumps diameter is so small that the difference is about 1µm or less.

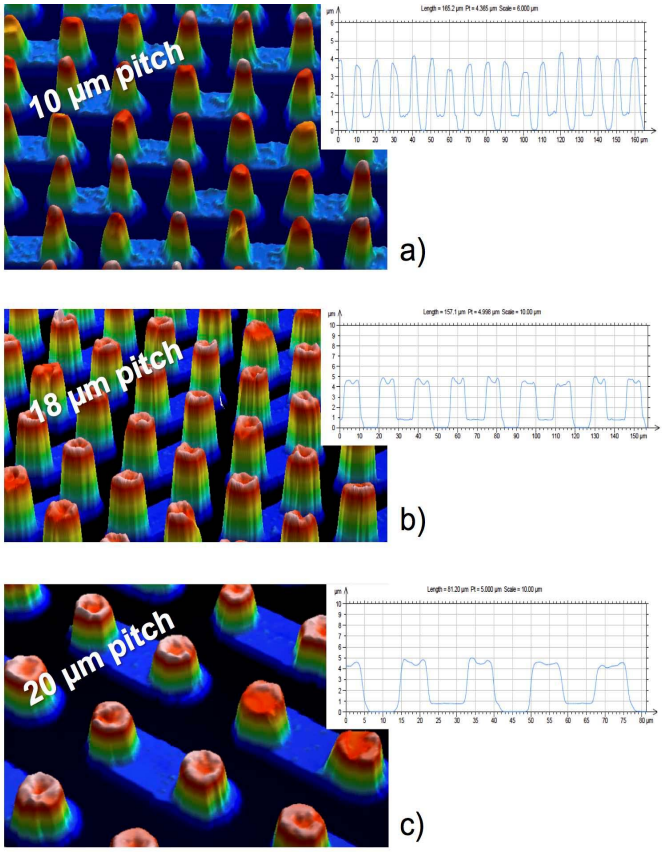

Figure 5: Images of test-structures In-bumps acquired with a "Coherence Correlation Interferometry" 3D profilometer:
a) 4 µm dia. 10 µm pitch; b) 7 µm dia. 18 µm pitch; c) 10 µm dia. 20 µm pitch.

SLAC's die placer bonder applies heat and compression to bond the chips [2]. For the Indium process, both substrates are heated to 170°C and the force (N) varies depending on the size of the chip, the bumps' size and the density of the array. For configurations studied in this paper the applied force ranges from 0.5 N up to 4 N.

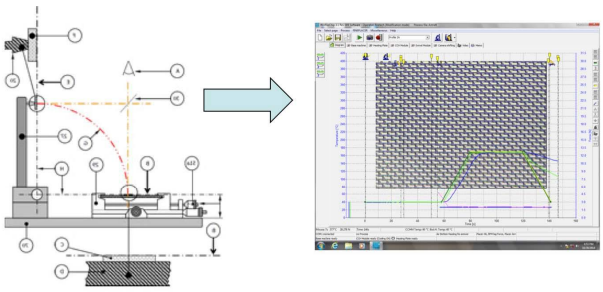

Figure 6: Schematic of the mechanics of the die placer and view of both chips though the beam-splitter or prism with process profile.

These test structures consist in dashed-daisy chains that once bump-bonded matched to crate a continuous ribbon. A schematic of the side view is shown below.

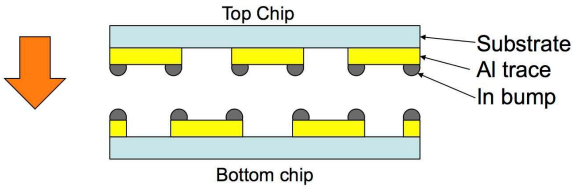

Figure 7: Cartoon of the daisy-chain's design of the test structure. The top chip chain is completed by the bottom chip chain once the bonding is performed creating a continuous Aluminum ribbon through the Indium bumps.

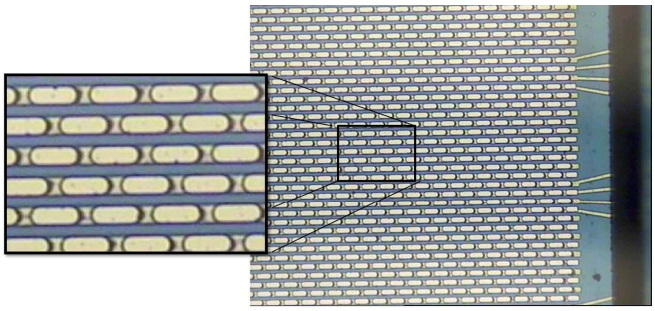

Fig 8: Alignment and bump of test structure (15µm pitch, 7µm OD) bumps. The top structure is on quartz while the ROC is on silicon chip.

The test structure arrays bumped and studied span from about 38,000 bumps to 122,500 bumps. Measurements of the resistance of the bump-chains in the smallest test structures give values in the low kilo-Ohms which gives a resistance per bonded-bump of about 1.8 Ohm.

The results are summarized in the following table where the yield for camera prototype chips and resistance for test structure chain-bumps are listed.

TABLE I. SUMMARY

# of Bumps	Pitch	Diameter	Bump-Yield	Bump Structure Ω
2,300	100	20	84%**	
135,168*	50	20	94%**	
9,200	50	20	81%**	
38,000	18	7		3.4 Ohm
54,500	15	7		2.9 Ohm
122,500	10	4		1.8 Ohm

* 2cmx2cm chip instead of 0.5cmx0.5cm.

** Values reflecting the edge effect due to single chip photo-lithography.

There are numerous applications that benefit from bump-bonding thin substrates. Below are preliminary flatness results of thin substrates after the bonding. In this example the chips are 100 µm thick silicon substrates with a pitch of 100 µm x 50 µm.

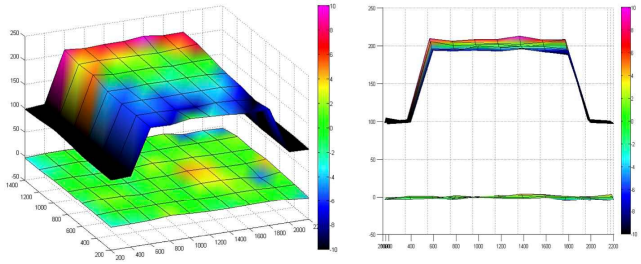

Figure 5: Graphs of the flatness map of thin chips after bond-bonding. The measurements in X, Y and Z are in µm. The top surface is the top bonded chip respect to the bottom chip. The surface resulted flat but with a tilt.

CONCLUSION

In conclusion, we showed SLAC's capability of in-house bump-bonding for Indium bumps. We plan to perform more tests for thin substrates and bumps features, and explore other substrates material and bumps metals.

ACKNOWLEDGMENT

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[1] M. Bigas, E. Cabruja, M. Lonzano, "Bonding techniques for hybrid active pixel sensor (HAPS)", 2007 Nucl. Inst. And Meth. In Phys. Research A 574 (2007) 392-400

[2] Finetech-Lambda Manual.