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eLine100: A Front End ASIC for LCLS Detectors in Low Noise Applications

A. Dragone*, P. Caragiulo, D. Freytag, P. Hart, R. Herbst, S. Herrmann, C. Kenney, J. Segal and G. Haller

***Abstract*– eLine100 is a fast-frame 96-channel readout ASIC for SLAC Linac Coherent Light Source (LCLS) detectors. The circuit has been designed to integrate the charge from high-capacitance 2D sensors with rolling shutter and 1D sensors. It has a noise floor of 55e^- + 8e^-/pF r.m.s at room temperature and it is suitable for applications requiring resolutions on the order of 100e^- r.m.s and signals up to 120 photons/pixel/pulse at 8keV (260ke^-). 2D sensors with a rolling shutter like the X-ray Charge Pump Sensor (XCPS), for which the ASIC has been optimized, present many pixels which are bussed on the same readout line. This characteristic, together with the fixed LCLS beam period, impose limitations on the time available for the read out of each pixel. Given the periodic structure of the LCLS beam, the ASIC developed for this application is a time-variant system, providing a two-stage low-noise charge integration, filtering, correlated double sampling and a processing speed of up to 250k pixel/s on each channel. To cope with the required input range, a charge pump scheme has been implemented using an asynchronous zero-balance measurement method. It provides on-chip 1-bit coarse analog-to-digital conversion of the integrated charge. The residual charge is sampled using correlated double sampling into an analog memory, multiplexed and measured with the required resolution by an external ADC. In this paper, the ASIC architecture and performances of the final release are presented.**

I. Introduction

The unique characteristics of X-Ray Free-Electron Laser (X-Ray FEL) sources, in terms of brilliance and narrow pulse duration, have increased the need for new large area detectors with fast readout capabilities and specifications that, depending on the experiment, can range from ultra-low noise requirements to extremely large full-scale and dynamic ranges. eLine100 (Fig. 1) is the latest addition to the new "eLine" class of multichannel time-variant integrating front-end Application Specific Integrated Circuits (ASIC) that SLAC has developed for the Linac Coherent Light Source (LCLS). The class is composed of two front-end ASICs, one designed for high-dynamic range applications (eLine10k [1]) and one designed for ultra-low noise applications (eLine100). The class also includes a switcher ASIC (sLine [2]) used to control the operation of column-parallel readout 2D sensors with rolling shutter such as the X-ray Charge Pump Sensor (XCPS), based on a concept by Pavel Rehak from Brookhaven National Laboratory [3] and under development at SLAC.

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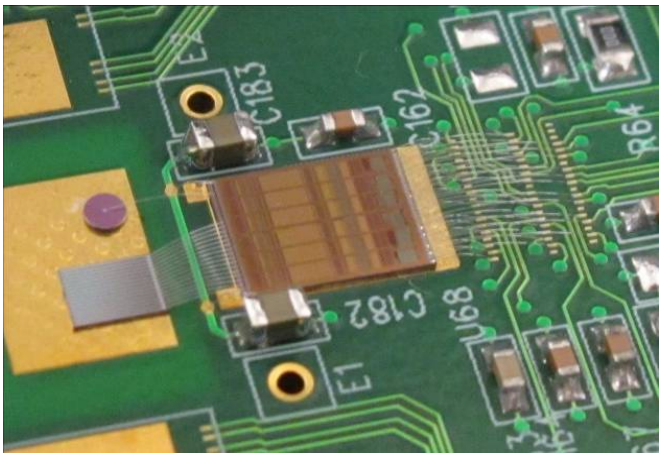

Fig. 1: eLine100 in a test system bonded to a strip detector (and a single diode).

In FEL applications, photons hit sensors simultaneously; therefore only integrating detectors can be used. eLine100 is designed to integrate charge from high-capacitance 1D sensors or 2D column-parallel readout sensors with rolling shutter. XCPS [3-4] is a pixel array detector with in-pixel charge gating capabilities (Fig. 2). The eLine100 ASIC was designed with a general purpose approach, optimized for XCPS.

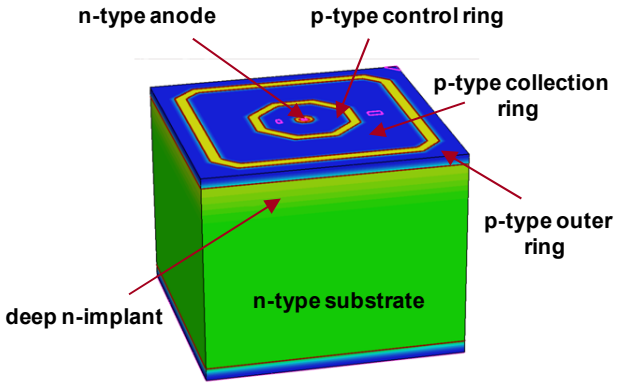

Fig. 2. XCPS pixel structure.

XCPS has a matrix architecture with pixels of 56x56µm^2 in which the charge is integrated and stored in a potential well controlled by varying the potentials on two diffused regions (control ring and collection ring). Pixels are isolated from each other by potential barriers (outer ring). The device is fully depleted by applying a high negative voltage to the junction on its entrance window. When a photon is absorbed, the generated carriers drift to the exit side of the device. The carriers are collected under the collection ring, where a potential well, isolated from the anode, is formed, controlled

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by the voltages applied to the control and collection rings (gating potentials). When the gating potentials are reversed, the charge is transferred to the anode. The integration and read out phases of pixels in the same row are controlled by a dedicated switcher ASIC (sLine [2]), which effectively implements the operation of a rolling shutter. Columns of the sensor are read out in parallel by the front-end ASIC. Accurate control of the gating potentials is important to completely transfer the charge from the well into a collecting electrode during the readout phase and to avoid injection back into the bulk of the pixel when returning to the integration phase. Such injection is the real origin of the kTC noise that would limit performance.

The detector is designed to satisfy stringent requirements in terms of spatial resolution, noise and timing of the X-ray Correlation Spectroscopy (XCS) instrument [5] at the Linac Coherent Light Source (LCLS); XCS is designed for the study of equilibrium and non-equilibrium dynamics in disordered or modulated materials. Typical requirements for this application are full-scale signals of 100 photons at 8keV and a readout noise much better than one photon. Specifically, an equivalent noise charge (ENC) better than 100e^- r.m.s is needed. The required large detector area results in a large capacitive load (2pF) at the front-end, making it hard to reach the required noise levels. The large channel count imposes limitations on the time available for the read out. XCPS detectors of up to 384 x 256 pixels are in fabrication for this instrument.

In this paper we report on the architecture and performance of the final release of the ASIC. eLine100 provides low-noise charge integration [10], real time adaptive time-variant filtering [7-9] and correlated double-sampling. As with all ASICs in the eLine class, a charge pump scheme is used, implementing a zero-balance measurement method [5] to satisfy the requirements for large full-scale signals. It provides an on-chip coarse analog to digital conversion allowing a measurement of the residuals with the required resolution. The residuals conversion is performed with external 14-bit ADCs. The actual version of the ASIC has 96 channels, a size of 6.8×5mm^2 and was fabricated in TSMC CMOS 0.25µm technology. After a description of the detector systems for which the eLine class is designed, the ASIC architecture will be discussed in section III. The charge pump approach will be described in section IV. The ASIC characterization and some experimental results are reported in sections V and VI.

II. Column-Parallel Readout Detector Systems

During the first year of operation at LCLS, the need for several new large area detectors arranged in different form factors and shapes, and covering a wide spectrum of experiments has been apparent. Modular, scalable designs are a must. To simplify integration and reduce development time, detectors have been designed around common platforms so that dedicated sensing heads could be incorporated in a common detector system. eLine is the first example of a class of ASICs for LCLS sharing a common back-end section and interface to the rest of the system. The class is designed for the readout of column-parallel readout sensors, although it can also be used for the readout of 1D strip sensors. A typical block diagram of these kinds of systems is shown in Fig. 3. Pixels in the sensor are arranged in a matrix fashion. The collecting nodes of the pixels are isolated by means of a "switch". Sometimes, like in XCPS, the collecting nodes are isolated from the collection area by means of controllable potential barriers. In other cases, the switch could be a FET (XAMPS [1, 6]). The "switches" associated to the pixels in a column are connected to the same readout line, while the gates (named transfer gates) of those associated with the pixels in a row are activated simultaneously. Columns of the sensor are read out in parallel by the front-end ASIC. This architecture allows a parallel readout of all the pixels in the same row. The full frame can be read out by cycling through the rows. Each column of the sensor is read out by a dedicated electronic channel.

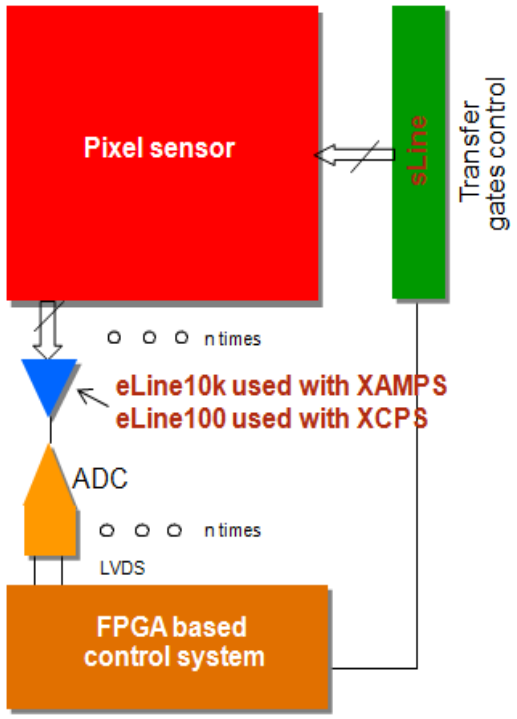

Fig. 3. Column-parallel read out system based on eLine.

External commercial ADCs are used to convert the output analog signals. The acquisition is controlled by an FPGA that maintains the synchronization between the LCLS beam and the selection of the rows to be read out. Typical array sizes (frame sizes) for XPCS are in the range of 384x256 pixels. Given the repetition rate of the LCLS beam (120Hz), a frame has to be read out in 8ms which, because of the parallel row readout, turns into a readout time slot of not more than 32µs per row (i.e., per pixel) on a specific readout channel. Multiple frame readout per pulse is desirable to perform more sophisticated corrections (acquisition of intermediate dark frames), but imposes additional timing constrains. eLine100 can process signals at a maximum rate of 250k pixel/s on each channel (i.e., 1kHz for 256x256 pixel frames).

III. ASIC ARCHITECTURE

A simplified block diagram of the ASIC architecture is presented in Fig. 4. The 96 channels of the ASIC are arranged in 6 groups of 16; each one connected to its own analog and digital multiplexers and dedicated outputs. The 6 blocks are read in parallel to speed up the read out phase. The acquisition is controlled by a single periodic signal (slot control, SC), whose period defines the readout time-slot per row. This signal is synchronized to the LCLS beam trigger. During the active part of the SC period the charge is read out from the pixels and sampled. During the inactive period stored data are read out and the system is reset.

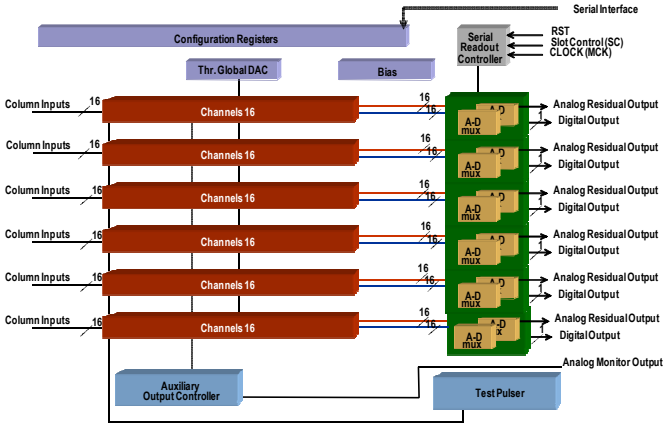

Fig. 4: Simplified block diagram of the 96-channel ASIC.

Each channel (Fig. 5) is composed of a front-end section with a two stage low noise charge integrator, a pulsed reset, a second-order non-inverting programmable LP filter, and a discriminating charge pump circuit. The back-end section of the channel is common to all the readout ASICs in the eLine class and is composed of two correlated double-samplers (CDS) and the multiplexers.

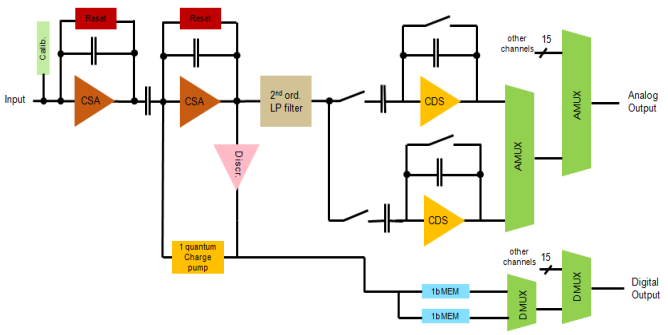

Fig. 5: Simplified schematic of a single channel.

The low noise preamplifier integrates the input charge and has an equivalent gain of 60mV/fC. The gain is split in two stages. To achieve such gain in a single stage, a feedback capacitor smaller than the minimum allowed by the technology would be required. Furthermore, it is convenient to split the gain in two stages to minimize the noise contribution due to the charge pump circuit. The low noise amplifiers (both stages) are implemented in a straight cascode configuration with gain boosting. To minimize the impact of the flicker noise, the input device is a PMOS (W= 0.75mm, L=0.36µm). The size of the input transistor is optimized for a 2pF input capacitance and for noise levels within the 100e^- r.m.s. required by the application.

To reset both stages of the preamplifier, the pulsed reset system also has two stages. To accommodate the collection of electrons, the first stage is actually a precharger that resets the output node of the first amplification stage close to the lower rail (about 0.5V).

To increase the output dynamic range and to minimize non-linearity effects in the preamplifier response, an output stage using zero-threshold MOSFETs has been implemented in both amplifiers. The second-order LP filter is designed according to a Sallen-Key non-inverting topology and makes use of a rail-to-rail differential amplifier with constant trans-conductance.

The filter has two coincident real poles with programmable time constant. Since the application requires the readout of a pixel within a given time slot, the time constant value has to be set in a way so that the response of the filter reaches a flat top in half of the time slot. Eight values of the time constant are implemented resulting in readout timing slots from 4µs to 32µs in 4µs steps.

The two CDS stages are used to sample and store the filter output, purged from the fluctuations introduced by kTC noise, and baseline fluctuations [9]. They also reduce low frequency noise. The two CDS stages work in an alternating way to allow simultaneous read-write of the same channel. While one sampler holds the previous event and presents it to the active one of two analog multiplexers for readout, the other sampler is ready to process the next event. In such a way, when a row of the sensor is processed the results from the previous one are read out with no dead time. This architecture allows the implementation of a "quasi-trapezoidal" noise weighting function [7-9]. Simulations and measurements of the noise weighting function for the eLine class of front-end ASIC are reported in [1, 6].

To satisfy the large required input dynamic range of 100 photons at 8keV (about 35fC of charge) a charge pump system, described in the next section, is included in the channel.

Channels are multiplexed in groups of 16 to the same output; 6 analog multiplexer with an output buffer are integrated. An automatic calibration system featuring an internal pulse generator is implemented combining a 10-bit DAC for the injection of calibration signals, and a 10-bit counter. Another 10-bit DAC is used for the global charge pump threshold setting in each channel. The logic for the acquisition, readout, and configuration is also common to all channels.

By making use of some innovative analog circuit solutions, the ASIC presents a noise floor of 55e^- + 8e^-/pF r.m.s at room temperature. It has a total dissipated power of about 3.5mW per channel and it is suitable for applications requiring resolutions on the order of 100e^- r.m.s and signals up to 120 photons at 8keV.

IV. The Charge Pump Approach

To cope with the large input dynamic range, a zero-balance measurement method has been implemented in the eLine class. This concept is widely exploited in the high dynamic range eLine10k ASIC [1, 6], but it has been useful to extend the full-scale range of eLine100 above the value required by the applications without compromising the front-end gain and noise performance. An asynchronous simplified version of the circuit implemented in eLine10k is also present in this design. The feedback capacitor of the second stage preamplifier (Fig. 5) is sized to hold ½ of the full input signal range without saturating the preamplifier. For input signals within ½ of the full scale (42fC) the charge pump system remains inactive. For larger signals, a charge equal to ½ full-scale is subtracted from the input node of the second amplifier until a residual smaller than ½ full-scale signal is stored in the second stage feedback capacitor. According to the scheme described in [1, 6] as soon as the second amplifier approaches saturation, a threshold discriminator (lower limit of the range) asynchronously activates a pump circuit composed of a single capacitor connected to the input node on one side and, by means of switches, to two external reference voltages (analog ground and a dedicated 2.5V supply Vdd pump) on the other side. At this point, the residue stored in the feedback capacitor is converted through the chain described in the previous section. The firing of the comparator is also stored in a DFF cell whose content is thus equivalent to an on-chip 1-bit analog to digital conversion and represents the MSB of the digitized amplitude. The digital information is read out together with the residue, which is digitized with an external 14-bit ADC.

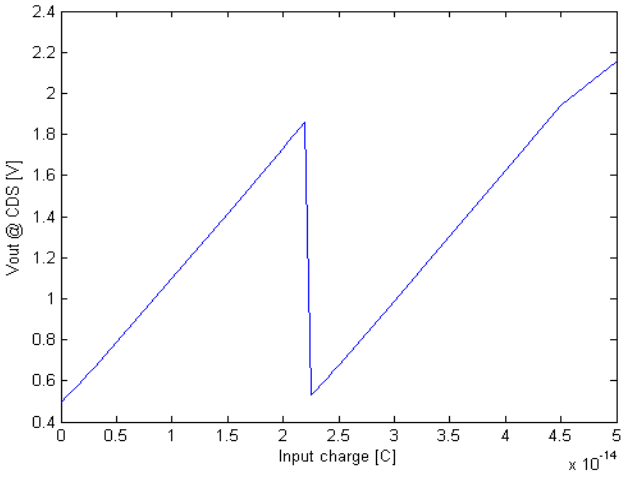

Fig. 6: Simulated analog residue response of eLine 100 at the filter output.

The external reference voltage (Vdd pump) can be adjusted allowing the tuning of the size of the pumped charge (and thus adjusting the upper limit of the range). Because of the gain in the first stage of the preamplifier, the kTC noise contribution of such a reference is estimated to be up to 4e$^-$ r.m.s. using standard external voltage regulators, thus it is negligible with respect to the required noise levels.

Because of the charge pump operation the circuit has a piecewise linear response as depicted in Fig. 6.

When the input charge increases, the output of the amplifier moves away from the baseline until it reaches the comparator threshold (pump threshold). At the first pump step the output of the amplifier moves back toward the baseline by a voltage step (pump height) that depends on the ratio between the pump capacitor and the feedback capacitor, and on the adjustable pump voltage (Vdd pump). Each pump step has an identical slope since the circuit configuration does not change. Calibration thus only requires the measurement of the voltage step associated to the pump step.

V. Measured Performance

eLine100 has been fabricated in TSMC CMOS 0.25 µm technology (Fig. 7). It has a size of 6.8 mm × 5 mm and a power dissipation of 3.5mW/channel.

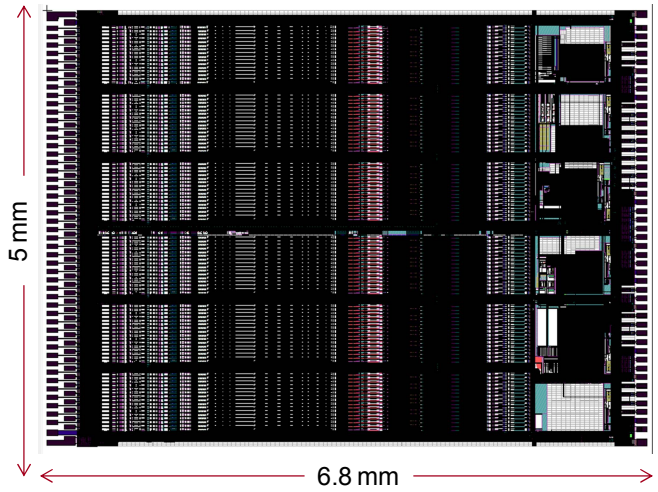

Fig. 7: Layout of eLine100.

The most relevant characteristic performance results of the ASIC in a test setup are reported here. The ASIC has also been characterized in several prototype detectors showing spectroscopic capabilities. Performance results in these prototypes are reported in [11].

A. Transfer characteristic, gain and linearity

This first set of measurements aims at testing the channel response as a function of the input charge, the behavior of the charge pump circuit, as well as the linearity and the gain of the device. In Fig. 8, the analog residue response measured at the output of the filter in a specific channel is reported. The characteristic was scanned using the internal 10-bit pulser. The pulser can operate in high-resolution mode using all 1024 levels to scan the first quarter of the dynamic range, or in low-resolution mode to scan the full dynamic range. The analog node in the channel is monitored using an auxiliary analog output implemented to monitor critical internal nodes for debugging purposes.

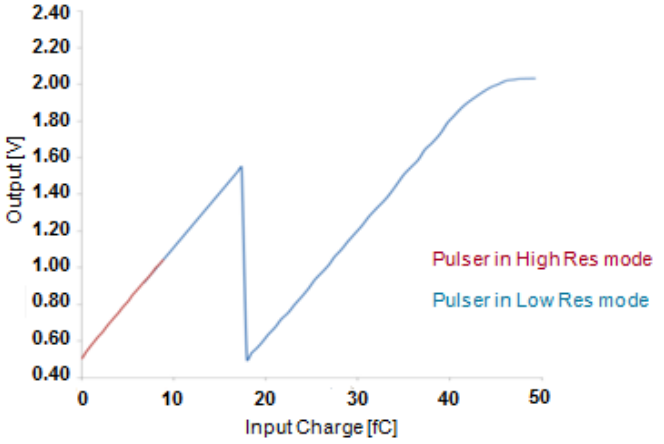

Fig. 8. Analog residue response measured at the output of the filter on a channel monitored using the auxiliary analog output.

The measured results are in agreement with the simulated curves. Fig. 9 shows the transfer characteristic of all 96 channels scanned with the internal pulser in low-resolution mode and digitized with an external 14-bit ADC. The curve show negligible gain dispersion.

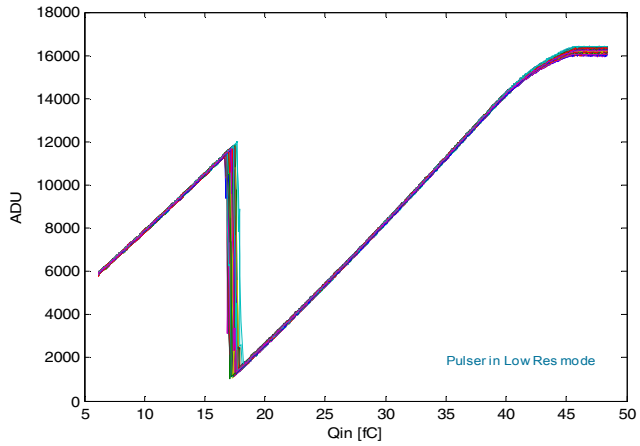

Fig. 9. Analog residue response measured at the output of a channel bank for all 96 channels.

A residual non-linearity below 1% has been measured, satisfying requirements. The overall channel gain is 58mV/fC, 3.4% smaller than the nominal value. The value is in line with the expected parasitic feedback capacitance.

The threshold dispersion in the pump comparator, activates the pump at different charge input values. This effect is irrelevant for the operation of the device since the reconstruction of the measured charge, combining the analog residue information and the pump bit, requires only the knowledge of the pump height [1, 6]. From the curves it is also apparent that the ASIC is able to measure signals up to 42fC which are equivalent to 120 photons at 8keV, meeting the requirement imposed by the XCS experiment.

B. Noise measurements

The second set of measurements aims at evaluating the noise performance of the ASIC. In these measurements, the filter was set to reach the flat top in 8µs, 16µs and 32µs. The last value is the typical row time required for the XCPS sensor. Fig. 10 shows the equivalent input r.m.s noise charge as a function of the channel. Good uniformity among the channels is achieved, with an average noise level of 55e$^-$ r.m.s. at 32µs, 62e$^-$ r.m.s. at 16µs and 75e$^-$ r.m.s. at 8µs. As series noise dominates at these time constants, the increase in noise with reduced filtering time is expected.

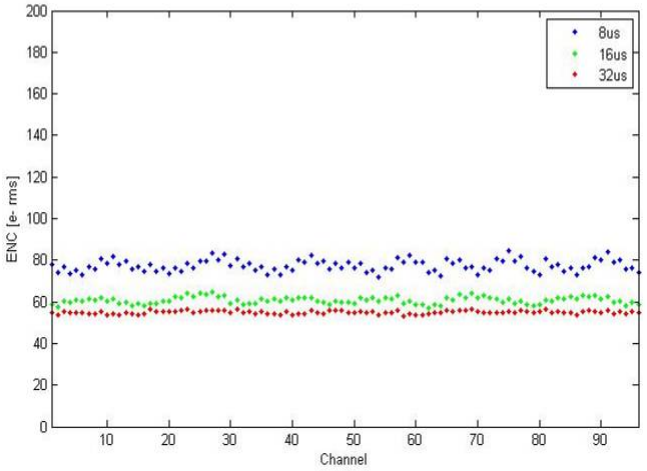

Fig. 10. Equivalent Noise input Charge (ENC r.m.s.) as a function of the channel.

In comparison, Fig. 11 shows the simulated noise behavior of the device as a function of the input capacitance showing agreement between simulated and measured values.

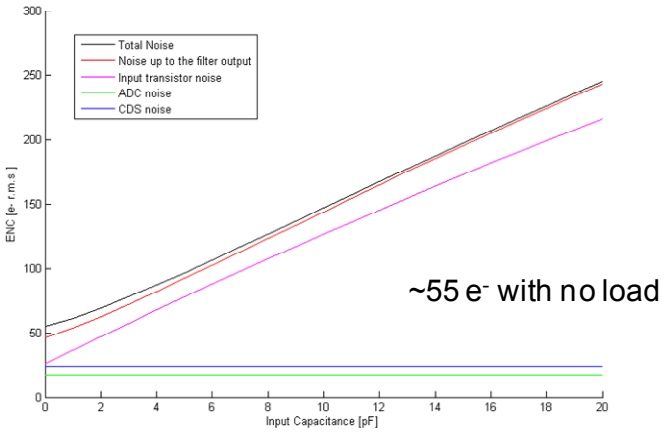

Fig. 11. Simulated Equivalent Noise input Charge as a function of the input capacitance for 32µs time slot operation.

It is also interesting to consider the plot in Fig. 12 in which the cumulative histogram of the noise of all channels referred to the input is reported. The Gaussian distribution shows a FWHM of 126e$^-$ (i.e., 55e$^-$ r.m.s.) as in the previous measurement.

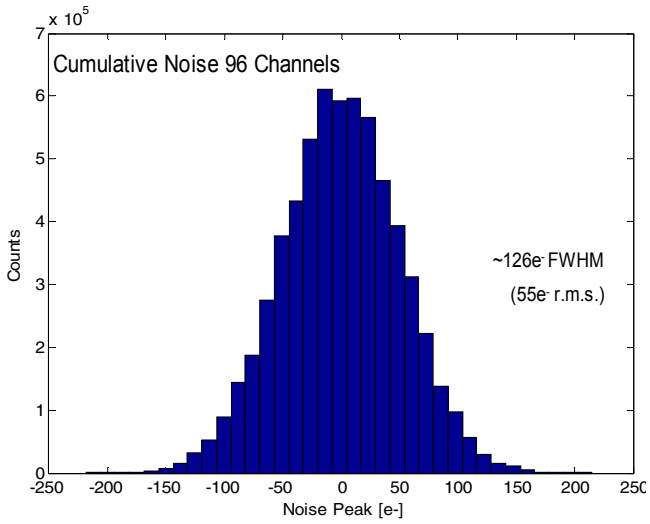

Fig. 12. Cumulative histogram of the noise of all channels referred to the input.

VI. Experimental Results

As an example of the performance achievable with eLine100, we here report a measurement of single 8keV photons (Fig. 13) from the fluorescence of a copper target. In the experiment, a planar-geometry silicon sensor with active edges was used to convert the x-rays into an electronic signal [12]. The sensor chip had dimensions of 3.4mm by 2.4mm, divided into sixteen strip elements and enclosed by a plasma-diced, doped edge (Fig. 1). The sensor was actively cooled to 6ºC. The achieved ENC at the input of the bonded channels was 66e- r.m.s. which corresponds to an energy resolution of about 560eV FWHM.

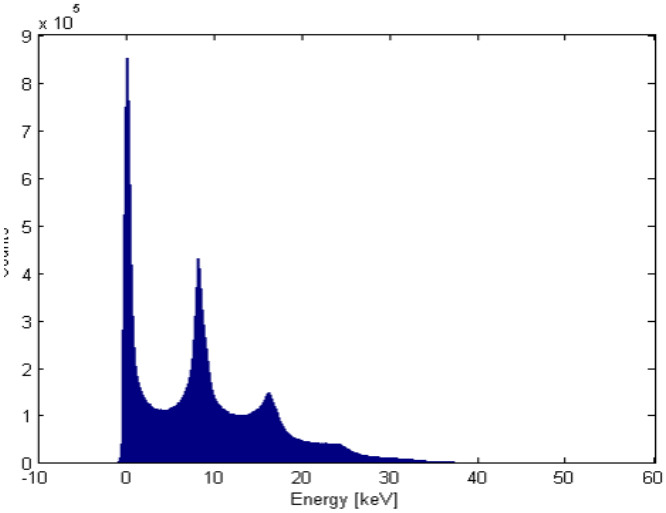

Fig. 13: Single 8keV photons from the fluorescence of a copper target.

Additional experimental results with a different setup will be presented in [11].

VII. Conclusions

A class of ASICs, eLine, for the readout of column-parallel readout sensors has been designed to satisfy the demanding experiments at LCLS. The class is composed of two front-end ASICs and a dedicated controller. eLine100 is the front-end tailored for ultra-low noise applications. Optimized for XCPS detectors and the requirements of the XCS experiment at LCLS, it is a charge-integrating time-variant architecture operating synchronously with the LCLS beam structure. To cover the large input dynamic range of 100 photons at 8kV, a charge pump architecture has successfully been implemented. The ASIC presents (Tab. I) a noise floor of 55e- r.m.s. at room temperature. It has a total dissipated power of about 3.5mW per channel and it is suitable for applications requiring resolution on the order of 100e- r.m.s. and signals up to 120 photons at 8keV. It is suitable for fast frame rate detectors and can process up to 250k pixel/s on each channel.

TABLE I
eLine100 Performance

Technology	TSMC 0.25µm
Die Area	6.8 mm x 5 mm
Number of Channel	128
Optimum Input Load	2pF
Channel Gain	58mV/fC
ENC	55e- +8e-/pF r.m.s.
Maximum Signal	260ke- (120 photons @ 8keV)
Dynamic Range	74dB
Power Consumption	3.5mW/channel
Read-out Speed	250k pixel/s/channel

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