A SOLID-STATE NANOSECOND BEAM KICKER MODULATOR BASED ON THE DSRD SWITCH

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Abstract

A fast solid-state beam kicker modulator is under development at the SLAC National Accelerator Laboratory. The program goal is to develop a modulator that will deliver 4 ns, ±5 kV pulses to the ATF2 damping ring beam extraction kicker. The kicker is a 50 Ω, bi-polar strip line, 60 cm long, fed at the downstream end and terminated at the upstream end. The bunch spacing in the ring is 5.6 ns, bunches are removed from the back end of the train, and there is a gap of 103.6 ns before the next train. The modulator design is based on an opening switch topology that uses Drift Step Recovery Diodes as the opening switches. The design and results of the modulator development are discussed.

INTRODUCTION

There are many applications that benefit from very fast high power switching. However, at MW power levels and nanosecond time scales, solid state options are limited. One option, the Drift Step Recovery Diode (DSRD) has been demonstrated as capable of blocking thousands of volts and switching in nanosecond to sub-nanosecond ranges [1-4].

When used as an opening switch, the DSRD exhibits a very fast turn off transient. The process is described in detail by its pioneers in [5,6]. In essence, charge is pumped into and then extracted from the DSRD under pulsed conditions. The turn off transient occurs precisely when the pumped charge is equal to the extracted charge and the DSRD is switched off.

At the SLAC National Accelerator Laboratory, a DSRD is being used as an opening switch in the development of a fast kicker modulator. The modulator is designed to create ±5kV pulses with <1ns rise and fall time on a 50Ω strip line kicker. As is common in beam optics, the absence of power in the kicker before and after the pulse is very important. The entire ±5kV kicker modulator is composed of two identical 5kV pulsing circuits, each with its own DSRD component. This paper describes the modulator topology and the status of tests on one of the two 5kV pulse circuits.

MODULATOR CIRCUIT

Each 5 kV pulser uses a resonant circuit to pump the DSRD and then extract the charge producing the turn off transient effect. This circuit is shown in Figure 1. Switches Sw1 and Sw2 are composed of high voltage, low inductance MOSFET arrays. They are used to pump the DSRD and remove residual energy. The parasitic capacitance of the switch array, C_{Sw}, is determined by the

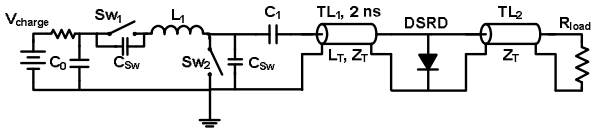

Figure 1: The DSRD kicker circuit.

Table 1: Modulator circuit specifications

Parameter	Value
V_{Charge}	100 – 1000 V
C_0	300 nF
C_{Sw1}	200 pF
C_{Sw2}	400 pF
L_1	200 nH
C_1	1 – 10 nF
L_T	90 nH
Z_T	50 Ω
R_L	50 Ω

arrangement of the MOSFETs in the array. Switch Sw_1 is composed of 2 series by 2 parallel MOSFETs and Sw_2 is composed of 2 series by 4 parallel MOSFETs. Each switch array is capable of blocking 2 kV.

The DSRD kicker operates in 3 distinct stages. At the beginning of stage one, capacitor C_0 has been DC charged to V_{Charge}. Switch Sw_1 is then closed while Sw_2 remains open. Capacitance C1 is resonantly charged through the forward biased DSRD and voltage across R_{Load} remains very low. Capacitive voltage doubling is observed on C_1. The DSRD is pumped with charge under this forward biased state. DSRD current, shown in blue in Figure 2, returns to zero amps at time $T_1/2$ as calculated in Eqn 1. At this time Sw_1 is switched opened and Sw_2 is closed.

$$\frac{T_1}{2} = \pi\sqrt{(L_1 + L_2)\cdot C_1} \qquad (1)$$

At the beginning of the second stage, current resonantly flowing out of capacitance C1 is shunted to ground through Sw_2. This current forms the extraction of charge from the DSRD. The DSRD current, now shown in red in Figure 2, reaches its maximum value at time $T_2/4$, calculated in Eqn. 2. During stage two, energy is stored in the inductance of transmission line TL_1.

$$\frac{T_2}{4} = \frac{\pi}{2}\sqrt{L_1 \cdot C_1} \qquad (2)$$

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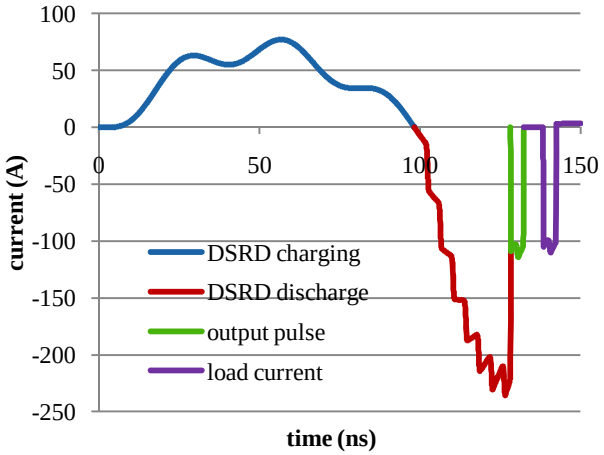

Figure 2: Simulated current at various points in the DSRD modulator.

Stage three begins when the DSRD is depleted of the pumped charge and abruptly turns off. The energy stored as current in the 2 ns transmission line TL_1 is commutated from the DSRD to transmission line TL_2, and is reflected toward the load by low impedance of C_1 and Sw_2. The output pulse, shown in green in Figure 2, is half of the peak current and twice the electrical length of TL_1. Current propagates through the 50Ω kicker to the matched impedance load. The load current, shown in purple in Figure 2, is absorbed by the load resistance. A load current of 100A corresponds with 5kV at the kicker.

TESTS

Tests on the described kicker modulator are underway to validate and refine the circuit. Several key parameters were varied to control the operating characteristics of the circuit. The most direct parameter, V_{Charge}, was used to increase the output voltage of the circuit. V_{Charge} was increased up to the point at which Sw_1 and Sw_2 were over stressed by voltage. Generally V_{Charge} was limited to 1kV or less. This was because during stage 2, voltage across Sw_1 was observed to oscillate about the charge voltage with amplitude equal to two times the charge voltage. This oscillation was produced by the LCL circuit formed between the storage capacitance, the switch parasitic capacitance and inductance L_1. On several occasions Sw_1 failed due to overvoltage.

The load voltage was measured with a 50Ω high voltage attenuator. Figure 3 shows the measured output voltage for two separate tests at different time resolution scales. The peak voltage was about 2 kV and the 10-90% rise time of the voltage was 1.4 ns. After the voltage pulse, the voltage at the 50Ω load remained very low demonstrating low residual power.

Figure 4 shows the output voltage produced by the kicker modulator while increasing V_{Charge} on capacitance C_0, an output voltage as high as 2.2 kV was recorded. The 2.2 kV output was measured with a charge voltage of

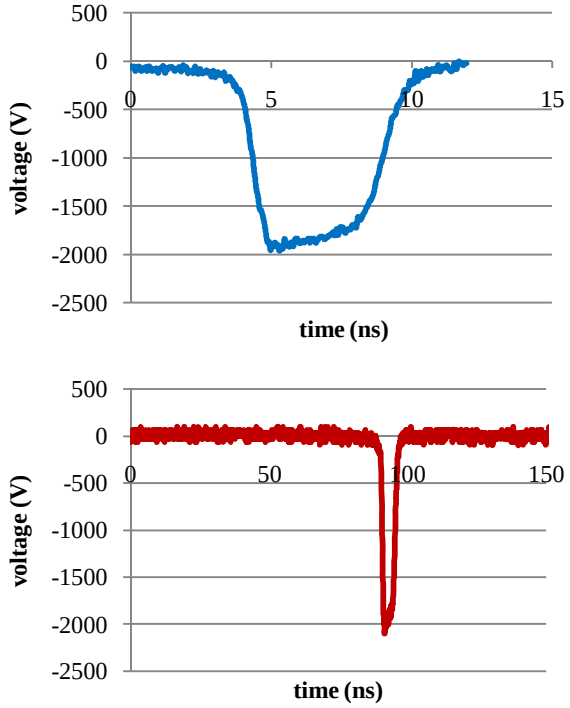

Figure 3: Measured voltage produced by the DSRD modulator at two different time scale resolutions demonstrating a) fast rise time and b) absence of residual power at the kicker.

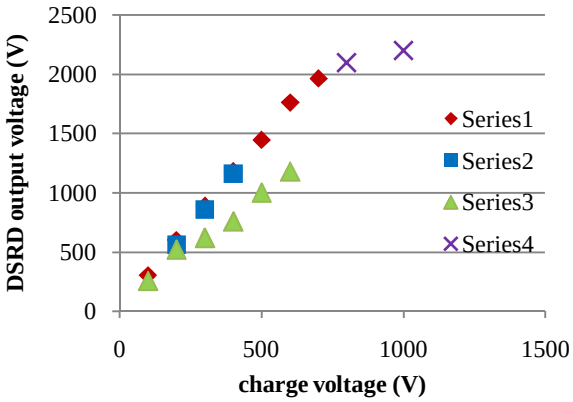

Figure 4: Measured peak voltage produced by the DSRD modulator.

1 kV, which is at the very upper stress limit of the circuit design.

To gauge the performance of the circuit, a comparison between DSRD current and output voltage was sought. In order to measure current, the DSRD was replaced in the circuit with a low resistance current viewing resistor (CVR). Unfortunately, this meant that the DSRD output voltage could not be measured simultaneously with output current, so measurements were made separately and then compared. An example of measured DSRD current is shown in Figure 5. Initially the current is positive when the DSRD would be undergoing pumping. The extraction

(negative) current is much greater in amplitude due to the closing of Sw_2. The DSRD should turn off abruptly when total charge is removed. The data in Figure 5 show that the peak current in the DSRD under those particular conditions would be 150A. With a 50Ω transmission line and load, this should correspond with an output voltage of 3.75kV.

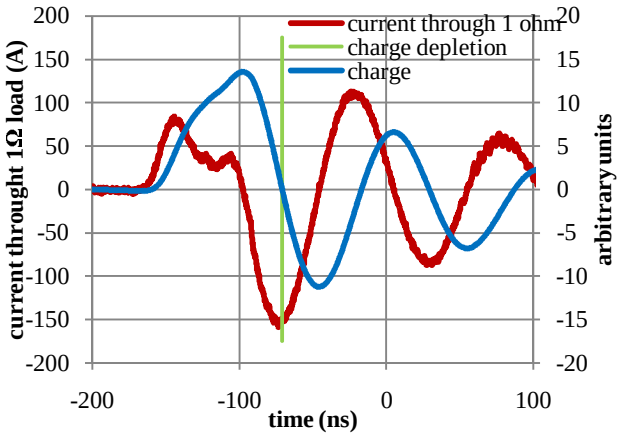

Figure 5: Measured current through 1Ω resistance estimating DSRD current. Green indicates when the DSRD abruptly turns off.

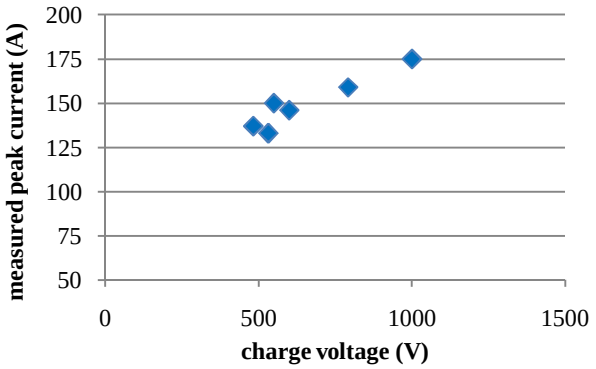

Figure 6: Measured peak current through 1Ω resistance.

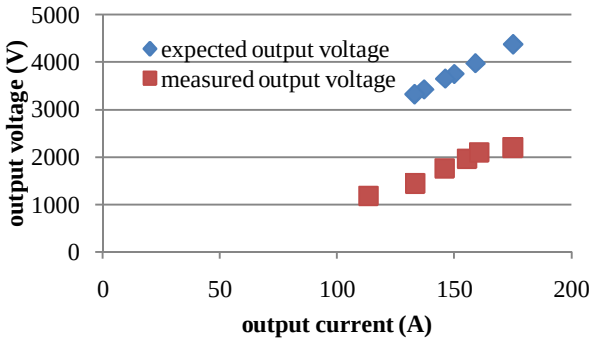

Figure 7: The blue data show the expected output voltage produced by the DSRD modulator based on measured current. The red data show the measured output voltage of the DSRD modulator at expected DSRD current.

Similar current measurements were made over a range of charge voltages. As the charge voltage was increased, the measured peak current increased. Figure 6 shows that for a particular set of data, the measured peak current ranged from 130A to 175A. This data was used to generate a plot of the expected output voltage with the DSRD. This is shown in blue in Figure 7.

Data were then taken with the DSRD reinserted into the circuit. Measurements were made over a similar parameter range so that the output current could be estimated without direct measurement. These data are included in Figure 7. A comparison between the measured output voltage and the expected output voltage based on output current shows that the measured output voltage from the DSRD is lower than expected.

STATUS

The solid state DSRD based kicker modulator presented in this paper demonstrated voltage pulses of several kV with rise times of less than 1.5 ns. The circuit demonstrated that very low if any residual charge remained in the kicker after the voltage pulse occurred. Ongoing efforts will turn toward increasing the output voltage produced by the circuit.

According to the circuit design, the magnitude of the output voltage was directly limited by the breakdown of the MOSFETs used to pump the DSRD under high voltage. In order to further increase the output voltage of the kicker modulator, the charge voltage will have to be increased beyond 1kV. Improvements are required to prevent breakdown of the pumping MOSFETs at high voltage. Extra series MOSFETs are one option.

The measured output voltage of the DSRD kicker was less than expected by a factor of two. This discrepancy needs further investigation. It is possible that DSRD current is lower than expected under charge extraction or that the DSRD reverse leakage current is greater than expected. Both theories will be investigated. The first step will be to develop a way to measure the DSRD current while it is used to produce high voltage.

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