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SLIM, Short-pulse Technology for High Gradient Induction Accelerators*

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Abstract

A novel short-pulse concept (SLIM) suited to a new generation of a high gradient induction particle accelerators is described herein. It applies advanced solid state semiconductor technology and modern microfabrication techniques to a coreless induction method of charged particle acceleration first proven on a macro scale in the 1960's. Because this approach avoids use of magnetic materials there is the prospect of such an accelerator working efficiently with accelerating pulses in the nanosecond range and, potentially, at megahertz pulse rates. The principal accelerator section is envisioned as a stack of coreless induction cells, the only *active* element within each being a single, extremely fast (subnanosecond) solid state opening switch: a Drift Step Recovery Diode (DSRD). Each coreless induction cell incorporates an electromagnetic pulse compressor in which inductive energy developed within a transmission-line feed structure over a period of tens of nanoseconds is diverted to the acceleration of the passing charge packet for a few nanoseconds by the abrupt opening of the DSRD switch. The duration of this accelerating output pulse - typically two-to-four nanoseconds - is precisely determined by a microfabricated pulse forming line connected to the cell. Because the accelerating pulse is only nanoseconds in duration, longitudinal accelerating gradients approaching 100 MeV per meter are believed to be achievable without inciting breakdown. Further benefits of this approach are that, (1) only a low voltage power supply is required to produce the high accelerating gradient, and, (2) since the DSRD switch is normally closed, voltage stress is limited to a few nanoseconds per period, hence the susceptibility to hostile environment conditions such as ionizing radiation, mismatch (e.g. in medical applications the peak beam current may be low), strong electromagnetic noise levels, etc is expected to be minimal. Finally, we observe the SLIM concept is not limited to linac applications; for instance, it could be employed to both accelerate the beam and to stabilize the superbunch mode of operation in circular track machines.

Introduction

The classical induction linac can be regarded as a linear array of magnetic core transformers, the secondary of each being a longitudinal moving charged beam (or packet) rather than a shared single straight copper wire. Assuming single-turn primary windings and proper phasing of the excitations, the overall operative accelerating potential applied to a charge packet equals the sum of the voltages applied to the primaries. This general induction principle is recognized as the most powerful method for accelerating multi-kilo-ampere beams when high peak power delivery to the beam is desired.

A competing but less well known induction acceleration technique was developed in Russia in the 1960's [1]. It was "coreless"; that is, it did not employ magnetic materials. Nevertheless, it depended upon rapid rate of change of magnetic flux to generate accelerating electric fields. This scheme involved staged triggering of a chain of high

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voltage (HV) gas switches driving planar transmission lines which sequentially impressed longitudinal electric fields on the moving charge packet to progressively accelerate it. This "macro" ***coreless*** induction accelerator, early precursor of the high gradient "micro" linac (SLIM) proposed herein, achieved much greater accelerating gradients than typical present day induction machines; these generally exhibit gradients of approximately 1 MeV/m.

A fivefold increase of the accelerating gradient in coreless induction accelerators was demonstrated in the 1980's in a Dielectric Wall (DW) accelerator structure. In this case switching was provided by turn-ON photoconductive switches [2]. A subsequent significant advance in the coreless DW structure was the introduction of a high gradient insulator that also served as vacuum envelope encompassing the beam [3]. At that time, some investigators believed that integration of a cast solid dielectric in the pulse forming lines with a high gradient vacuum interface and SiC photoconductive switches might achieve gradients approaching 250 MeV/m. Unfortunately this DW accelerator architecture faced several serious challenges. In particular, prior to each triggering of the switch, the pulse forming lines and the photoconductive switches are subject to substantial voltage stress for a significantly longer period than the pulse duration itself. Consequently, to avoid field emission of electrons, secondary electron avalanches, and high voltage breakdown, the accelerating gradient must be limited. A second disadvantage is that conversion efficiencies of photons-to-carriers in photoconductors are generally less than one per cent, which means the light triggering system must be large - especially if the beam energy is in the hundred MeV range and the peak current is several hundred amperes. A further disadvantage is that the characteristic slow decay of photoconductivity limits the potential pulse rate of such DW accelerators. This approach has not reached a dead end, however G. Caporaso et. al. have recently overcome a number of these difficulties.

Based on R&D efforts conducted in the 1980's (see [2] and [5]), a novel and more attractive high gradient coreless induction linac concept emerged that does not suffer the above disadvantages. The general features of this approach are as follows: the natural state of the solid state switches is ON (a current conductive state) hence the solid state switches and pulse forming lines are voltage stressed only during the pulse itself. In this coreless induction system, energy is developed in the magnetic field when the switches are ON, and only for short intervals (several nanoseconds) are the switches OFF and stressed. Furthermore, because the storage is inductive, only low voltage power supplies are required. (A further benefit is that these supplies typically exhibit superior reliability and lower costs than high voltage supplies.) Note the essential distinction of this concept is the use of an extremely fast solid state opening switch. At that time, the Drift Step Recovery Diode (DSRD) [4] was recognized as a highly promising opening switch for this purpose. In 1989 integration of the DSRD and advanced dielectric materials into an induction system was first proposed for e+e- colliders [5].

Upon opening, the DSRD switch abruptly diverts stored magnetic energy to acceleration of the charged particle beam. Because the accelerating pulses need only be nanoseconds in duration, there is reason to expect longitudinal accelerating gradients to approach 100+ MeV per meter. And, because this approach avoids use of magnetic and photoconductive materials, one can envision accelerator operation at repetition rates in the MHz regime. Nevertheless, to achieve this performance with a DSRD switch the pumping charge in

both forward and reverse directions through the device ***prior to its opening*** must be controlled very precisely. The SLIM based accelerator relies upon these same insights but uniquely integrates advanced dielectric materials and the DSRD solid state nanosecond opening (OFF) switch into the induction cell.

Specifically we intend to implement the SLIM concept by exploiting a proven solid state pulse generation method which (1) can increase the output power within each coreless induction cell up to the megawatt range and (2) can reduce rise and fall times of the accelerating potential to one nanosecond or less. The DSRD is ***only active element*** in each coreless induction cell. (Conventional step recovery diode switches do not open sufficiently rapidly and do not function in the megawatt range.) Note the DSRD's referred to herein are comprised of multiple p-n junction diodes in series stacks - ten to fourteen junctions would be typical for a 10kV standoff.

First, in Section I we present the theoretical basis for the use of DSRD's for generating flat-topped nanoseconds-duration current pulses, in particular in resistive loads. Presently this technology is being developed for beam kicker applications [6]. In Section II we introduce the SLIM coreless induction accelerator concept which, similarly, is dependent upon subnanosecond DSRD switching. (This SLIM concept was initially presented by the authors on the Muon Collider Mini Workshop at Fermi National Laboratories in June 2008.) Section III presents the results of relevant DSRD pulse-generation experiments and simulations.

I. Designs for producing 600 + KW, 2nsec pulses in a resistive load using the DSRD opening switch.

One of a number of alternative DSRD-based pulse compressor circuits is based (Figure 1) on two switches. The first switch, external to the accelerating cell, determines the duration of the pumping pulse that is subsequently compressed. This switch (Sw) is a fast ON/OFF switch - most likely a HV MOSFET. The second switch is an extremely fast OPENING (OFF) switch (D1) which is a DSRD. It interacts with a pulse forming line (T1) to determine the duration of the output pulse. The latter occurs during the last of three successive time periods. The first period is the "pumping" interval $t1 < t < t2$, where t1 and t2 are the instants when the first (conventional) switch is turned ON and OFF respectively. During this pumping interval current builds up within L1 and also - very importantly - forward current develops in the DSRD stack. The second time interval is from t2 to t3 where t3 is the instant when the DSRD abruptly opens (i.e. when its minority carrier supported reverse current terminates). The final time period is from t3 to t4 where $tp = t4 - t3$ is the duration of the current pulse impressed on the load R1. This duration equals the round-trip time of the pulse forming line.

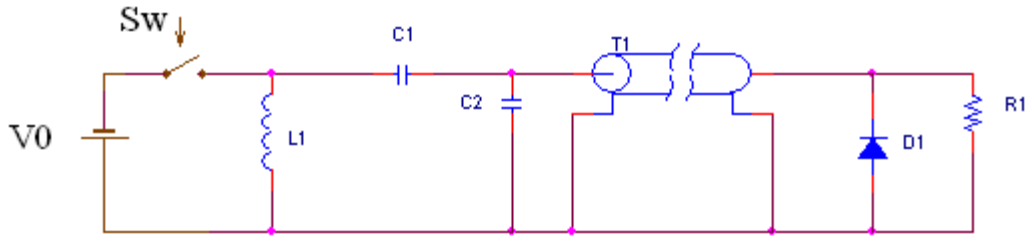

Fig.1 Simple diagram of two stage voltage booster

One critical aspect of the DSRD justifies the complexity of this and other functionally equivalent circuits: the pumping interval must be short (i.e. preferably 50 nsec or less) to ensure the populations of injected minority carriers are confined very near to the metallurgical p-n junctions within the DSRD stack. If the minority carrier distributions were allowed to reach steady state, as is typically the case with conventional step recovery diodes, the abrupt opening of the DSRD switch would be compromised by diffusion of the minority carriers.

For a specific example consider the case in which t2-t1 = 150nsec, L1 = 40nH, and V0 = 120V. The pumping pulse is shown in Fig. 2 where the trace shows that the switch is closed at t1 = 0 and stays ON until t2 = 150 nsec. (This is longer than the optimal 40-50 nsec on-duration but is convenient for modeling purposes.)

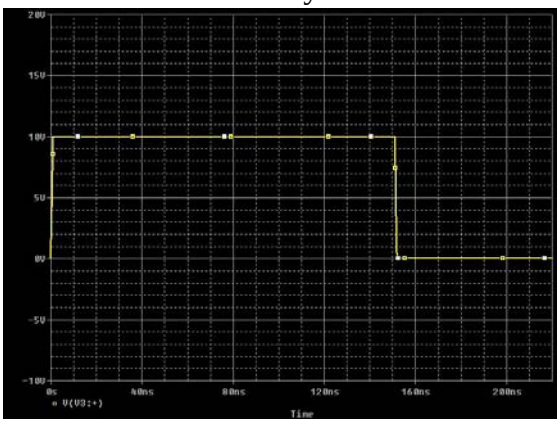

Fig. 2 The trigger pulse for ON/OFF Sw

The voltage across inductance L1 and current in the coil L1 vs. time are shown in Figures 3 and 4 respectively.

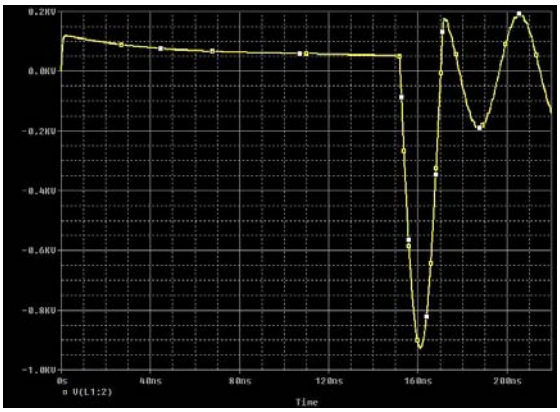

Fig. 3 Voltage across inductor L1 vs. time

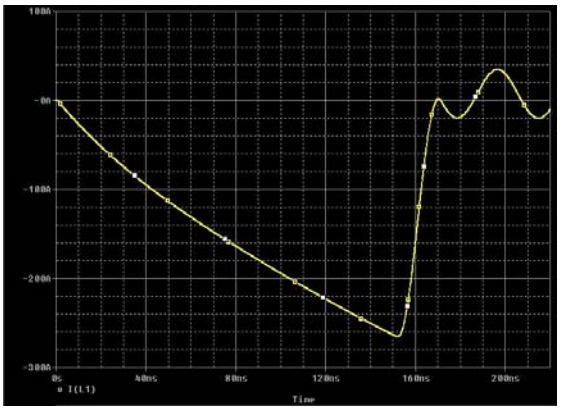

Fig. 4 The current in inductance L1 vs. time

In a truly ideal case the voltage across the inductance would be constant vs. time but in practice there are small resistive drops in the Sw, V0, and L1 loop, hence the model shows a voltage drop vs. time apparent in Fig 2 for the t1 <t <t2 (pumping) interval.

For the conditions presented above the maximum current is Im~260A for t = t2. For capacitance values of interest, as described below, there is the essential but small (~11%) leakage of current into the transmission line which forward biases the DSRD. Note the transmission line effectively acts as an inductance L2 during this first time interval.

The period of energy accumulation for the output pulse ends at t=t2.The switch Sw is then opened, changing the circuit topology, and the second transient period is started.

Because the current in inductor L1 cannot be interrupted instantly it commutates to the balance of the circuit as modeled in Fig. 5.

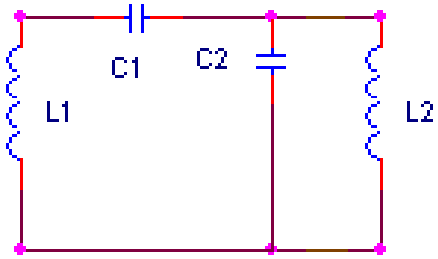

Fig. 5 Idealized circuit configuration after t = t2. Latent resistances are ignored

This LC-circuit has four natural frequencies, the fastest of which is an oscillation with a period T where

$$T = 2\pi \cdot \sqrt{\frac{L_1 L_2}{L_1 + L_2} \cdot \frac{C_1 C_2}{C_1 + C_2}}$$

If, for instance, C1=30nF, C2=1.5nF, and L2=100nH, then half of the oscillating period would be 20 nsec. Assuming these values the trace presented in Fig. 6 illustrates the expected transient current in capacitor C2. Upon the opening of the on/off switch (Sw) at t2 the large current developed in L1 compels an overwhelming reversal of current through C1 which is initially satisfied by current through C2. But C2 and L2 comprise a parallel resonant pair, and hence, after a brief (characteristic) half-cycle interval, the current though L2 (i.e. series current through the transmission line) and the voltage across C2 will have fully reversed.

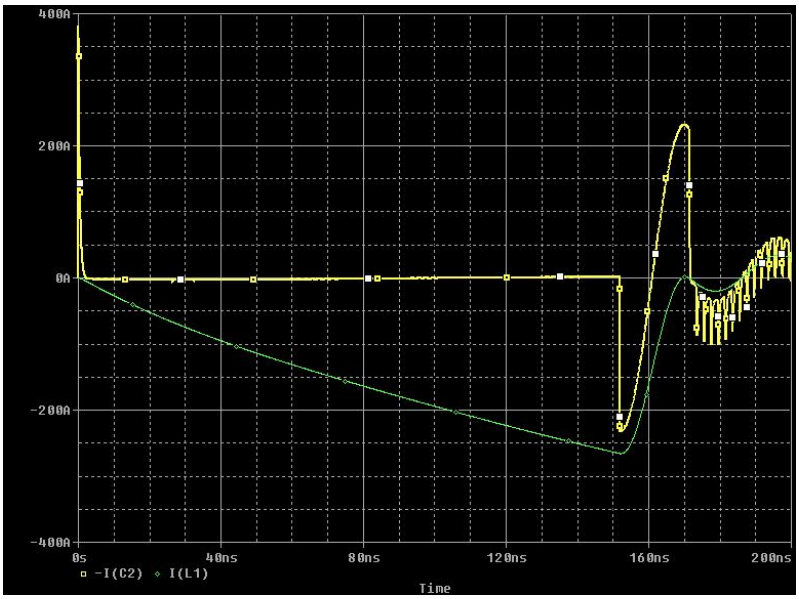

Fig. 6a Trace of current in C2 (yellow) and L1 (green) currents during the first and second periods

(Note this current direction in L2 is consistent with the development of a blocking voltage on the DSRD.) Consistent with imposing this current on the C2-L2 pair a large voltage develops across L1. This L1 voltage trace is displayed in Fig. 3 and the related currents are shown in Figure 6a and 6b. For the circuit parameters mentioned above, the voltage at the L1 – C1 junction reaches a peak of ~940V, which corresponds to a voltage gain of ~7.8. The second transient period ends – by design – when, simultaneously, the current in L2 reaches its negative limit extreme, and the minority carriers in the DSRD have been extracted. At this instant (t3) the space charge regions within the p-n junctions comprising the DSRD stack abruptly expand to support the voltage established by the current within the resistive load. The actual rate of this extreme (subnanosecond)

opening depends on the specific, tailored physical properties of the p-n junctions within the DSRD stack (for example, the doping profiles, the carrier concentration, physical area of p-n junction, etc.) and parasitic capacitances.

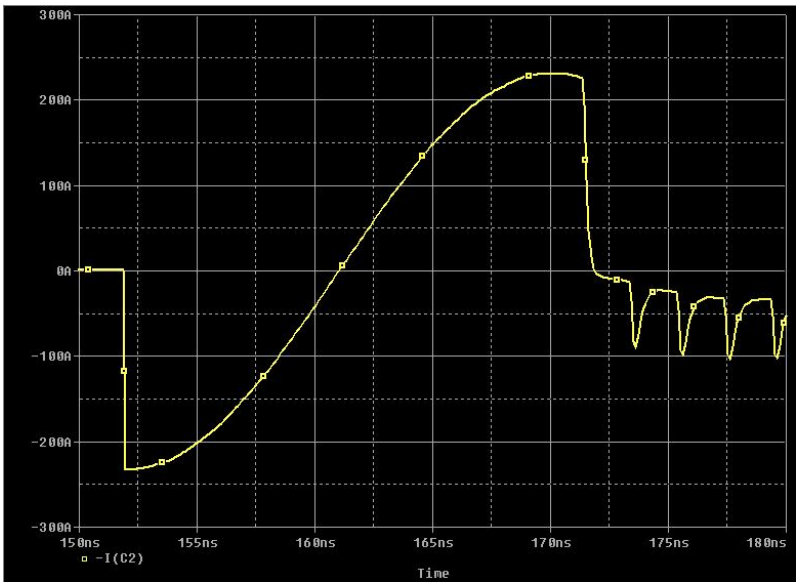

Fig. 6b An expanded time scale view of the high current half-cycle following the pump interval (t1-t2)

The properties of the delivered pulse involves transmission and reflection related to the transmission line during the third period (i.e. during $t3 < t < t4$, where $tp = t4 - t3$). Before discussing wave processes during this period, we consider the experimental current traces for the DSRD itself and the total current delivered by the transmission line. (Note the difference between these is the current carried by the resistive load.) These currents are shown in Figure 7 for the second and third periods in Fig. 7.

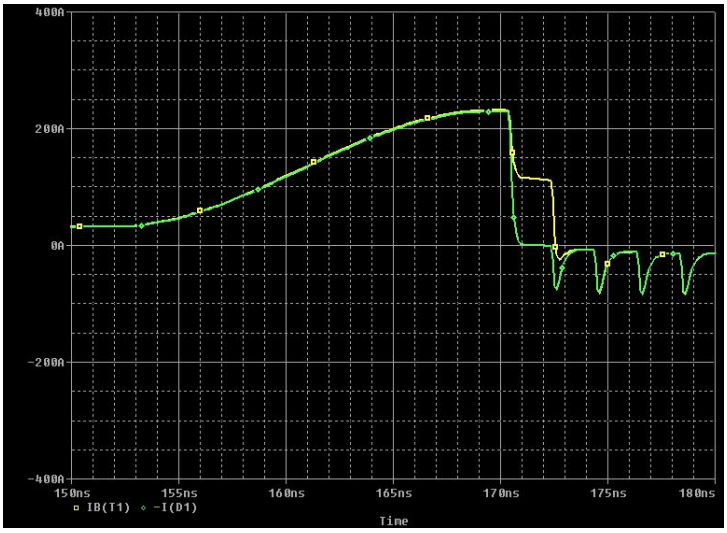

Fig. 7 The DSRD current (green) and the transmission line (L2) current on its end (yellow) vs. time

The abrupt collapse of reverse current in the DSRD denotes the beginning of the pulse during which the (maximum) current through the transmission line is split between the resistance load and a reflected wave into the transmission line. Here is convenient to consider the matching impedance case in which the characteristic impedance of the transmission line is equal to the load resistance of 50 Ohms, and the electrical length of the transmission line is 1 nsec. For these parameters conditions, the currents in the DSRD and the transmission line from 170 nsec to 175nsec would be as shown in Fig. 8.

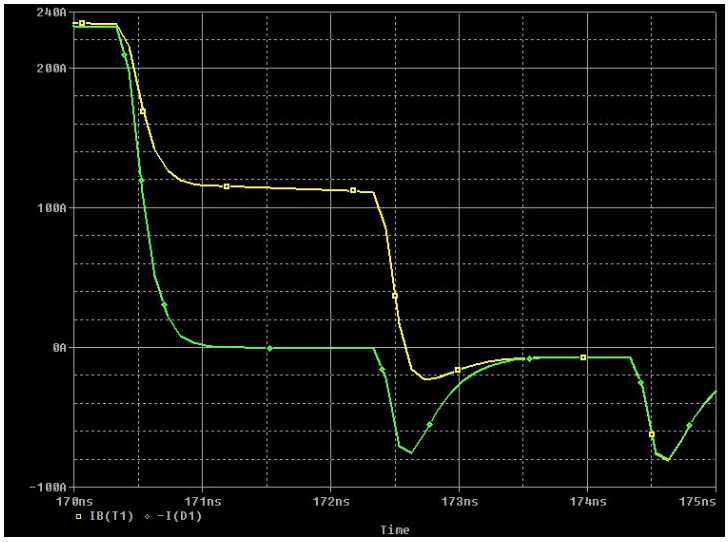

Fig. 8 The DSRD current (green) and the transmission line current on its end (yellow) vs. time for an interval of 170nsec-to-175nsec

The corresponding current trace vs. time for the 50 Ohm load resistor is shown in Figure 9.

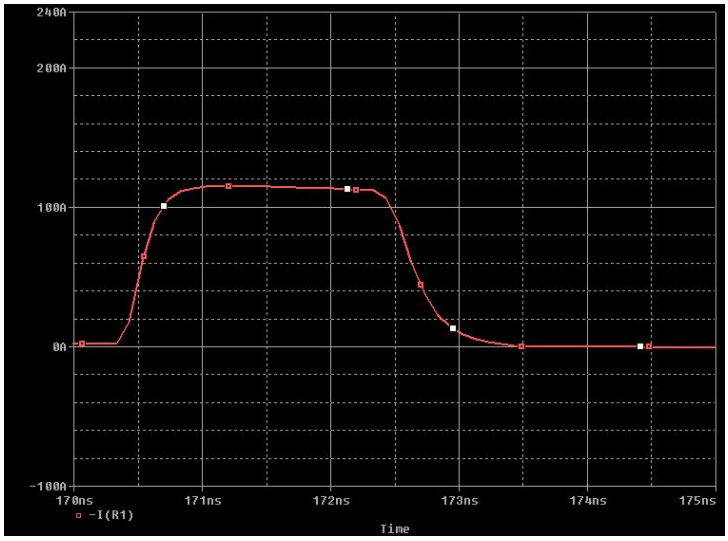

Fig. 9 Load current vs. time for third period (170nsec-to-175nsec)

It should be apparent that when the DSRD switch opens half of the current must be commutated to the 50 Ohm load resistor and the other half must be reflected into the 50 Ohm transmission line. The left-traveling waveform associated with the latter arrives at C2 after one nanosecond where C2 effectively presents a short circuit at the frequencies of interest. This in turn produces a reflected wave in the transmission line that, after one more nanosecond, presents the load (and open DSRD) with a short circuit, abruptly terminating the current flow in the load. During the intervening two nanoseconds the current in the load will have been maintained, hence the load will have experienced a sharply delineated flat-topped current pulse.

For the circuit parameters as mentioned above, the voltage on the 50 Ohm load is ~5.75 kV and the pulse width is 2 nsec. The corresponding output pulse power is 661 kW and the total voltage gain is ~48.

Various other transmission-line circuit topologies can exploit the abrupt opening of the DSRD to produce short flat-topped pulses. On the other hand, other topologies would be suitable for generation of short pulses using abrupt opening switches.

II. Modeling of DSRD-based Coreless Induction Acceleration

DSRD in shunt configuration:
The above method of the pulse generation based on the opening switch is adaptable to providing accelerating electric fields in a coreless induction linac. For example, a simplified cross section of a cylindrically symmetric candidate coreless induction cell is shown in Fig.10.

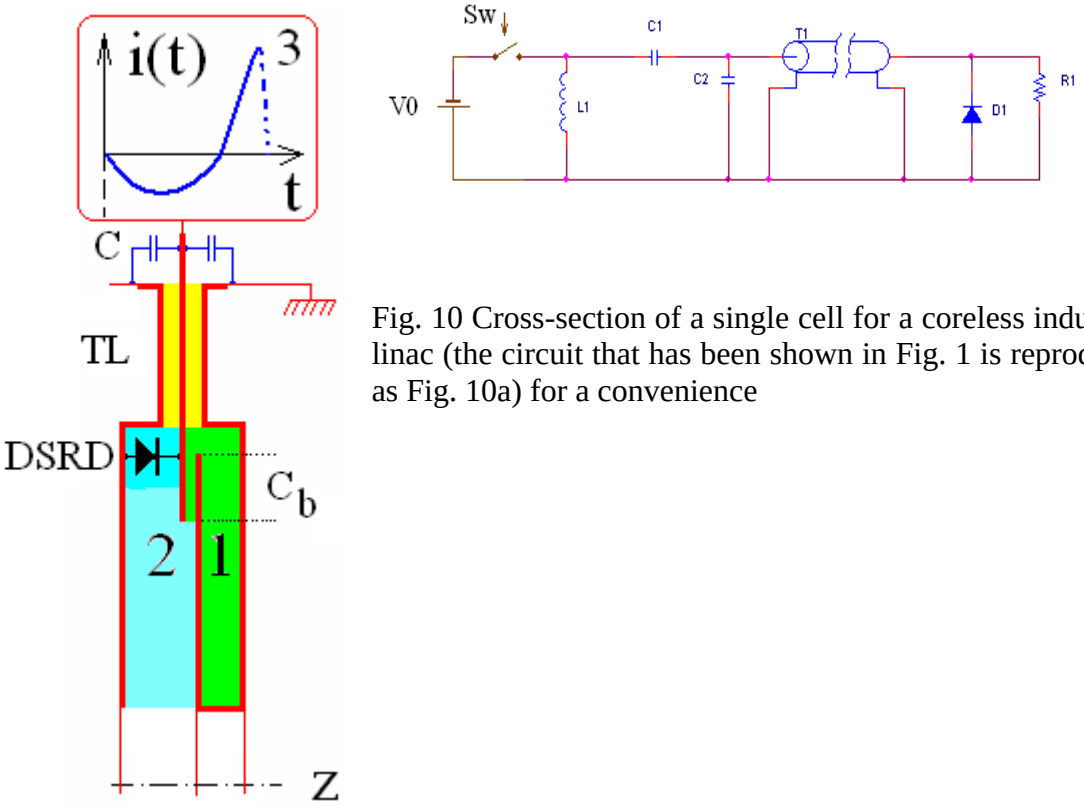

Fig. 10 Cross-section of a single cell for a coreless induction linac (the circuit that has been shown in Fig. 1 is reproduced as Fig. 10a) for a convenience

In this drawing the charged particle packet travels along the axis labeled "Z" and the circuit of Figure 1 is embedded into the coreless induction cell - the topology of the transmission line (TL), the input shunting capacitor (C) [formerly labeled C2], and DSRD are unchanged. For convenience the components sourcing the current are not shown again but the time-dependent current they deliver is represented (as item 3) in Fig. 10. There are two planar (strip-line) cavities 1 and 2; one is shorted on the small radius close to the particle beam trajectory and the other is an open gap at this radius. This open end of cavity 2 presents the charged particle beam with an accelerating electric field. Both cavities are effectively shunted by the DSRD at the outer radius but to avoid DC shorting of the source a capacitive gap (Cb) is introduced as shown. As discussed above in relation to the generation of a flat-topped current pulse in a resistive load, when the DSRD switch opens the current in TL, by design, is at its maximum. At this instant part of this current propagates in the two cavities toward the gap (the load) and the rest propagates backward in TL toward the capacitively shunted power source. In this

implementation case, the load is comprised of two cavities excited basically in parallel. Even though cavity 1 only briefly carries power, it serves an invaluable but subtle role: it provides a ground referenced outer surface to which the neighboring coreless induction cell can be abutted. This allows the coreless induction cells to be tightly stacked.

Let us evaluate the coreless induction parameters for accelerating a 690A beam with a 2 nsec pulse width. As it is seen in Fig. 9, a 2 nsec, 115A pulse into a 50 Ohm load is generated by the circuit shown in Fig. 1. If we distribute in azimuthal direction (around z axis) six transmission lines, each with its own DSRD, the effective source resistance perceived by the on-axis beam will be approximately 8 Ohm. A reasonable value of Cb capacitor may be Cb=100 pF in which case the peak voltage across it would be less than 1.5 kV. The predicted accelerating voltage in the gap (red) and the voltage across Cb (yellow) are shown in Fig. 11 for a period 150 nsec<t< 175 nsec.

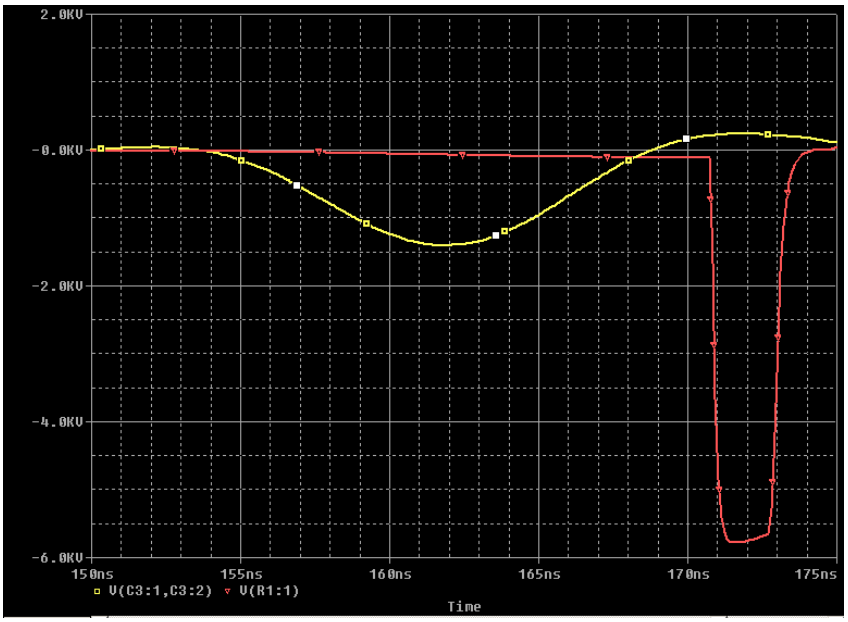

Fig. 11 Simulated accelerating voltage (red) and the voltage across the blocking capacitor Cb (yellow) vs. time

Consider the length of TL to be 20 cm filled with a medium having a dielectric constant of 2.25 to obtain a round-trip propagation time of 2 nsec. We estimate the length of DSRD assembly sufficient to support a 6 kV pulse would only have to be few mm in the axial direction. The section length of planar cavities 1 and 2 may be 30 um for a two nanosecond pulse width. This corresponds to the maximal breakdown electric field within the coreless induction cell of 200 MV/m. If one assumes a safety factor of 0.5, the average accelerating cell gradient would be comparable to the accelerating gradient of modern rf structures, i.e. 100 MeV/m. We stress that this E-field exists in the coreless induction structure only for a short period of time (a couple nanoseconds after the DSRD stack opens) hence breakdown would be unlikely if proper care has been taken during design of the coreless induction cell.

DSRD in series configuration:

An alternative and appealing scheme employs the DSRD in series and avoids the need for Cb as shown in Figure 12.

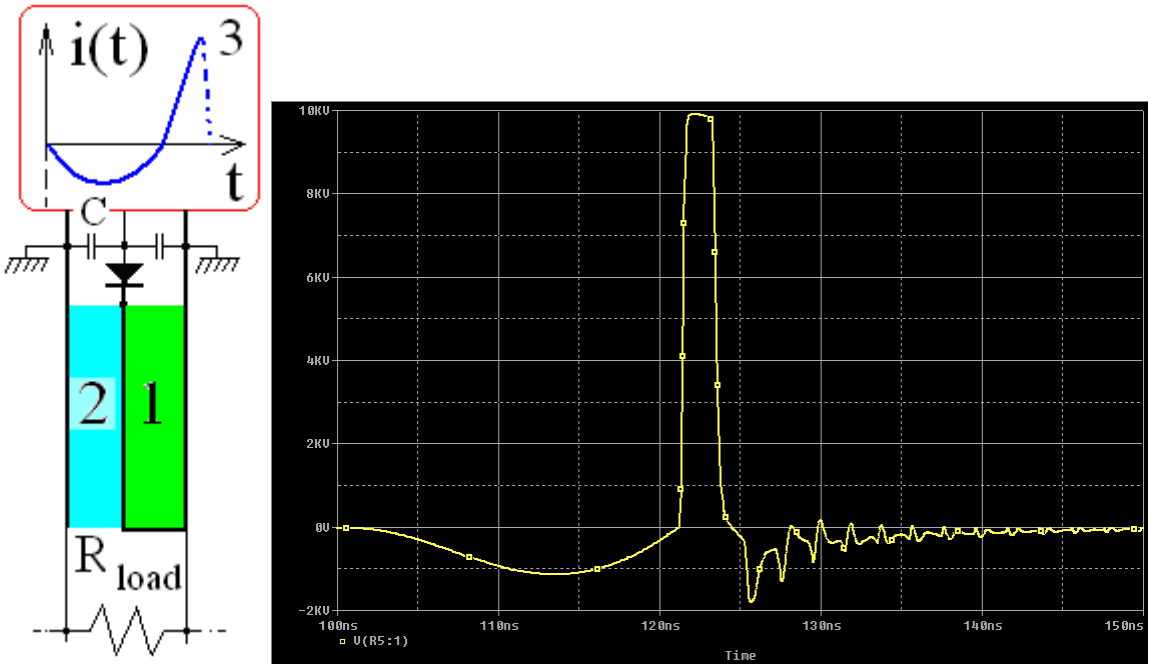

Fig. 12 a) Coreless induction cell with the DSRD stack in series and b) simulated beam loaded accelerating voltage

There the loading related to the existence of the charged particle beam is shown explicitly. A simulation of this coreless induction model was performed for the case of 2 nsec pulse width and 200A load current. The coreless induction cell input (yellow) and output (red) currents are shown in Fig. 13.

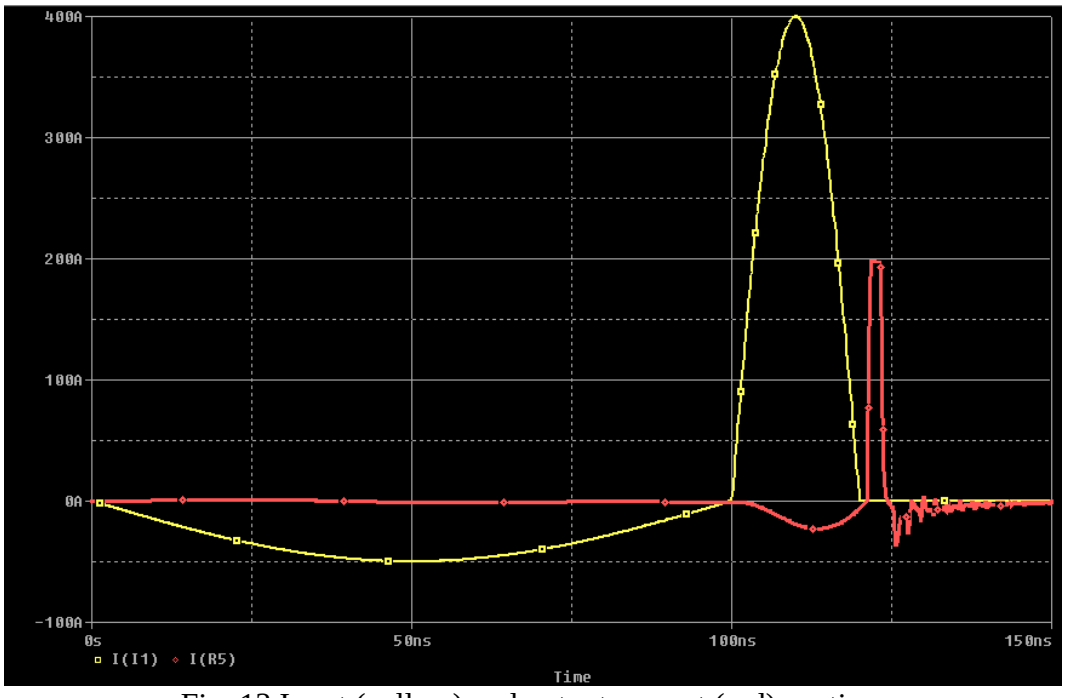

Fig. 13 Input (yellow) and output current (red) vs. time

Here the amplitude of DSRD current in the forward direction peaks at 50A midway through a half cycle of 100nsec duration. The cycle period is five times less for the reverse DSRD current and the peak amplitude of this reverse current is 400A.

There is an interesting and conceptually simpler circuit scheme for producing the desired time-dependent input current for driving a DSRD that is integrated into the shorted on the small radius cavity (or strip line). It leads to a variant that deserves serious consideration. The overall circuit diagram for this simpler scheme is shown in Fig. 14.

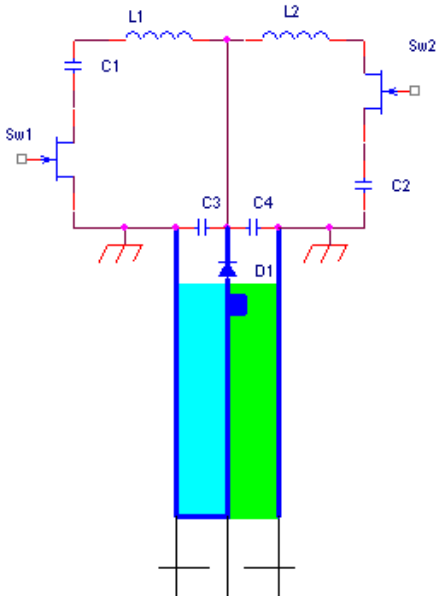

Fig. 14 Simplified circuit diagram for coreless induction cell employing a series DSRD

Two individual LC sub-circuits, each with its own switch, are employed. Capacitors C1 and C2 are precharged from a single power supply (not shown). When switch Sw1 closes a cycle of forward pumping of the DSRD diode D1 begins. The capacitance C1 and the inductance L1 determine the subsequent time dependence of this forward current. When this current reaches zero, Sw1 is opened and Sw2 is closed. The current in L2-C2 loop goes in the reverse DSRD direction. By design, L2 * C2 << L1 * C1 and L2 << L1; these conditions result in much greater peak current during the reverse current interval. The yellow trace shown in Fig. 13 illustrates the input current. This conceptually simpler circuit has two disadvantages, the need for two independent trigger channels for Sw1 and Sw2, and an even greater disadvantage, the peak current through Sw2 must be very high and the discharge period must be extremely short. But, taking a lesson from classic magnetic pulse compression schemes, we observe that Sw2 and the simple inductor L2 can be replaced by a single saturating magnetic inductor functioning as a closing switch. The circuit diagram for this variant is shown in Fig. 15.

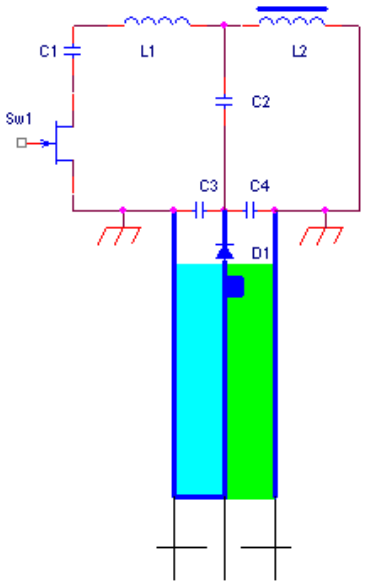

Fig. 15 Simplified circuit diagram for exciting a DSRD based coreless induction cell using a saturating magnetic closing switch

The magnetic core parameters must be chosen to ensure the core saturates at the instant the delivery energy from C1 to C2 (through L1, inductor, and DSRD) is complete. Once saturation occurs capacitor C2 quickly discharges through the DSRD in the reverse direction until the DSRD abruptly opens. Note in this case the inductive role of the

transmission line TL is served by the saturated inductor whereas the duration of the pulse is determined by the round trip time of the shorted (blue) cavity. The length of the two cavities (strip lines) would be 200-300mm to produce a 2 nanosecond pulse.

Results of simulations and preliminary experiments demonstrating proof-of-principle indicate that the SLIM concept is applicable to circular hadron machines: for example, induction synchrotrons [8] or/and fixed field alternating gradient (FFAG) machines [9]. Such machines require (1) an accelerating system capable of handling a long bunch and (2) means that ensures the long bunch will be stable in longitudinal direction during acceleration.

We propose the induction system for a synchrotron accelerating a superbunch would contain two types of SLIM-type modules. The first provides the acceleration for a long pulse width (a pulse width is slightly less than the revolution time). The second is precisely synchronized with the first one but solely serves to ensure longitudinal confinement of the superbunch during acceleration. The latter SLIM impresses a short and high voltage pulse on both the leading and trailing edges of the superbunch. The repetition rate for both induction modules is 1/T where T is a bunch revolution time.

Figure 16 illustrates a process of the long acceleration field formation.

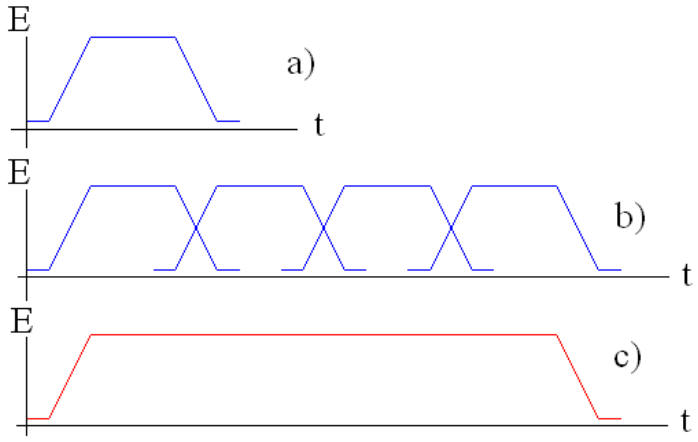

Fig. 16 a) accelerating gradient of single cell, b) accelerating gradient applied to the beam by four consecutive cells, and c) the effective total accelerating gradient

Let us assume that each SLIM cell produces an ideal accelerating pulse (Figure 16 a) with 2 nsec flat top and one nanosecond rise and fall. Because each cell is driven independently, they can be sequenced as shown in Figure 16b such that the beam will sense a continuous accelerating gradient (Figure 16 c). The overall duration of accelerating field experienced by the beam depends only on the number of cells employed. This approach is applicable to the acceleration of superbunches but to maintain nearly ideal superbunches one must ensure the accelerating field within each cell is negligible except during its intended acceleration pulse.

Intentional longitudinal containment of the superbunch during acceleration can also be achieved using the SLIM approach. The tendency for longitudinal spreading due to space charge can be cancelled by impressing an additional (moving) spatial electric field distribution generated by SLIM cells. In particular, the head and tail particles of superbunch must experience supplemental e-fields as shown in Figure 17.

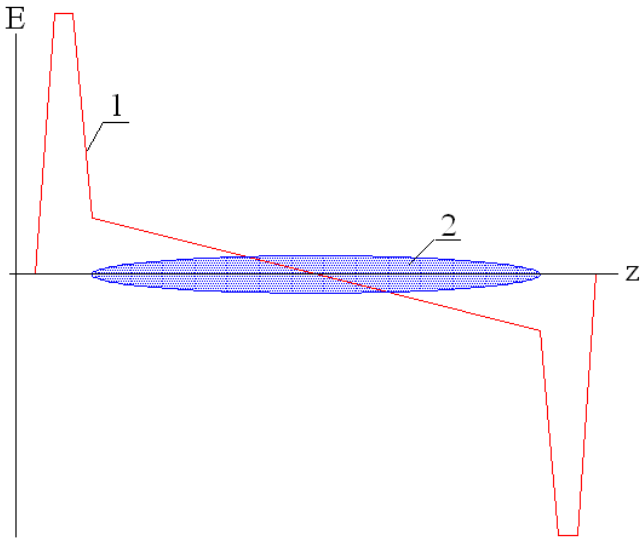

Fig. 17 Superposition of the supplemental E(z) field distribution (1) and the superbunch (2)

In order to maintain the longitudinal shape of the superbunch in circular hadron machines the corrective fields must function in the megahertz range, to which SLIM cells are well suited.

III. Experimental Proofs

The schematic circuit shown in Figure 1 was adopted for demonstrating the SLIM concepts. The experimental setup consists of a modified LLNL HV-MOSFET driver board, courtesy of Ed Cook (LLNL), and a Russian DSRD. These are shown in Fig. 16.

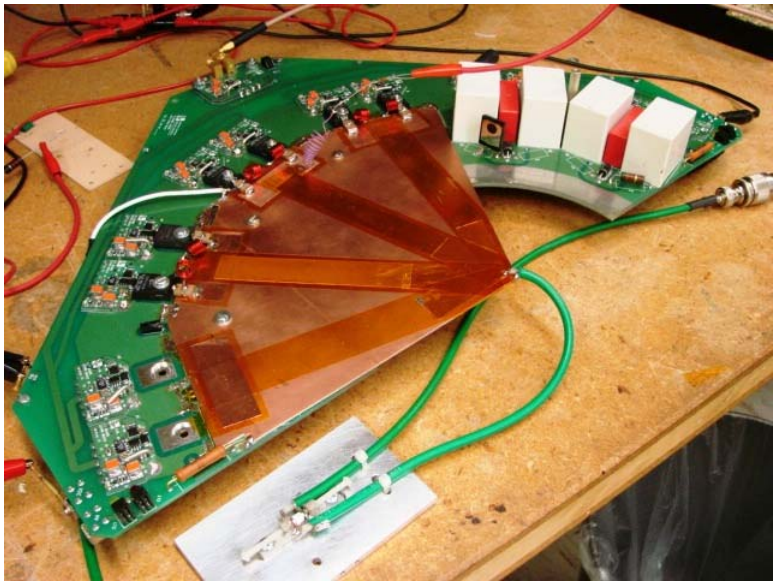

Fig. 16 Experimental setup

The setup consists of the following: six parallel APT1001RBVR MOSFETs, used as the primary ON/OFF switch, and ceramic capacitors of 0.1 uF @ 1 kV, employed as the primary storage energy and DC blocking capacitors. The pulse storage energy is developed within 250 nH storage inductances, one for each HV-MOSFET. A hand-crafted strip line functions as a 2.6nF capacitor shunting the driven end of a 23 cm long 50 Ohm cable loaded with 50 Ohms. This strip line fulfills the role of C2 in Figure 1. To ensure fidelity of measurement, a wide-band precision 26-

dB Barth attenuator [7] is used to scale the high voltage signal. The total attenuation is 800:1.

The output pulse observed on the resistive load is shown in Fig. 17.

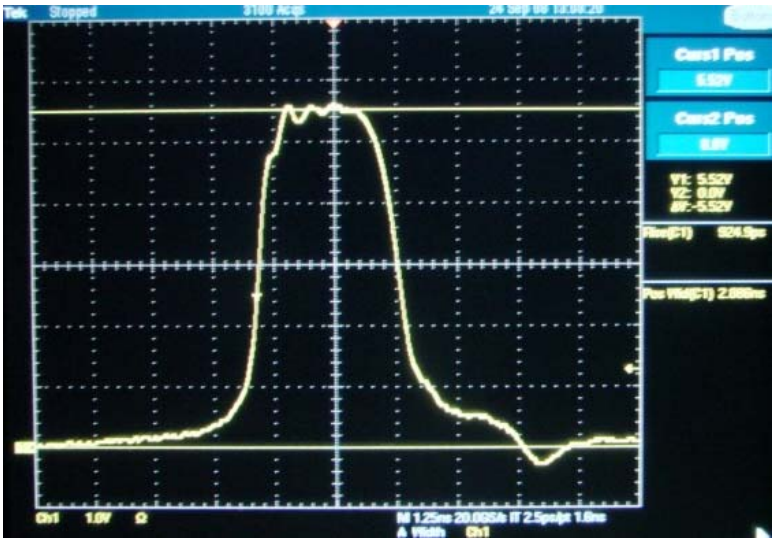

Fig. 17 A 387 kW output pulse. Horizontal scale is 1.25 nsec per div.

It has a 10-90 rise time of 0.9 nsec, a FWHM pulse width of 2.9 nsec, and an amplitude of 4.4 kV at the 50 Ohm load. In this case residual energy remains in the circuit after the body of the pulse has passed; this is less than 7% as shown in Fig. 21.

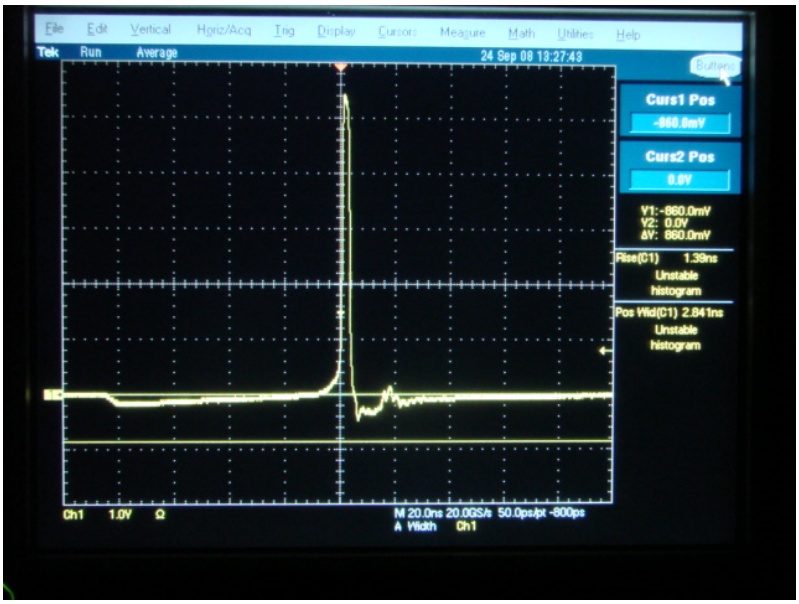

Fig. 18 The same waveform as Fig. 17 but the horizontal scale is 20 nsec per division

This residual energy would be very troublesome if the pulses to a linear array of SLIM cells were to originate from a single source. But even when each cell is driven independently, ensuring the flat-top character of the pulses is a challenge.

We note that because of the characteristic short pulse lengths the SLIM concept is amenable to further refinements to the control of longitudinal motion in circular hadron machines. For example, a part of the superbunch, which tends to promote synchrotron instability (for whatever reason) could be affected either by adjusting the charging cell voltage or by adjusting synchronization within a subset of individual cells. The ability of

this concept to work in the megahertz range is demonstrated on the setup shown in Figure 19.

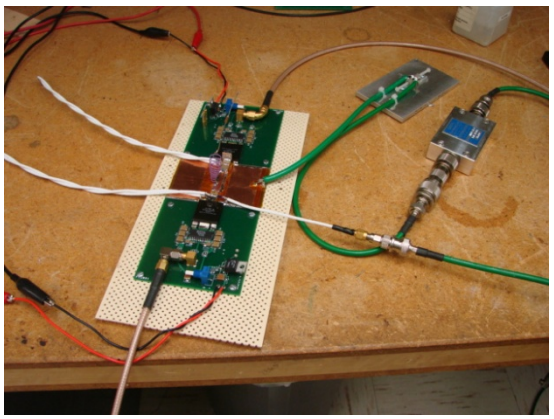

Fig. 19 Experimental setup

Two DE475-102 MOSFETs are used as the primary switches. The other components are similar to the components of previous setup. The upper waveform shown in Figure 20 is the voltage on the primary inductance (top waveform); the 3 MHz trigger sequence is below.

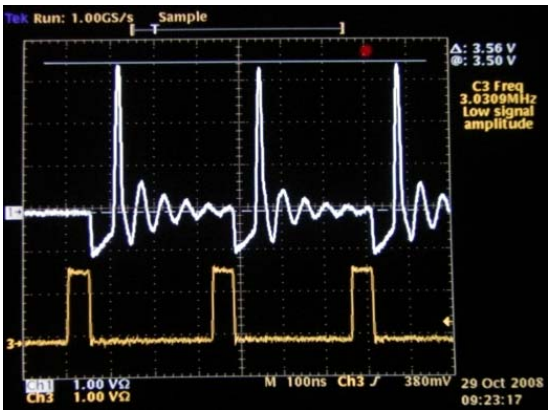

Fig. 20 Demonstration of operation at a 3 MHz repetition rate

The 3 MHz output train of nanosecond pulses is presented in Figure 21a. An individual pulse in this train is shown in Figure 21b.

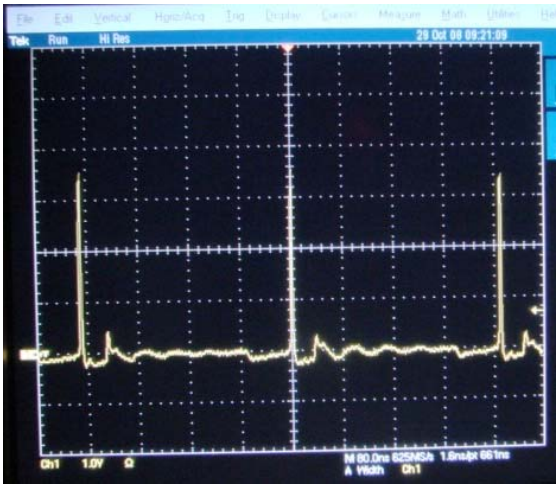

Fig. 21a Output of 3 MHz nanosecond pulse train (80 nsec/div)

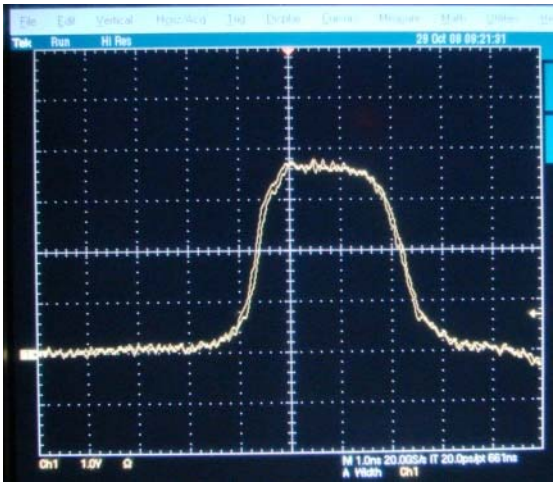

Fig. 21b Waveform of the nsec pulse (1 nsec/div)

Conclusion

The working principles of DSRD-based pulse compression circuits have been introduced. The integration of such circuits into coreless induction cells for high-gradient acceleration of charged particle beams - the SLIM concept - has been proposed and relevant

experimental results presented. The focus herein has been upon applying the SLIM concept to hadron programs, both linear and circular but other programs such as FEL, FEM, etc. might also benefit from this technology.

The proposed SLIM high-gradient acceleration approach depends on the availability of an extremely fast and compact switch. Ideally, the normal state of this switch would be ON such that the switch only experiences voltage stress during a small OFF portion of the duty cycle. In contrast, normally OFF switches would support voltage stress during a substantial fraction of the duty cycle and, thus, would tend to fail in challenging environmental conditions such as heavy ionizing radiation, hard electromagnetic noise level, etc. We have shown the DSRD solid-state opening (OFF) switch satisfies these requirements.

Furthermore we have described circuits which employ the DSRD that function as pulse compressors suited to high-gradient acceleration of charged particle beams. Within these circuits magnetic energy - developed from economical and reliable low-voltage power supplies – is developed in tens of nanoseconds. Upon opening of the DSRD switch this energy is largely transferred to the charged particle beam within an interval of a few nanoseconds. An evaluation of the cell acceleration gradient shows that values up to 100 MeV per meter could be realized. A further benefit of this coreless SLIM approach is that it promises to work at pulse repetition rates in the MHz range.

We observe that both distinct trends for the modern induction accelerators: that of high-gradient and low rep-rate induction acceleration, and that of low-gradient and high rep-rate induction acceleration, could be satisfied by this SLIM approach.

Reference

[1] A. I. Pavlovskii, et. al., “Linear Accelerator with Radial Lines - LIA-30”, Beams 92, ed. By D. Mosher and G. Cooperstein, p. 273
[2] A. Krasnykh, “Analysis of Modulator Schemes for Nanosecond Induction Linacs”, in Proc. of the Meeting on Problems at Collective Method Acceleration, Dubna, 1982, p.136 (in Russian). See also SLAC-WP-078 (in English).
[3] G. Caporaso et. al., “High Gradient Induction Accelerator”, Proc. of PAC07, p.875, Albuquerque, New Mexico, USA
[4] I. Grekhov, et. al., “Power Drift Step Recovery Diode”, Solid State Electronics, v. 28, p. 597, 1985
[5] A. Krasnykh, et. al., “High Gradient Linear Collider”, Proc. of the 11th All Union Meeting on Charge Particle Accelerators, Dubna, 1989, v. 2, p.103 (in Russian).
[6] F.O. Arntz et. al., “A Kicker Driver Exploiting Drift Step Recovery Diodes for the International Linear Collider”, Proc. of 11th European Particle Accelerator Conference (EPAC 08), Magazzini del Cotone, Genoa, Italy, 23-27 Jun 2008
[7] http://www.barthelectronics.com/
[8] K. Takayama and J. Kishiro, “Induction synchrotron”, Nuclear Instruments and Methods in Physics Research A 451 (2000) 304-317
[9] K.R. Symon et al., “FFAG Particle Accelerator”, Phys. Rev., Vol.103-6, 1837-1859, 1956

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There are several schemes that have been used for the rectangular nanosecond pulse generation. In most common cases, the combination of transmission line with a turn ON switch is employed. The energy is stored in the electrostatic manner. During a storage time, the normal switch state is OFF. The switch and transmission line are stressed to hold off the voltage during a whole charging period. Three basic circuits are typically employed for the square-pulse generation with turn ON switch. They are Line-type scheme, Blumlinein scheme, and Zarem-Marshall-Hauser scheme. Ideal discharging circuits for these three schemes are shown in Fig. A-1 a), b), and c) accordingly.

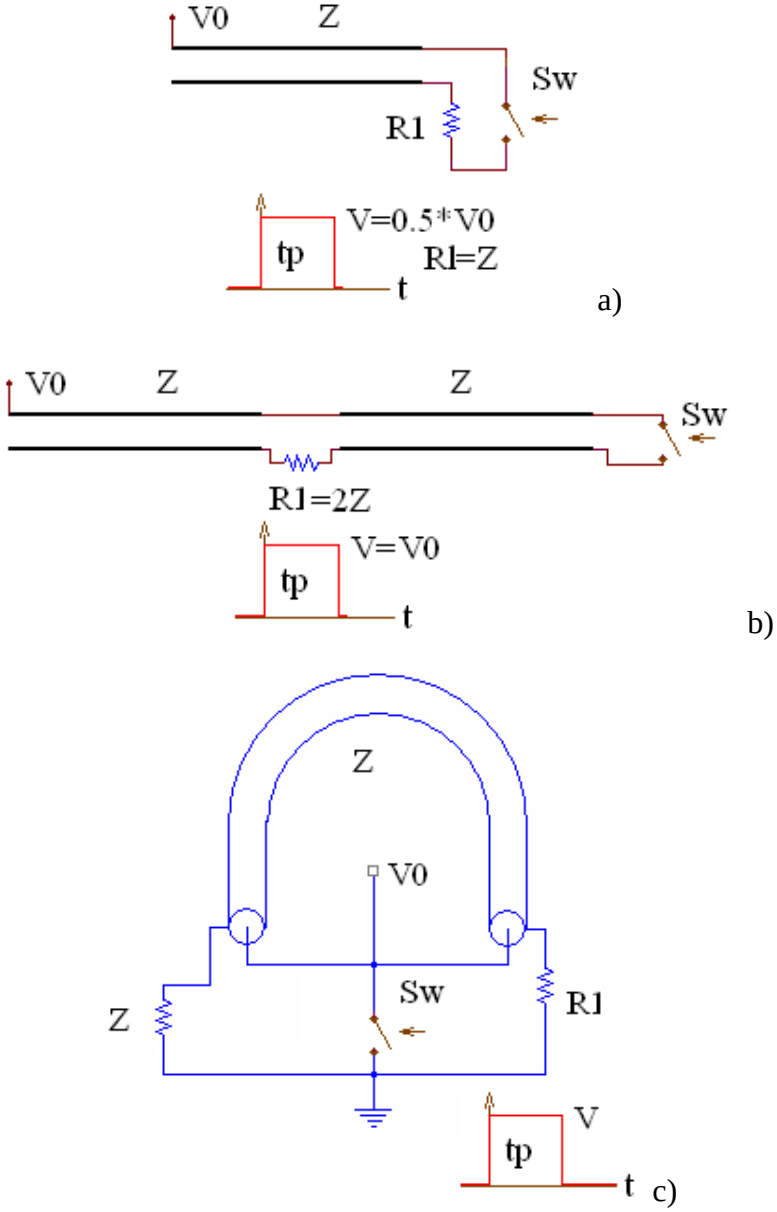

Fig. A-1 Simple diagrams of the discharging circuits for a square pulse formation on resistive load

A discharging circuit for line-type scheme generates a pulse width tp on the load Rl with an amplitude V that is half of charging voltage of transmission line Z. A discharge circuit for Blumlein scheme (with dual transmission lines) creates a pulse tp, the amplitude of

that is equal the charging voltage V=V0. However, the load impedance must be twice higher of the impedance of used transmission lines. The current through the switch is twice higher in compare with line-type scheme (if the rest parameters are the same). Both circuits generate a rectangular output pulse on the matching load with no after pulses. The third circuit creates a square-pulse on the mismatching load Rl with no after pulse. The output amplitude depends on the ratio between transmission line (Z) and load (Rl) impedances.

The discharge circuits shown in Figure A-1 a) and b) may be easily transformed for the case in which the turn OFF switch is used. The normal switch state is ON. The switch will stay ON for a magnetic energy storage period. The switch will be OFF only for short period of square-pulse generation. Transmission line and switch will be electrically stressed only for this short period. A circuit diagram for Line-type and Blumlein schemes based on OFF switch is shown in Fig.A-2 a) and b) accordingly.

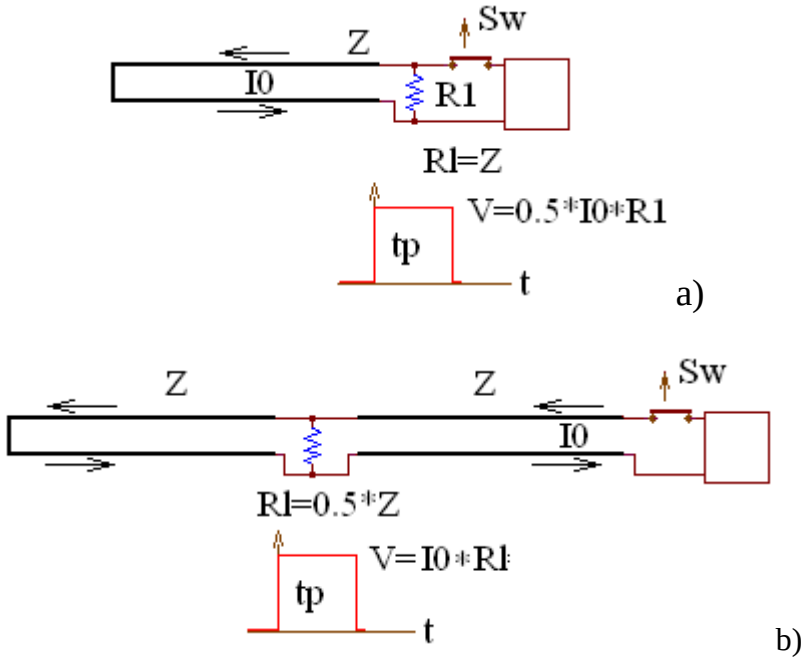

Fig. A-2 Simple diagrams of the circuits based on OFF switch for a square-pulse generation on resistive load

The load Rl will be shorted for a period of ON time. When the switch is OFF, the transient process is begun. During transient process, a rectangular pulse is created if the matching conditions are satisfied. Amplitude of the output pulse will correspond shown in Fig.A-2 equations. The load in these circuits is connected in parallel with transmission line. The load of the discharging circuits (Fig. A-1 b) is connected in series with transmission line. As a result, to satisfy the Blumlein condition for a circuit based on the OFF switch, the load impedance must be twice lower than transmission one. It is easy to show that the reflection on the load connection for both circuits shown in Fig. A-1 b) and Fig. A-2 b) will equal 0.5. A modification of the line-type circuit with OFF switch was used in scheme shown in Fig. 10. Both schemes suit for the SLIM concept.