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XAMPS Detectors Readout ASIC for LCLS

A. Dragone*, J.F. Pratte, P. Rehak, G. A. Carini, R. Herbst, P. O'Connor and D. P. Siddons

***Abstract*–An ASIC for the readout of signals from X-ray Active Matrix Pixel Sensor (XAMPS) detectors to be used at the Linac Coherent Light Source (LCLS) is presented. The X-ray Pump Probe (XPP) instrument, for which the ASIC has been designed, requires a large input dynamic range on the order of 10^4 photons at 8 keV with a resolution of half a photon FWHM. Due to the size of the pixel and the length of the readout line, large input capacitance is expected, leading to stringent requirement on the noise optimization. Furthermore, the large number of pixels needed for a good position resolution and the fixed LCLS beam period impose limitations on the time available for the single pixel readout. Considering the periodic nature of the LCLS beam, the ASIC developed for this application is a time-variant system providing low-noise charge integration, filtering and correlated double sampling. In order to cope with the large input dynamic range a charge pump scheme implementing a zero-balance measurement method has been introduced. It provides an on chip 3-bit coarse digital conversion of the integrated charge. The residual charge is sampled using correlated double sampling into analog memory and measured with the required resolution. The first 64 channel prototype of the ASIC has been fabricated in TSMC CMOS 0.25 µm technology. In this paper, the ASIC architecture and performances are presented.**

I. Introduction

hotons provide humans most of the information from the Penvironment. Thus it is not surprising that, also for research in natural sciences, photons provide the most important tools to study nature. Recent successes in the development of linear accelerators have opened the route to a new generation of X-ray photon sources, producing extremely bright ultrafast coherent laser-like X-rays pulses. The Linac Coherent Light Source (LCLS), under construction at SLAC National Accelerator Laboratory is one of these machines.

Among many new applications, this type of source provides a way to study stimulated changes in the structures of molecules and condensed matter systems. The LCLS instrument allowing this study is the so called X-ray Pump Probe (XPP) instrument in which the ultra-short (100fs at 120Hz) LCLS pulses will be used to probe the transient state of matter excited by a fast optical laser [1]. Depending on the experiment, X-ray absorption and emission or X-ray scattering will be recorded. X-ray scattering or diffraction requires a 2D integrating detector. Typical requirements for this instrument include input dynamic ranges for both the sensor and thus the electronics on the order of 10^4 photons (8keV) to be acquired with a resolution of half a photon FWHM. This leads to large capacitance pixels making the required noise levels very challenging to achieve. Furthermore the required detector area and the pixel pitch needed for a good position resolution impose limitations on the time available for readout.

A new generation of X-ray Active Matrix Pixel Sensors (XAMPS) specifically targeted for X-rays applications is under development at Brookhaven National Laboratory and will be used as the sensing element for this detector.

This paper introduces a new charge integrating readout Application Specific Integrated Circuit (ASIC) architecture designed to cope with XAMPS and to satisfy the stringent requirements in terms of input dynamic range, noise and timings of the XPP instrument. Due to the periodic structure of the LCLS beam, the ASIC is design according to a time-variant approach to maximize the readout speed. It provides low-noise charge integration [2], real time adaptive filtering and correlated double sampling. In order to cope with the large input dynamic range a charge pump scheme implementing a zero-balance measurement method has been introduced. It provides an on chip 3-bit coarse amplitude digital conversion and thus it allows a measurement of the residuals with the required resolution. The residual conversion is performed with an external 14-bit ADC. After a description of the XAMPS, the detector system, the ASIC architecture will be discussed in section III and IV. The charge pump approach will be described in section V. The first prototype of the ASIC has 64 channels, and has been fabricated in TSMC CMOS 0.25 µm technology. The ASIC characterization and the experimental results of this first prototype are reported in section VI.

II. XAMPS

XAMPS, originally conceived for protein crystallography, is a position sensitive ionization detector made on high resistivity silicon [3]. It consists of a pixel array detector with integrated FET switches (fig. 1).

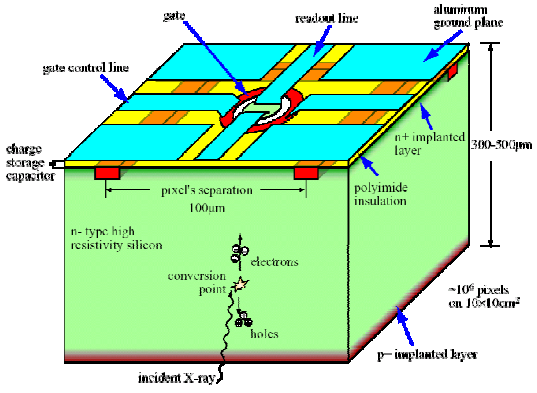

Fig. 1. XAMPS pixel structure and principle of operation.

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A. Dragone* and R. Herbst are with the SLAC National Accelerator Center, Menlo Park, CA 94025 USA (* corresponding author, telephone: 650-926-2613, e-mail: dragone@slac.stanford.edu).

J.F. Pratte, P. Rehak, and P. O'Connor are with the Instrumentation Division, Brookhaven National Laboratory, Upton, NY, USA.

G. Carini and D. P. Siddons are with the National Synchrotron Light Source, Brookhaven National Laboratory, Upton, NY, USA.

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Pixels are isolated from each other by potential barriers. The device is fully depleted by applying a high negative voltage to the junction on the entrance window of the device. When a photon is absorbed, the generated carriers drift to the exit side of the device and are collected by an implant, which is the floating electrode of the pixel or the source of the FET. Thus, this region, which occupies most of the pixel area, together with the isolated metal layer on its top form the capacitor in which the charge is stored. During this phase the voltage of the gate keeps the transistor in a high resistance state. The charge flows to the drain, connected to readout lines, when the gate voltage switches the transistor to low resistance. A deep implant prevents any charge from flowing directly from the bulk to the drain.

Pixels are arranged in a matrix fashion. The drains of the switches associated to the pixels in a column are connected to the same readout line, while the gates (named transfer gates) of those associated to the pixels in a row are activated simultaneously. This scheme allows a parallel readout of all the pixels in the same row. The full frame can be read out by cycling through the rows.

XAMPS of 1024 x 1024 pixels with pitches of 60 µm and 90 µm are in production for this instrument [3,4].

III. The Detector System

A block diagram of the final detector system is reported in Fig. 2. Each column of the sensor is read out by a dedicated electronic channel arranged as 16 ASICs of 64 channels each.

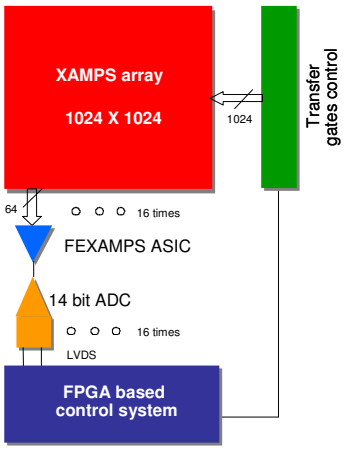

Fig. 2. Detector system block diagram.

Discrete external 14 bit commercial ADCs are used to convert the output analog signals. The acquisition is controlled by an FPGA that maintains the synchronization between the LCLS beam and the selection of the rows to be readout. Considering the repetition rate of the LCLS beam (120Hz) a frame has to be readout in 8 ms which, because of the parallel row readout of the XAMPS, turns into a readout slot time of not more than 8 µs per row i.e. per pixel of a specific readout channel. Multiple frame readout per pulse is desirable to perform more sophisticated corrections, but it imposes additional timing constrains.

IV. ASIC Architecture

Fig. 3 presents a simplified block diagram of the ASIC.

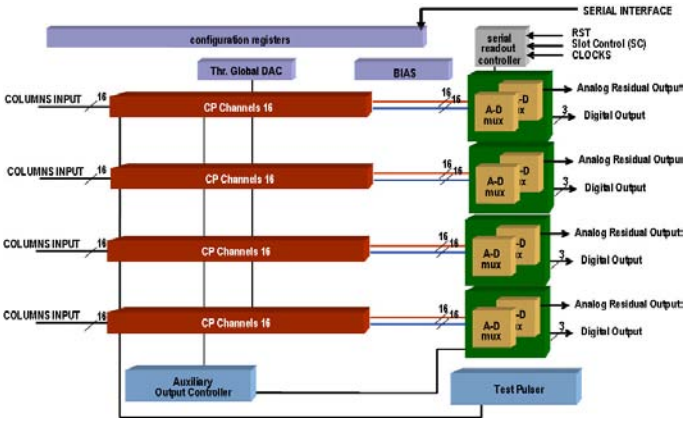

Fig. 3. Simplified block diagram of the 64-channels ASIC.

The 64 channels of the ASIC are arranged in 4 groups of 16; each one connected to its own analog and digital multiplexers and dedicated outputs. The 4 blocks are read out in parallel to speed up the readout procedure. The acquisition is controlled by a single periodic signal (SC slot control) whose period defines the readout time slot. This signal is synchronized to the LCLS beam trigger. During the active part of the SC period the charge is read out from the pixels and sampled. During the inactive period stored data are readout and the system is reset.

Each channel (fig. 4) implements a low noise charge integrator with a programmable double polarity pulsed reset, a 2nd order non inverting programmable LP filter, two double correlated double samplers and a discriminating charge pump circuit.

The low noise preamplifier integrates the input charge into a feedback capacitor. It is implemented according to a straight cascode configuration with gain boosting. To minimize flicker noise impact, the input device is a PMOS biased at 200 µA. Its size (W= 1.5mm L=0.24µm) is optimized for a 15pF input capacitance and for noise levels within the 500e- r.m.s. required by the instrument.

The pulsed reset system is able to set the DC output point of the amplifier either to the same value of the input (about 2V) close to the upper rail or close to the lower rail (about 0.5V) allowing the possibility to integrate charge of both polarities, accommodating the two different classes of XAMPS detectors under development. To increase the output dynamic range and to minimize non-linearity effects in the preamplifier response, an output stage using zero-threshold MOSFETs has been implemented.

The 2nd order LP filter is designed according to a Sallen-Key non inverting topology and makes use of a rail-to-rail differential amplifier with constant transconductance.

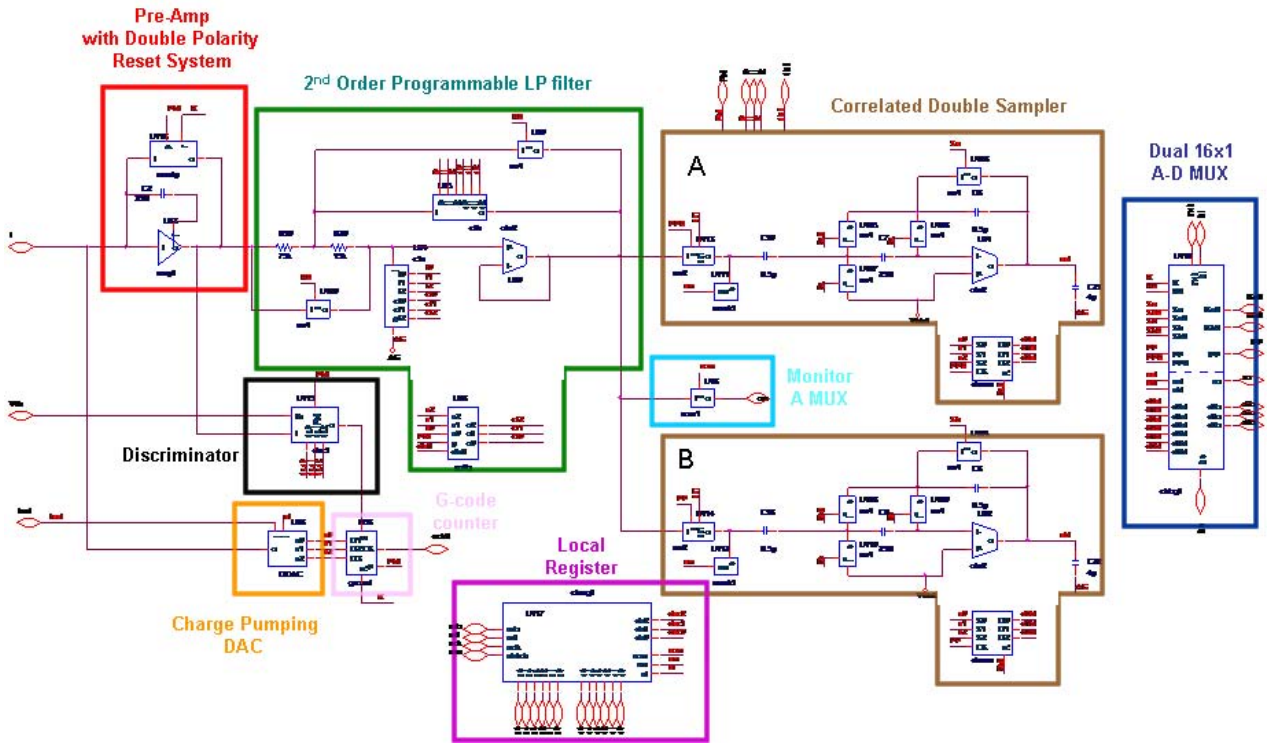

Fig. 4. Block diagram of a single ASIC channel.

The filter has two coincident real poles with programmable time constant. Since the application requires the readout of a pixel within a given time slot, the time constant value has to be set such that the response of the filter reaches a flat top within a fraction of the slot. Eight values of time constant are implemented resulting in readout timing slots from 1 µs to 8 µs in 1 µs steps.

The two correlated double samplers (CDS) are used to sample and store the filter output, purged from the fluctuations introduced by KTC noise, low frequency noise, baseline fluctuations [2,5] and CDS amplifier offset. They work in an alternate way to allow simultaneous read-write of the same channel. While a sampler holds the previous event and presents it to the active one of two analog multiplexer for readout, the other sampler is ready to process the next event. According to this architecture a "quasi-trapezoidal" noise weighting function can be implemented [2]. Fig. 5 shows the shape of the function extracted from the full channel simulation.

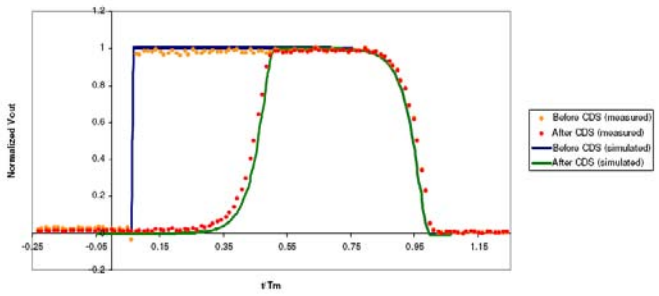

Fig. 5. Simulated and Measured Noise Weighting Function normalized to the readout time slot.

As shown in the figure, without performing the CDS a very steep leading edge in the weighting function is present. As know from the noise weighting function theory [2,6,7], this effect leads to a large series noise (a factor 2 difference in the series noise ENC has been calculated with and without CDS). The slope of this leading edge is related to the reset system time constant and to the fact that the reset system might split series noise doublets at the input. To avoid such effect either a slow reset is required or a correlated double sampling scheme. We preferred to implement the second for the additional advantages of the CDS technique mentioned before.

To cope with the large required input dynamic range of 10^4 photons at 8keV (about 3.5pC of charge) a charge pump system, described in the next section, is included in the channel. For input signal within 1/8 of the full dynamic range (about 0.44pC) the charge pump system remains inactive. For larger signals quanta of charge are subtracted from the input node until a residual smaller then the 1/8 of the dynamic range is stored in the preamplifier feedback capacitance, according to the scheme introduced in the next section.

Common to all channels are a number of 16:1 multiplexers for monitoring and readout. An automatic calibration system featuring an internal pulse generator is implemented with a 10-bit DAC for the injection of calibration signals and a 10-bit counter. Another 10-bit DAC is used for the global charge pump threshold setting, with each channel implementing 3-bit trimming for equalization. The logic for the acquisition, readout, and configuration is also common to all channels.

By making use of some innovative analog circuit solutions the ASIC is expected to provide the required resolution of 0.5

photons FWHM in the dynamic range of 10^4 photons at 8keV with a total dissipated power below 3mW per channel.

V. The Charge Pump Approach

To cope with the large input dynamic range a zero-balance measurement method has been implemented [8-10]. The preamplifier feedback capacitance is sized to hold 1/8 of the full input dynamic range without saturating the preamplifier.

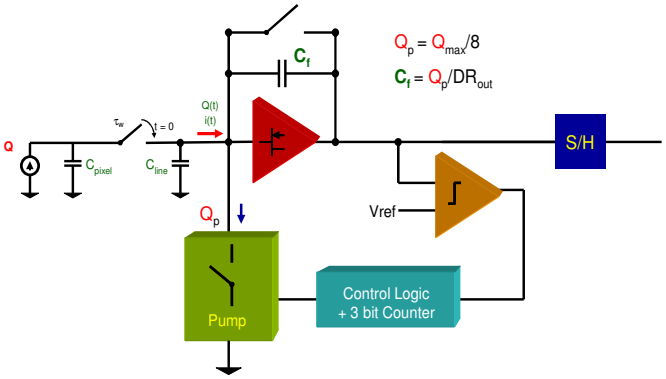

Fig. 6. Charge pump principle of operation.

If larger signals arrive the preamplifier moves toward saturation and the additional charge remains stored in the input node capacitance. The charge pump approach makes use of a charge pump connected to the input node controlled by a 3-bit counter. As soon as the saturation condition is approached a threshold discriminator enables the counter (driven by a periodic clock at 25 MHz). Every increment in the counter removes a 1/8 full dynamic quantum of charge from the input node until the output of the preamplifier returns above threshold. At this point the residual signal stored in the feedback capacitor is converted through the chain described in the previous section. The value stored in the 3-bit counter is equivalent to a coarse digital conversion and represents the MSB of the amplitude digitization. It is readout together with the residual which is digitized with an external 14-bit ADC. The pump is designed using 7 capacitors connected together to the input node on one side and, by means of switches, to two external reference voltages (analog ground and a dedicated 2.5V supply) on the other side. A single capacitor is switched for each increment of the counter. The external reference voltage can be adjusted allowing the tuning of the size of the charge quanta. The kTC noise contribution of such a reference is estimated to be up to 30 e^- r.m.s. using standard external voltage regulators, thus it is negligible with respect to the required noise levels.

As an example, a post layout simulation of the charge pump behavior in response to 2 subsequent full dynamic input pulses of charge (worst case) saturating the preamplifier is reported in fig. 7.

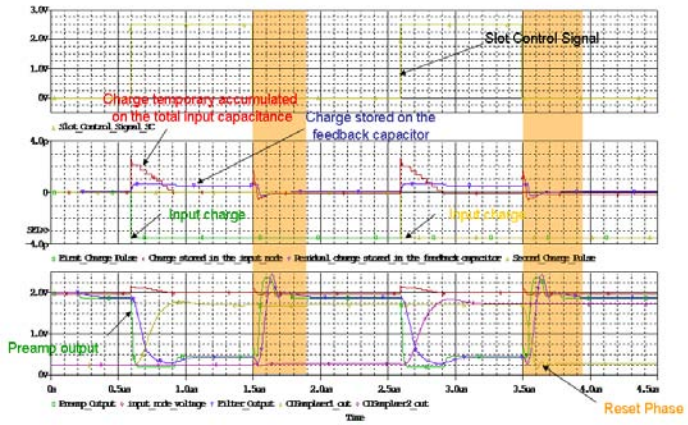

Fig. 7. Post layout simulation of the charge pump behavior for 2 subsequent full dynamic input pulses.

VI. First Results from the Prototype

The first ASIC prototype, built to prove the architecture concepts and test its performance before a first release, has been fabricated in TSMC CMOS 0.25 µm technology (Fig. 8).

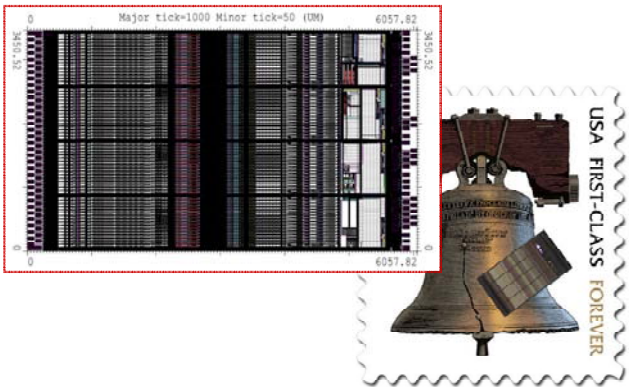

Fig. 8. ASIC layout and dimension.

It has a size of 6 mm × 3.45 mm and a power dissipation of 3mW/ch. The implemented features are fully working. Although minor issues are present, which prevent it from fully meeting the specifications for the XPP instrument, the prototype can be used in a first detector prototype together with a 64x64 XAMPS. Two different test systems have been built: one accommodating only the ASIC and another one with both the sensor and the ASIC. In the following, some test results performed on the ASIC alone will be presented, while test results on the detector system will be presented in [4].

A. Channel analog response at the output of the filter

This first set of measurements was aimed at testing the analog response of the first section of the ASIC channel, including the preamplifier with the reset system, the filter and the charge pump. Fig. 9 shows the analog voltage waveform, measured at the output of the filter of a channel by means of the on chip monitor multiplexer. A single period of the Slot Control (SC) signal i.e. the readout time per row is shown. In

this test the ASIC is configured for collecting holes, so from the baseline of 2 V the output of the signal swings down as soon as the active part of the SC period begins in sync with the charge injection at the input. When SC goes low again the reset system restores the baseline.

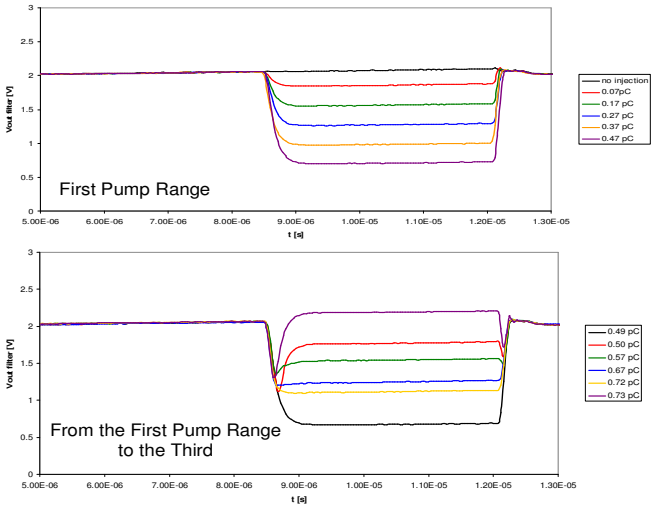

Fig. 9. Analog voltage waveform, measured at the output of the filter.

The top plot shows different waveforms within the first range of the charge pump. When the injected charge is instead higher than about 0.49pC (bottom plot) the pump is activated removing a quantum of charge from the input and leaving the residual in the feedback capacitor. The residual is proportional to the voltage level reported in the bottom plot.

B. Residual analog output as a function of the input charge

This second set of measurements was designed to test the full channel response as a function of the input charge pulse amplitude. Fig. 10 shows the fitted transfer characteristic at the output of the chip.

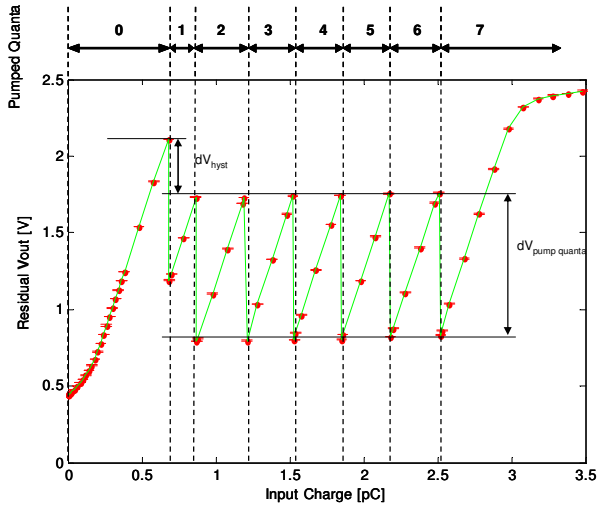

Fig. 10. Fitted transfer characteristic at the output of the chip.

The residual voltage at the output of the filter of a channel, sampled by the correlated double samplers and presented at the output by the on chip analog multiplexer was recorded using an external 16-bit ADC. The corresponding pump counter value, presented at the output by the on chip digital multiplexer, was also recorded.

The curve confirms the correct behavior of the ASIC and proves the concept. The 8 ranges of the charge pump are fully working and a negligible dispersion in the quanta steps has been measured. At the same time it shows some of the limitations of this first prototype. In particular a non linearity greater than the desired 1% has been measured in the lower part of the input dynamic range (below 200 fC) preventing the prototype to reach single photon detection. The second issue concluded by this plot is related to the hysteresis in the comparator that activates the pump which is larger than expected. Such hysteresis is responsible for the vertical translation of the first pump transition with respect to the others. Although such an effect does not compromise the behavior of the chip it implies a reduced input dynamic range (linear up to 3pC instead of the desired 3.5pC) limiting the range to set the pump threshold and the charge quanta amplitude.

The causes of both this issues are well understood and the fixes have been implemented in the revision of the ASIC.

C. Noise measurements

The third set of measurements were intended to evaluate the noise performance of the prototype. The first test performed was related to the measurement of the system noise weighting function. Following the definition of such a function [7] a charge pulse was produced at the input of a channel and the analog output before and after the correlated double sampler was monitored. The sampled value at the measurement time (just before the end of the SC period) was recorded as a function of the delay between the charge injection and the sampling time. The measured values are reported in Fig. 5 together with the simulated weighting function. Curves are normalized to the measurement time and also in amplitude. The good matching between simulated and measured curves shows the good performances of the filter.

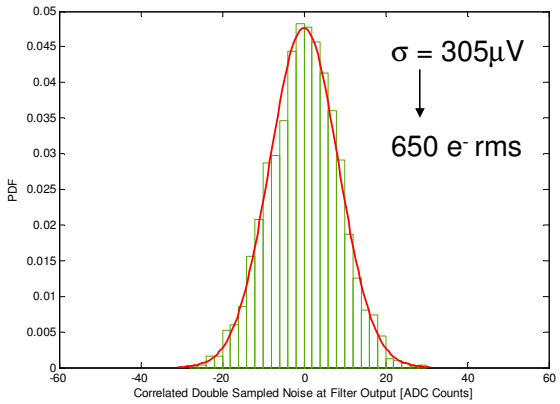

Fig. 11. Probability Density Functions in terms of ADC counts (16-bits) extracted from the measurements at the output of the filter performing a software correlated double sampling filtering.

The second test was to measure the noise level at the output of the filter performing a software correlated double sampling filtering. Figure 11 shows the Probability Density Functions (PDF) in terms of ADC counts (16-bits) extracted from the measurements with a filter time to the flat top of 4 μs.

The measured sigma on this histogram is very close to the 500e^- r.m.s. specified for the instrument. Further investigations are required to complete the noise tests on the back-end section of the ASIC. Preliminary tests do not show any significant contributions related to cross-talk between adjacent channels or noise induced by the on chip clocks.

VII. Conclusions

An ASIC dedicated to the readout of X-ray Active Matrix Pixel Sensors to be used in the X-ray Pump Probe instrument at LCLS has been designed and fabricated. It implements a charge integrating time-variant architecture operating synchronously with the LCLS beam structure. To cover the large input dynamic range of 10^4 photons at 8kV, a charge pump architecture has been successfully implemented. The first prototype has been fabricated in TSMC 0.25 μm technology and is currently under test. Some test results have been presented, proving the feasibility of the architecture. Minor issues have been found and understood.

In parallel with the completion of the tests, the design of the revision to be submitted on the beginning of 2009 is in progress.

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