December 2008
SLAC-PUB-13462

KPiX, An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information.

D. Freytag, R. Herbst, J. Brau, M. Breidenbach, R. Frey, G. Haller, B. Holbrook, R. Lander, T. Nelson, V. Radeka, D. Strom, M. Tripathi

***Abstract*–The Silicon Detector proposed for the International Linear Collider (ILC) requires electronic read-out that can be tightly coupled to the silicon detectors envisioned for the tracker and the electromagnetic calorimeter. The KPiX is a 1024-channel read-out chip that bump-bonds to the detector and communicates through a few digital signals, power, and detector bias. The KPiX front-end is a low-noise dual-range charge-amplifier with a dynamic range of 17 bit, achieved by autonomous switching of the feedback capacitor. The device takes advantage of the ILC duty cycle of 1 ms trains at 5 Hz rate by lowering the supply current after the data acquisition cycle for an average power consumption of <20 μW/channel. During the 1 ms train, up to four events exceeding a programmable threshold can be stored, the amplitude as a voltage on a capacitor for subsequent digitization, the event time in digital format. The chip can be configured for other than ILC applications.**

I. Introduction

KPiX is a multi-channel system-on-chip, for self triggered detection and processing of low level charge signals. The chip generates digital amplitude- and time-information for each signal above a selectable trigger threshold. The project was motivated by the requirements of the Silicon Detector (SiD) for the International Linear Collider (ILC). However, there is flexibility to make the device suitable for other applications as well.

The specifications for KPiX are driven by the requirements of the silicon-tungsten calorimeter and those for the silicon tracker system planned for ILC. The chip is to be bump-bonded, either to a 1000-channel silicon pixel detector in the electromagnetic calorimeter, or (two chips) to a 2000 channel silicon strip detector for the tracker system. This eliminates a costly cable plant for the detector signals, and minimizes the occupied volume and extraneous materials. Only two control signals (reset and command) are needed, in addition to the system clock, to configure the chip to autonomously control the acquisition and read-out of data.

In order to achieve low power consumption (<20 μW/channel) for ILC applications, the chip runs at full power only during the beam period (~1 ms), at reduced power during the 2 ms digitization cycle and with only the residual CMOS power draw during data read-out and idle time (197 ms). The power pulsing is achieved by pulsing down currents by a factor ~100 while keeping the full supply voltage. This avoids power loss due to recharging of filter capacitors and it achieves fast power-up times of a few tens of microseconds

TABLE I
SPECIFICATIONS

Noise Floor	0.15 fC, (1000 el.)
Peak Signal (Dual Range)	10 pC
Range Switching	Selectable, ~400 fC
Trigger Threshold (normal)	Selectable, 0.1 to 10 fC
Calibrator	Full Scale, two Ranges
Buffer Depth	Four each Pixel

II. Digital Section

The digital section comprises a block which controls the operation of the full chip, and an array of digital blocks which reside in each pixel cell.

The common block comprises a state machine sending out the required sequences of control signals, first to acquire and store the necessary configuration data into registers, then, for each data cycle, to send out the control signals necessary for data acquisition. This block also contains ten Digital-to-Analog Converters with 8-bit step size, but approximately 12 bit precision of each step, covering the full range between the power rails.

The digital section residing in each pixel cell contains a timing generator, running off the system clock and started for each trigger, controlling the acquisition of the analog data. Further there is an event counter and nine words of 13-bit memory.

Ten DAC levels control threshold and calibration amplitudes and sixteen register-bits control various options in the operation of KPiX.

III. Processing of Charge Signals

Up to four sequential signals can be handled in each pixel during one data cycle. The operations needed for the

Manuscript received November 14, 2008. This work was supported by the U.S. Department of Energy contract No. DE-AC02-76SF00515 (SLAC-PUB-13462)

D. Freytag, SLAC National Accelerator Laboratory, Menlo Park, Ca. USA (telephone: 650-926-2785, e-mail: drf@slac.stanford.edu).
R. Herbst, M. Breidenbach, G. Haller, T. Nelson SLAC-NAL
J. Brau, R. Frey, D. Strom, University of Oregon, USA
B. Holbrook, R. Lander, M. Tripathi, UC Davis, USA
V. Radeka, Brookhaven National Laboratory, USA

Presented at the 2008 IEEE, 10/19/2008 to 10/25/2008, Dresden Germany

acquisition are broken up into three functional blocks: the Charge Amplifier (fig.1), the Acquisition Block (fig. 2), and ADC with Memory (fig. 3). The input charge is picked up by the charge sensitive amplifier and stored in the default feedback capacitor (fig. 1). If the default range is exceeded, a condition detected in the range threshold discriminator, a 10 pF capacitor is automatically added to the feedback to extend the range to 10 pC.

Two kinds of reset are provided, a digital reset, which is active during power-up and after each event, and a soft DC reset. For ILC operation, the digital reset can also be activated before each beam crossing. The DC reset, which can be activated by setting a register bit, is advantageous for non-bunched signals like cosmic rays or radioactive source data. Both kinds of reset are immediately inhibited on receipt of a trigger, to avoid compromising the stored data.

For DC-coupled signals, the leakage is compensated by a servo circuit. The amount of leakage is determined with no signal present and held during the signal period.

A precision calibrator sends up to four signals with amplitudes and timings as defined during the set-up cycle. An 8-bit DAC provides 256 calibration values, with each level defined to a precision of ~12 bit. Each cell has a calibration-mask-register to enable calibration in arbitrary combinations of cells. The first calibration pulse can be selected for a high calibration range, so that the system can be tested up to the full-scale range of 10 pC

For negative-polarity signals, an inverter is inserted after the charge amplifier. The polarity of the calibration signal is reversed too.

.

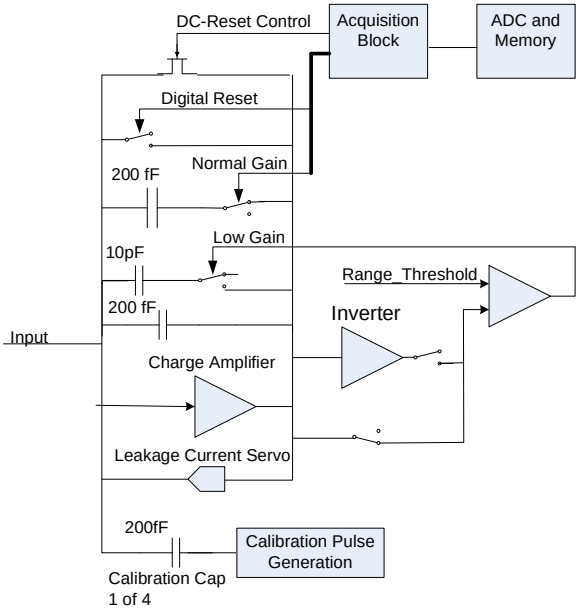

Fig. 1. Amplifier Block .

The charge-amplifier signal is amplified, shaped and sent to the trigger stage (fig. 2). For signals above the (selectable) trigger threshold, the digitally controlled acquisition cycle is started. After a wait period to allow for settling of the charge-amplifier signal and to synchronize with the system clock, the signal is acquired in one of four storage capacitors. The coupling elements form a low pass filter of 0.5 us time constant. After a programmable time interval, the signal is held in the sampling capacitor, and control is passed to the next sampling capacitor. The charge amplifier is reset and ready to accept the next signal after a period of trigger-inhibit has elapsed. Because the integration interval is precisely controlled, the stored amplitude is proportional to the signal, even if the asymptotic amplitude is not reached. A strobe signal is sent to the memory block to record event time.

To allow for non-uniform pixel response, a choice between two different trigger thresholds is available in each cell (not shown in fig. 2). There is also a high-low discrimination system (not shown) to catch the signal early for the trigger-inhibit, while latching the trigger only for the higher threshold.

For the tracker application, an option to carry the trigger over to the neighboring cells is provided, so that spill-over signals below trigger threshold can be picked up as well.

A common external trigger is provided for test-beam and other applications.

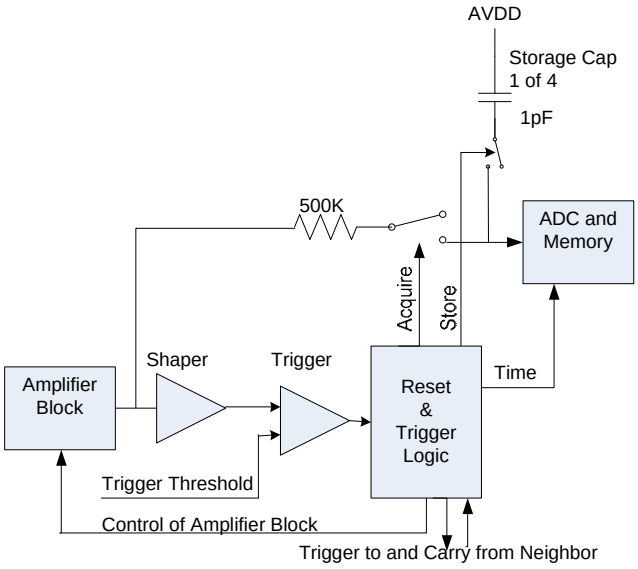

Fig. 2. Acquisition Block

In the ADC-and-Memory Block (fig. 3), the analog information previously stored in 4x1024 capacitors is digitized in four cycles, each for 1024 capacitors in parallel. The Wilkinson method is used for the conversion, with a current mirrored into each cell running down the charge in the storage capacitor. A ramp-threshold discriminator detects the transition through zero and causes the content of a common Gray counter to be stored in memory. The ADC has 13-bit resolution.

This method of digitization could proceed independently in each cell, offering the possibility of DC operation. The four buffers in each cell could be filled and read out on a rotating basis. This would require an upgrade of the digital core.

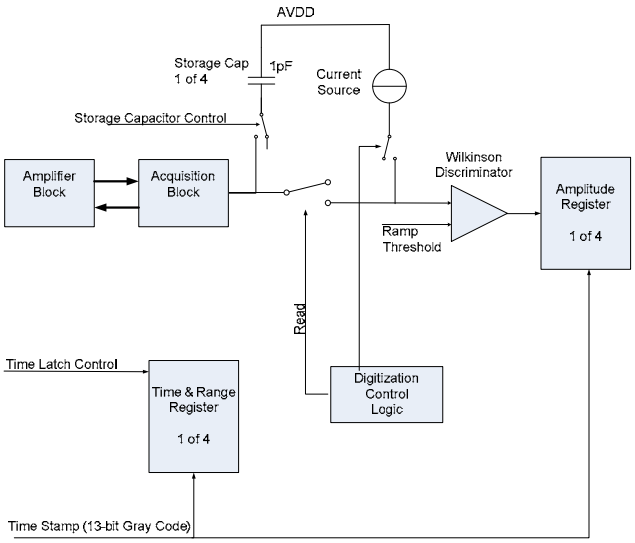

Fig. 3. ADC and Memory

IV. Measurements

A 64-channel prototype was fabricated in the TSMC CMOS 0.25 µm mixed-signal technology. Measurements performed on this prototype follow.

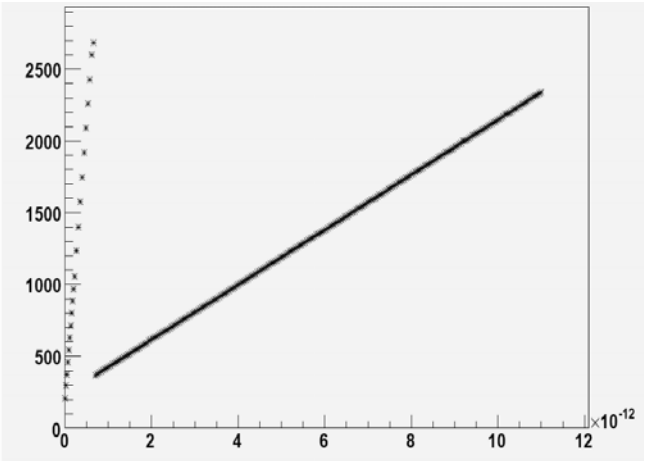

Fig. 4. Full-scale Calibration

Fig. 4 shows the result of a calibration run covering the full amplitude range of the amplifier by means of the high-calibration mode. The automatic range-switch takes place at ~0.5 fC, as determined by the range-threshold DAC. It is also possible to force low gain operation throughout, which is useful for some applications.

RMS values for the linear fits in the two branches are 1 fC for normal gain, 10 fC for low gain. From the rms value in normal gain obtained in the high-cal run one can deduce that the DAC steps are defined with 13-bit precision.

Fig. 5 shows the calibration of the normal-gain range using the normal-calibration mode. The rms-value of the fit is 1.9 ADC or 0.43 fC. The lower plot shows the residuals, indicating a very smooth characteristic of the calibration DAC, except for a small break at half scale due to the transition from n-type to p-type switches in the DAC. The rms value of the linear fit of 0.42 fC is close to the value of 0.15 fC determined by repeated measurements of the baseline.

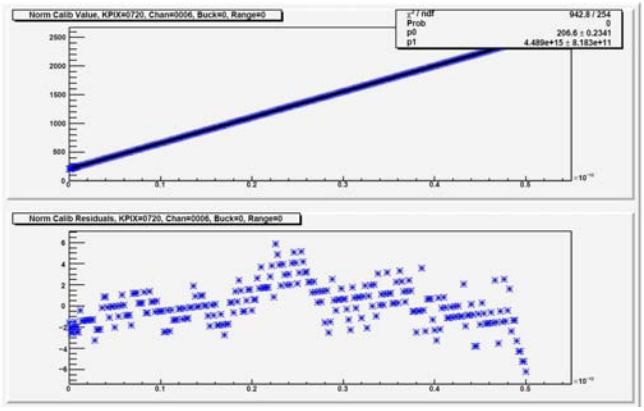

Fig. 5. Normal-range Calibration

Fig. 6 shows two histograms of noise in 64 cells set to double gain. In double-gain mode, a slightly improved noise performance is observed, because noise sources downstream of the charge amplifier enter with lower weight. The ADC noise is high-lighted, the noise in the trigger branch is the open histogram. The noise in the trigger branch is determined by recording the trigger rate as a function of threshold in each of 64 cells and fitting an error function to the data points. Nearly all cells are below the specification of 1000 electrons (0.15 fC).

All noise measurements were performed without an external capacitive load at the input. The noise slope due to a capacitive load was determined separately as 35 electrons/pF. This needs to be added in quadrature to the noise reported here.

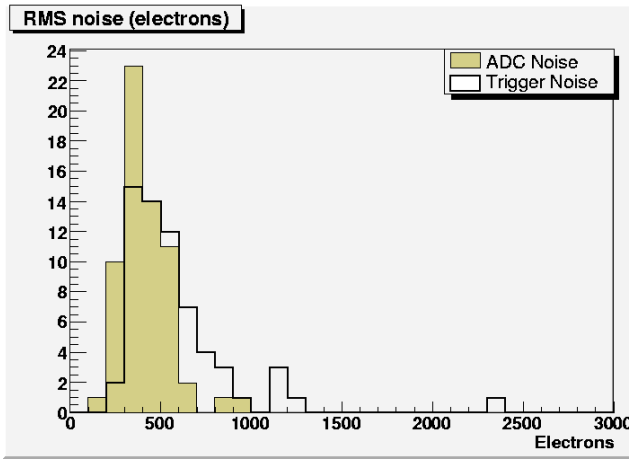

Fig. 6. Noise in Double Gain for 64 Cells

Fig. 7 shows data taken in a SLAC test beam of 10 GeV/c electrons for a group of three CDF sensors (128-channel devices) arranged in layers of vertically oriented strips. A synchronous signal 1 ms before the beam pulse was used to power up KPiX. An external trigger at the correct beam time served as a common data strobe.

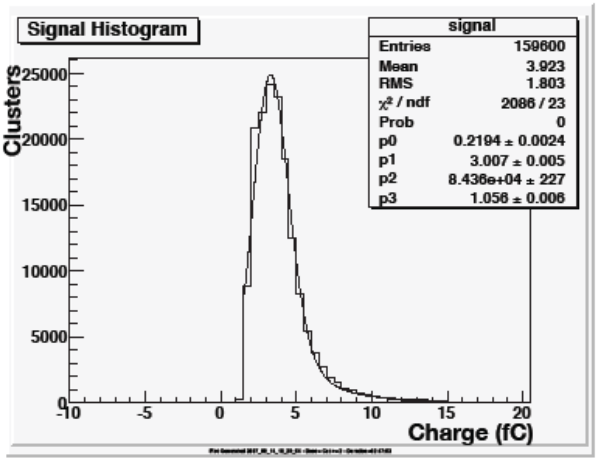

Fig. 7. CDF Tracker Chips in SLAC Test Beam and KPiX

Plotted are double-coincidence clusters of strips and the fitted curve is a Landau distribution convoluted with a Gaussian for the noise.

Fig. 8 shows data (obtained by H. Band of the University of Wisconsin) with cosmic rays into a Resistive Plate Chamber running in avalanche mode. Additional RPC's were used to generate an external trigger for KPiX. The data peak at 3 pC and the spike near zero is attributed to tracks missing the RPC.

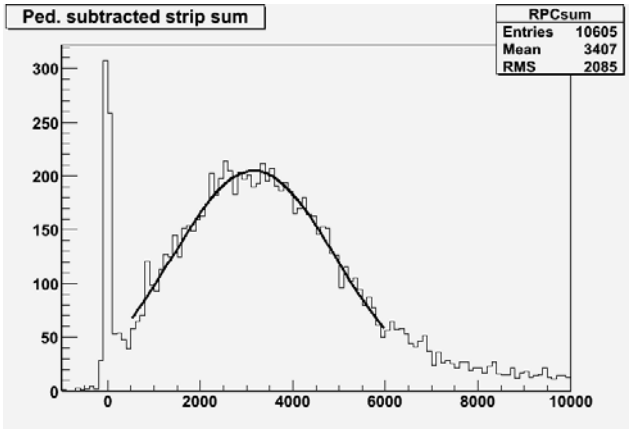

Fig. 8. Resistive Plate Chamber in Avalanche Mode, Cosmic Rays

A separate run for background (fig. 9) shows a distribution with a sigma of 29 fC, while the expected noise is less than 10 fC. The difference may be due to pick-up.

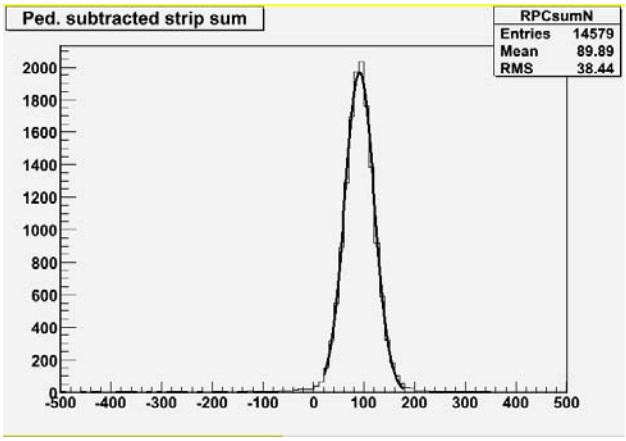

Fig. 9. Background Signals in Resistive Plate Chamber

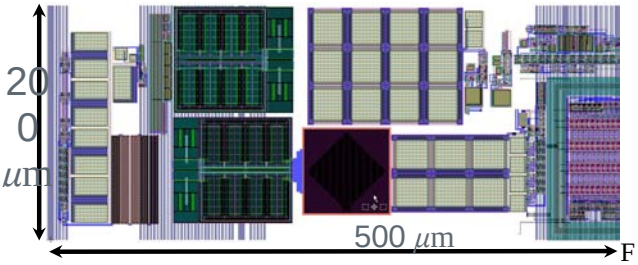

Fig. 10. A Single Pixel Cell of KPiX, Dimensions 500 μm x 200 μm

Fig. 10 shows the lay-out of a single cell of KPiX. Two adjacent cells will be mirror images so that digital and analog circuitry is well separated by diffusion barriers.

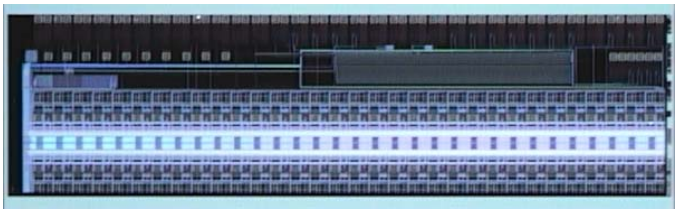

Fig. 11. A 64-channels Version. Dimensions 7 mm x 1.8 mm

Fig. 11 shows the layout for a 64-cell device. More rows will be added at the bottom to generate a 1024-cell device of dimension 7 mm x 17.8 mm.

V. SUMMARY

A 64-channel prototype of the projected 1024-channel device has been tested and found to meet specifications. A number of new features have been added to the original design to make it useful for other than ILC applications. Tests with chips bump-bonded to calorimeter- and tracker-sensors are in progress, as well as experimental studies with Resistive Plate Chambers (RPC) and Gas Electron Multiplication Chambers (GEM). The transition to the full sized chip is planned in two steps, 256 and then 1024 channels, mainly to save on prototype fabrication costs.