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Hybrid MOSFET/Driver for Ultra-Fast Switching

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***Abstract*- The ultra-fast switching of power MOSFETs, in ~1ns, is very challenging. This is largely due to the parasitic inductance that is intrinsic to commercial packages used for both MOSFETs and drivers. Parasitic gate and source inductance not only limit the voltage rise time on the MOSFET internal gate structure but can also cause the gate voltage to oscillate.**

This paper describes a hybrid approach that substantially reduces the parasitic inductance between the driver and MOSFET gate as well as between the MOSFET source and its external connection. A flip chip assembly is used to directly attach the die-form power MOSFET and driver on a PCB. The parasitic inductances are significantly reduced by eliminating bond wires and minimizing lead length. The experimental results demonstrate ultra-fast switching of the power MOSFET with excellent control of the gate-source voltage.

I. Introduction

Power MOSFETs have great potential as switches for high speed high voltage applications like pulsed power. The theoretical carrier transit time from drain to source is on the order of 200ps in any cell of the silicon die [1]. Although the MOSFET is intrinsically capable of ~1ns switching, the packaging inductance largely degrades the performance of the device. The major contributors are the parasitic gate inductance (Lg) and parasitic source inductance (Ls). At high frequency, Lg will present a large impedance that will isolate the driver from the gate electrode of the MOSFET die. High switching speed means high di/dt through MOSFET source and drain, which will create a large voltage drop across Ls. This voltage can be higher than the gate driver voltage and will eventually turn off the device. This negative feedback can drive the MOSFET into an oscillatory state. A damping resistor is normally inserted in series with the gate electrode to prevent such oscillations, however, this further impedes the transfer of charge to the gate.

Two methods are currently used to improve the switching speed of commercial power MOSFETs. One method is to use a specially designed package and die to minimize the parasitic inductances; the other is to integrate the driver and die into same package. IXYS RF uses the first method in their DEI-series MOSFET, and claims a very low parasitic inductance (~1nH). The second method is used by Microsemi, in their DRF100/DRF1200 MOSFET. But these devices are still limited to switching speeds of ~3 ns. One possible reason is the Al bonding wire, used in both devices to make the connection between the die and terminal, still introduces a significant source of parasitic inductance.

DCA (direct chip attachment) is now available as a common PCB assembly method. Among all the DCA methods[3], Flip-chip assembly is the most promising one since it is completed eliminated the use of bonding wires in our design. Here several hybrid boards are designed then assembled using this method to get a high speed MOSFET switch module.

II. Design

Three variations of circuit boards (PCB#1, PCB#2 and PCB#3) were made to accommodate different package and circuit configurations. All three boards share the same driving circuit, shown in Fig. 1. PCB#1 connects a single totem pole driver to either a DE275 or TO247-packaged power MOSFET. PCB#2 and PCB#3 connect two identical drivers, in parallel, to a die form power MOSFET. The difference is the totem pole driver of PCB#2 is in a SO8 package and in PCB#3 it is assembled from raw dies using the flip-chip method. Because of the limited availability of die form MOSFETs, the totem pole driver and input buffer of PCB#3 is slightly different than that used for PCB#2. Fig. 2 is a photo of the PCB#3. The power MOSFET is mounted on the bottom side of the board. The major specifications of the critical components are listed in Table I.

The circuits are composed of 4 function blocks; load, power MOSFET, totem pole driver and input buffer. The design and assembly of these blocks will be discussed separately in the following sections.

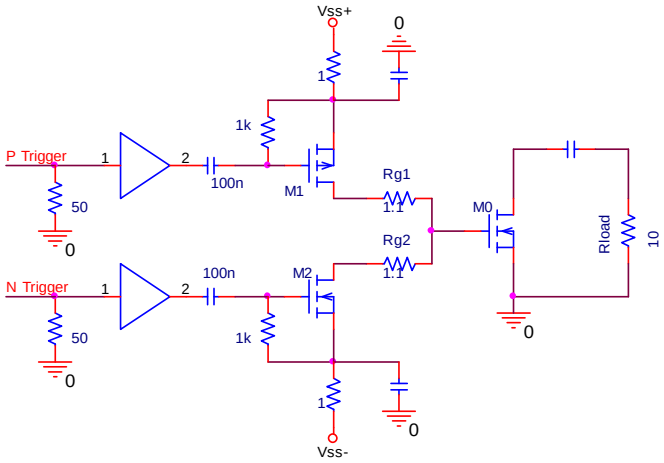

Fig. 1. Circuit diagram of the hybrid circuit

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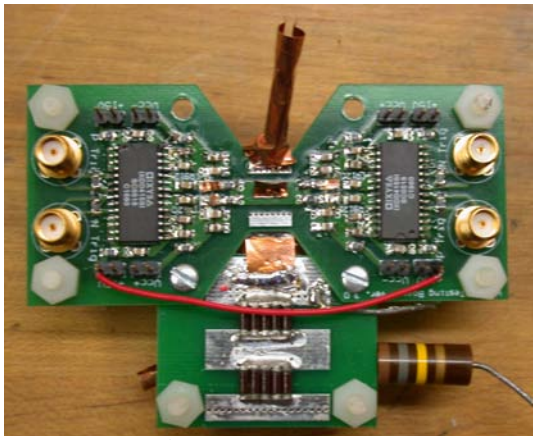

Fig. 2. A photo of the hybrid circuit. PCB#3 is shown here

TABLE I SPECIFICATIONS OF CRITICAL ELEMENTS

		PCB #1	PCB#2	PCB#3
Input Buffer	PN	EL7158		IXDD415SI
	Min PW	~8ns		6ns
	Iout	12A		15A
	Vcc	12V		30V
Totem Pole	PN	FDS4559		IRFC120/9120
	Vdss	60/-60 V		100/-100V
	Rds(on)	0.055/0.105 Ohm		0.21/0.48 Ohm
	Id	4.5/-3.5 A		9.4/-6.6A
	Qg	12.5/15 nC		25/27 nC
	Ciss	650/759 pF		330/350 pF
Power MOS FET	PN	DE275-102N06A	APT30M75BLL / APT30M75	APT1201R2
	Package	DE275	TO-247 / Die	Die
	Vdss	1000V	300 V	1200V
	Rds(on)	1.6 Ohm	0.075 Ohm	1.2 Ohm
	Id	8A	44A	12A
	Qg	50 nC	57 nC	100 nC
	Ciss	1800pF	3018 pF	2540 pF

A. *Load*

The load is a stand alone PCB which is used with all three boards. Five 1nF 1000V C0G capacitors and two 47nF 1000V X7R 1206 SMD capacitors are used as energy storage elements. And ten 27 ohm HSF-1 cylindrical thick film SMD resistors are connected in a 2 by 5 array as a 10.6 ohm resistive load. These resistors have no trim cut which minimizes the inductance and potential voltage enhancement on the trim edge. The load is connected to the power MOSFET using a 1cm wide copper foil.

B. *Power MOSFET*

The circuit performance is critically dependent on the layout of the power MOSFET section. It is designed to adapt the die form MOSFET to the board with a minimum of parasitic inductance.

A flip-chip assembly technique has been selected from the available DCA methods for its capability to minimizing packaging inductance. The gate and source terminals are all on the top side of the die and the metalized bottom is the drain terminal. First, solder bumpers are attached to the Al electrodes on the top side of the die. In order to reduce the inductance, as many bumpers as possible are used. Then the die is flipped and electrical contacts to the circuit board are made using conductive epoxy. Then, silver epoxy is applied on the bottom side of the die (now facing up), and a copper foil is attached to make the external drain connection.

C. *Totem Pole Driver*

The totem pole driving stage has two complimentary MOSFET. The PMOS is connected to the positive voltage source and will control the turn-on of the power MOSFET. While the NMOS is on the negative source and will control the turn-off of the power MOSFET. Two output resistors (Rg1 and Rg2) are used to give independent control of on/off switching and limit shoot through current.

A current source driver is used instead of the traditional voltage source driver. The key difference is that the driver voltage can now be higher than the maximum gate-source voltage of the power MOSFET. The current is set by the sum of the gate resistor value and the drive MOSFET on resistance. Since the totem pole switches, M1 and M2, will only conduct a very short period of time, the final voltage on the M0 gate, which is controlled by the on time of the driver, will be relatively small compare with the driver voltage. This driving scheme is selected based on the analysis of MOSFET switching processes[4]. From the analysis, the switching speed of the MOSFET does not depend on the final gate voltage but rather, the gate current at the start of conduction. Using a voltage source driving scheme, the maximum voltage is limited by the M0 gate breakdown voltage. This will reduce the maximum available current.

D. *Input Buffer*

A commercial integrated circuit MOSFET driver is used as the input buffer, which converts the TTL level trigger from the function generator to a higher voltage level suitable for MOSFET switching. An EL7158 driver is used for PCB#1 and PCB#2. An IXDD415SI is used in PCB#3 because it has a shorter minimum output pulse length, which makes it possible to used a higher driver voltage for totem pole stage.

The input buffer is capacitively isolated from the totem pole. This isolation provides level shifting, which facilitates the use of two voltage sources for the totem pole driver.

III. RESULTS

Fig. 3 shows the typical gate and output waveforms of the same power MOSFET, in a TO247 package and the hybrid assembly under the same drive condition. The waveform is measured using Tektronix TDS684C (1GHz BW, 5GS/s) with P6139A probe (500MHz BW). The merits of the hybrid circuit are clearly shown by these waveforms: 1. The turn on speed (Falling time) of the hybrid circuit is much faster than the packaged one. 2. The gate waveform of the hybrid board has much less oscillatory behavior than the packed one. 3. The switching delay, especially the turn off delay, is much smaller for the hybrid circuit. Closer examination of the turn on switching time shows more than a factor of 2 reduction (3.25±0.09ns/1.40±0.03ns) for the hybrid circuit. The

commercially available low inductance MOSFET (DE275-102N06A) was also test using this platform. Although it exhibited improved switching speed, compared to the T0247 device, the gate waveform is still exhibited oscillations, unlike the hybrid circuit. (Since there are large differences in the specifications of DE275-102N06A and APT30M75, the comparison of switching performance is very complex and not presented in this paper.)

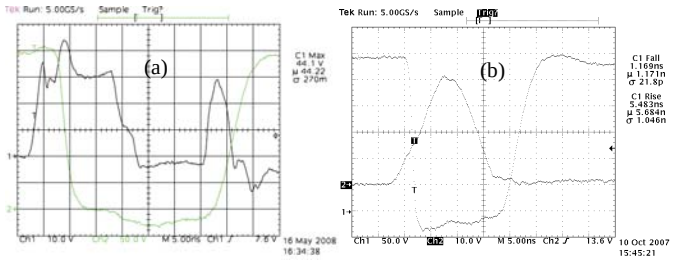

Fig. 3. Gate and Drain voltage waveforms of (a) TO247 package device(Gate:CH1, Drain:CH2) and (b) PCB#2 hybrid circuit (Gate:CH2, Drain:CH1)

The PCB#2 hybrid circuit can connect one or two parallel drivers to drive the power MOSFET gate. A series of experiments were performed using different gate resistance value and single or dual totem pole driver. Since the two drivers drive the power MOSFET in parallel, the effective Rg is 1/2 of the value for each driver. The results are shown in Fig. 4. This result suggests that the package inductance of the totem pole IC plays an important role in the total parasitic gate inductance[2] otherwise the speed should be the same for a single driver with Rg = 1.1 Ohm and a dual driver using 2 Ohm on each side.

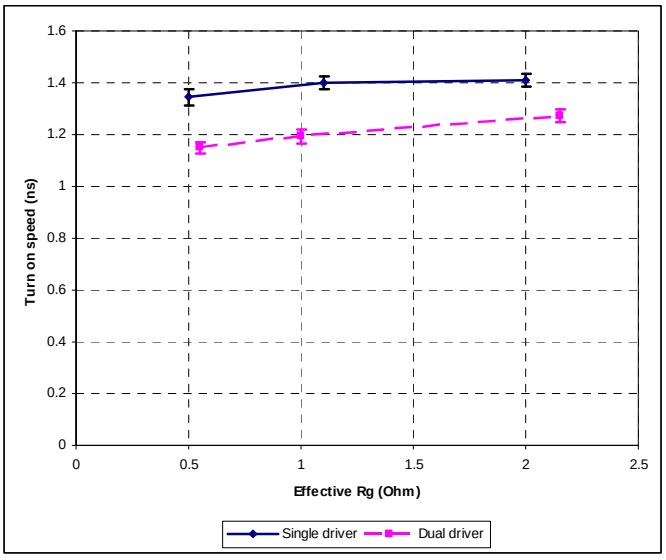

Fig. 4. Switching speed at different gate resistance

PCB#3 is designed to verify this explanation and improve the performance further. On PCB#3, the totem pole driver is also attached using flip-chip assembly to minimize the inductance. The initial experiments with PCB#3 using a single driver resulted in slightly better performance than the PCB#2 dual driver case, which suggests the explanation above is reasonable. Fig. 5 shows a switching waveform using PCB#3. Using parallel drivers, PCB#3 has a potential to switching even faster. The measurement of this switching is limited by the probe bandwidth. A custom high voltage high bandwidth attenuator is proposed for future investigation.

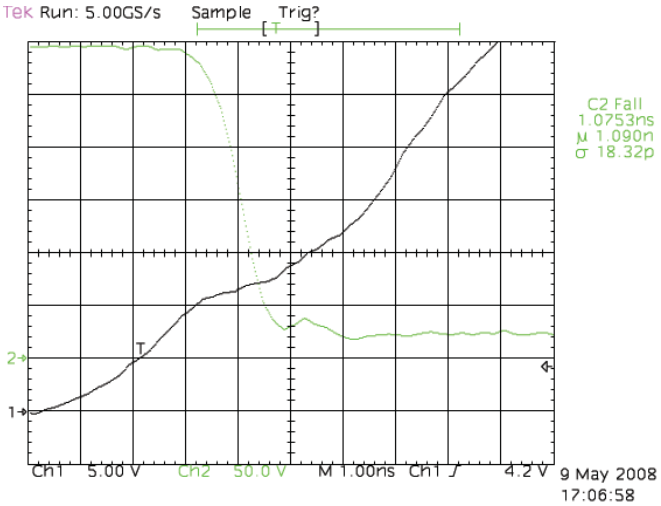

Fig. 5. Fast switching with hybrid circuit, CH1: Gate voltage, CH2: Drain voltage. Switching speed: 1.09±0.02ns. Charge voltage: 300V, Load 10 Ohm.

IV. Conclusion

A hybrid MOSFET/driver configuration is presented in this paper. The flip-chip assembly method is used to attach the power MOSFET and driver on a PCB. This direct chip attachment method largely reduced the package inductance and as a result a very clean gate waveform and ~2.3 time faster switching speed are achieved comparing with packaged devices. This hybrid topology has also demonstrated a switching speed of ~1 ns, switching 300V into 10 Ohm load, $dI/dt \sim 3\times10^{10}$ A/s.

Acknowledgment

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