THE FONT4 ILC INTRA-TRAIN BEAM-BASED DIGITAL FEEDBACK SYSTEM PROTOTYPE

P.N. Burrows, G. Christian, C. Clarke, B. Constance, H. Dabiri Khah, T. Hartin, C. Perry, C. Swinson, John Adams Institute, Oxford University, UK.
A. Kalinin, Daresbury Laboratory, UK; S. Molloy, G.R. White, SLAC, USA.

Abstract

We present the design of the FONT4 intra-train beam-based digital position feedback system prototype. The system incorporates a fast analogue beam position monitor front-end signal processor, a digital feedback board, and a fast kicker-driver amplifier. The system latency goal is less than 150ns. We report preliminary results of beam tests at the Accelerator Test Facility (ATF) at KEK using electron bunches separated by c. 150ns.

INTRODUCTION

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

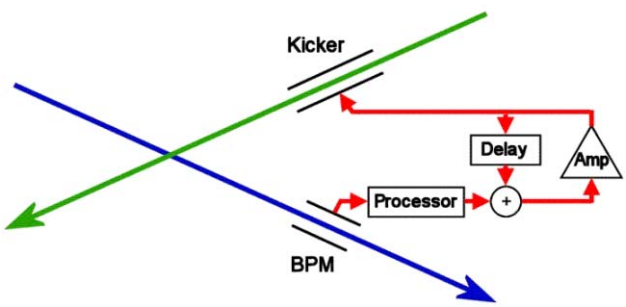

Figure 1: Schematic of IP intra-train feedback system for an interaction region with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the electron and positron beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm. Previously we have reported on all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for 'room temperature' Linear Collider designs with very short bunchtrains a few hundred nanoseconds in length, such as NLC [2], GLC [3] and CLIC [4]. We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [5], 54ns (FONT2) [6] and 23ns (FONT3) [7].

Here we report on the design, development and beam testing of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) device [8]. The use of a digital processor will allow for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is now possible for ILC given the long, multi-bunch train in the current design, which includes machine parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively. Initial results were reported previously [9].

FONT 4

A schematic of the FONT4 feedback system prototype and the experimental configuration in the ATF extraction beamline is shown in Figure 2. The layout is functionally equivalent to the ILC intra-train feedback system. An upstream dipole corrector magnet can be used to steer the beam so as to introduce a controllable vertical position offset in stripline BPM ML11X. The BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board to provide an analogue output correction signal. This signal is input to a fast amplifier that drives an adjustable-gap stripline kicker [10], which is used to steer the beam back into nominal vertical position. BPMs ML12X and ML13X serve as independent witnesses of the beam position.

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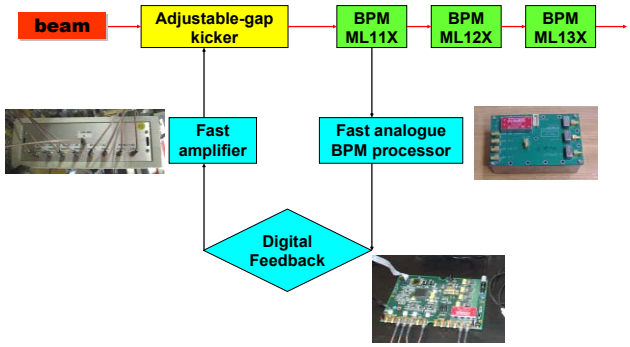

Figure 2: Schematic of FONT4 at the ATF extraction beamline showing the relative locations of the kicker, BPMs and the elements of the feedback system.

The ATF damping ring can be operated so as to provide an extracted train that comprises 3 bunches separated by a time interval that is tuneable in the range 140 - 154 nanoseconds. This provides a short ILC-like train which can be used for controlled feedback, or feed-forward [11] system tests.

FONT4 (see also [9]) has been designed as a bunch-by-bunch feedback with a latency goal of less than 140ns. This meets the minimum ILC specification of c. 150ns bunch spacing, as well as the smallest spacing allowed at ATF. This will allow measurement of the first bunch position and correction of both the second and third ATF bunches. The correction to the third bunch is important as it allows test of the 'delay loop' component of the feedback, which is critical for maintaining the appropriate correction over a long ILC bunchtrain. The constituents of the design latency are shown in Table 1.

Table 1: Design parameters for the FONT4 system

Source of delay	Contribution to latency (ns)
Beam time-of-flight	4
Signal return time	10
BPM processor	7
ADC/DAC	40
FPGA processing	25
I/O	3
Amplifier risetime	40
Kicker fill time	3
Total	**132**

ANALOGUE BPM SIGNAL PROCESSOR

The design of the front-end BPM signal processor [9] is based on that for FONT3 [7] and is illustrated in Figure 3. The top and bottom (y) stripline BPM signals were subtracted using a hybrid. The resulting difference signal was band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signal is low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds, in an attempt to yield a total processor latency in the range 5-10ns. The performance of the FONT4 signal processor was reported previously [9]; the latency is around 7ns.

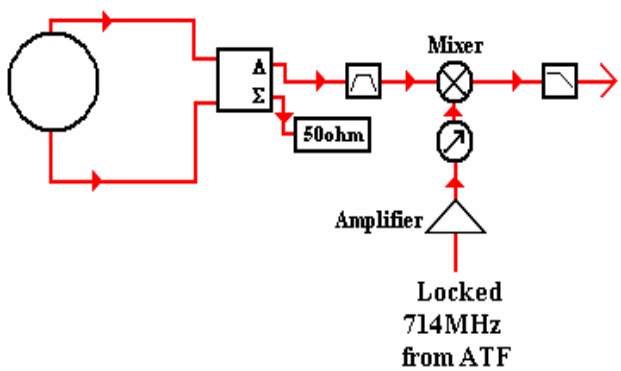

Figure 3: Schematic of FONT4 BPM signal processor.

DIGITAL FEEDBACK BOARD

The custom digital feedback processor board is shown in Figure 4. There are two analogue signal input (output) channels in which digitisation is performed using Analog Devices ADCs (DACs) which can be clocked at up to 105 (210) Ms/s. The digital signal processing is based on a Xilinx Virtex4 FPGA [8] which can be clocked at up to 500MHz. The on-board clocking is derived from the 357 MHz master ATF clock that is phased with respect to the beam. Logic operations are triggered with a pre-beam signal. The ADC/DAC are clocked at 357/4 Ms/s and the FPGA at 357 MHz. The analogue BPM processor output signal is sampled at the peak to provide the input beam position signal to the feedback.

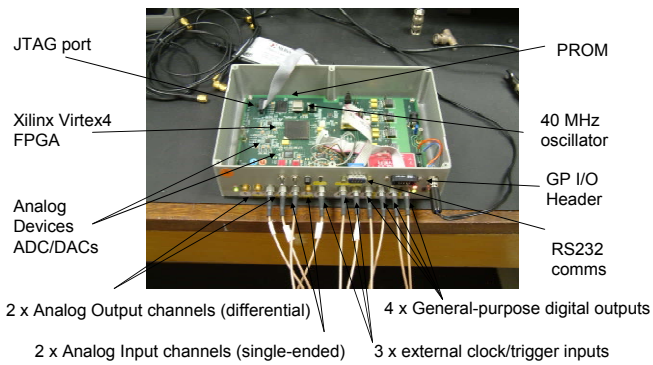

Figure 4: FONT4 digital feedback board.

The gain stage is implemented in digital logic via a lookup table stored in the FPGA. The output is converted back to analogue and used as input to the driver amplifier.

FEEDBACK AMPLIFIER

An outline design of the driver amplifier was made in Oxford and two units were manufactured by TMD Technologies [12], a UK-based RF company. The amplifier was specified to provide +-30A of drive current into the kicker [10], whose striplines were shorted at the upstream end (nearer the incoming beam). The risetime, starting at the time of the input signal, was specified as 35ns to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds. Although current operation is with only 3 bunches in a train of length c. 300ns, it is planned in future to operate

ATF with extracted trains of 20 or 60 bunches with similar bunch spacing; the design allows for this upgrade.

BEAM TEST RESULTS

First beam tests were performed in December 2006. Figure 5 shows, as an example, closed-loop operation with the feedback output set to a large positive value. The incoming bunchtrain, with bunch spacing 154ns, was steered to a negative position. The feedback detected bunch 1 and corrected bunches 2 and 3 to large positive positions.

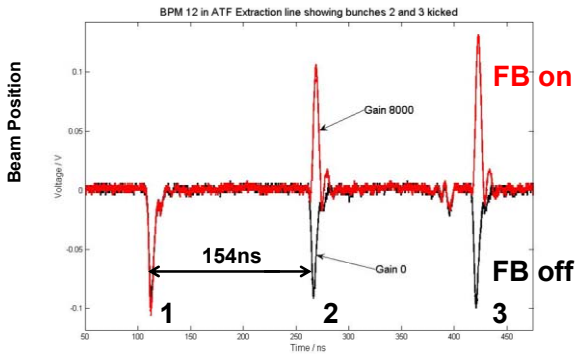

Figure 5: Illustration of feedback amplifier test.

In February 2007 the delay-loop function was implemented in the FPGA logic. Figure 6 shows its operation. The incoming bunches are shown as black squares (top). The blue squares (middle) show the effect of feedback, with coarsely optimised gain, on bunch 2; without the delay loop bunch 3 remains uncorrected. The red squares (bottom) show the effect of the delay loop, whereby bunch 3 is also corrected with a signal derived from both bunches 1 and 2. The latency is c. 140ns.

In May 2007 beam tests were performed with systematic variation of the feedback gain so as to optimise the quality of the position correction. Figure 7 shows an example in which the beam (bunch 2) was steered to zero for a range of incoming positions of c. +-300 microns. Interestingly the correction to bunch 3 is not quite perfect. This arises because of the fact that bunch 2 sits systematically high in position with respect to bunches 1 and 3; such a static position offset within the train can in principle be accounted for in the feedback logic. This will be the subject of ongoing feedback tests in 2007/8.

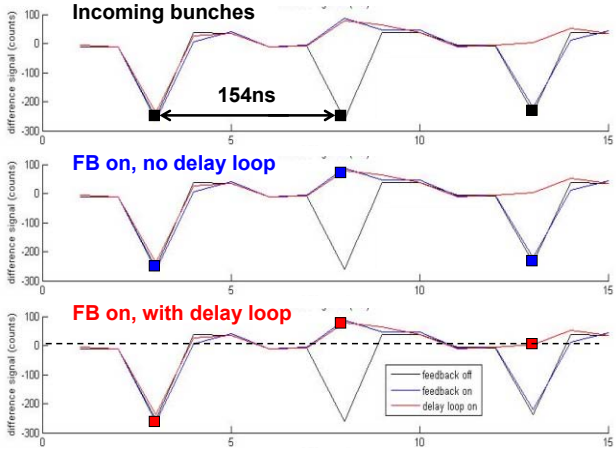

Figure 6: Illustration of feedback test with delay loop.

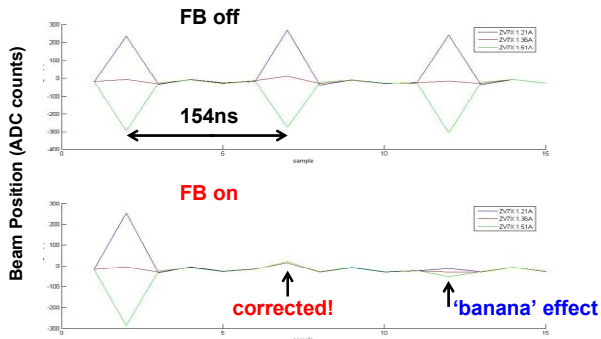

Figure 7: Feedback performance with optimised gain.

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