DEVELOPMENT OF A GENERAL PURPOSE POWER SYSTEM CONTROL BOARD*

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Abstract

In an effort to control modern solid state power modules, a general purpose, multi function power system control board (PSCB) has been under development as a collaboration project between Pohang Accelerator Laboratory (PAL), Korea, and Stanford Linear Accelerator Centre (SLAC), USA. The PSCB is an embedded, interlock supervisory, diagnostic, timing, and set-point control board. It is designed to use in various power systems such as sequenced kicker pulsers, solid state RF modulators, simple DC magnet power supplies, etc. The PSCB has the Ethernet communication with the TCP/IP Modbus protocol.

INTRODUCTION

As high frequency switching solid state devices are replacing tube devices and linear devices, power systems become more compact and modular. In order to maintain reliable operation of the power system module, the control board is required to have complex diagnostic and control functions. Moreover, the control board needs to be compact and low power consuming to work with a power system module. It also needs to have a fast communication with a main control station. However, there is no such control board available commercially. Therefore, a general purpose power system control board (PSCB) has been under development as a collaboration effort between PAL and SLAC. Fast and slow signal diagnostic functions are specially emphasized in the PSCB. Several PSCB prototypes are fabricated and tested in PAL.

MAJOR SPECIFICATIONS

The PSCB is a multi-function diagnostic controller. Main specifications and functions of the PSCB are listed in the table 1. As listed in the table, the PSCB has multiple control inputs such as remote gate trigger synchronization, slow and fast ADCs, tandem and external interlock inputs, and various serial communication ports. Main communication of the PSCB is the Modbus TCP/IP UTP Ethernet serial communication. The PSCB has a mutual communication monitor. The PSCB has various control input and output commands such as trigger initialize, trigger start, stop, and reset, stored RAM data reading, arrangement register writing, diagnostic register reading, relay on and off control, digital analog conversion control, etc.

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Table 1: Major Specification of PSCB

INPUT	
Fast Signal	8 Channel (CH) ADC; 20 MSample/s, 10 MHz bandwidth; Pulse signal with ± 1V max. level, 50Ω impedance, 2mS max. width; Memory size: 512kB/CH x 8-CH = 4096kB
Slow Signal	8-CH ADC with a multiplexer; 1Msps sampling speed; Signals with 0~10V level, 1kΩ impedance; Memory size: 512kB
Digital	19-CH (9-CH Optocoupler isolated and 10-CH non-isolated TTL); Tandem Interlock input
TIMING	
Remote Gate Trigger Sync.	1-CH remote gate trigger synchronization signal input; Optical fiber receiver input; Frequency: 1 to 150 Hz; Pulse Width and Delay: Adjustable from 1 μS to 2ms with 10ns adjustable step resolution.
Clock	100 MHz FPGA clock
COMMUNICATION	
Ethernet	Modbus TCP/IP UTP Ethernet; serial
RS232C	Serial
JTAG	Serial
OUTPUT	
Digital	10-CH (3-CH Optocoupler isolated and 7-CH non-isolated TTL); Tandem Interlock output
DAC	8-CH; 16-bit; Bipolar; ± 10V level output

STRUCTURE

A block diagram of the PSCB is shown in Fig. 1. In Fig. 1, all inputs and outputs listed in Table 1 are shown. The fast and slow analog signal inputs are connected into differential input operational amplifier circuits in order to minimize common mode signal noise level. Digital inputs and outputs are optocoupler isolated. The 8-ch DAC are not isolated outputs. The PSCB uses a DSP and a FPGA. It uses SRAMs for data storage. The major function of the DSP is communication while the FPGA is used for high speed signal processing.

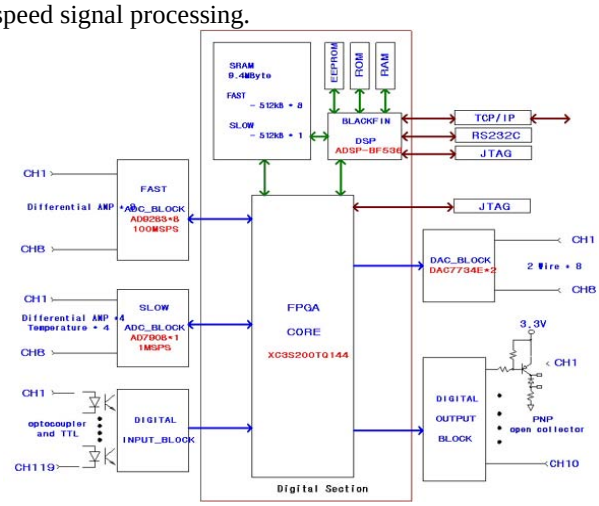

Figure 1: Block diagram of PSCB

Major Components

In the following, major components of the PSCB are listed;

- DSP: Analog device-ADSP_BF_533 × 1, with μC linux operating system
- FPGA: Xilinx Spartan3 _ XC3S1500FG676 × 1
- Fast ADC: Analog Device AD9238 × 8
- Slow ADC: Analog Device AD7908 × 1
- DAC: Burr-Brown DAC7664 × 2

Important properties of the PSCB PCB are

- PCB size : 270mm * 140mm
- +48V Single External power source
- Total power consumption of about 15 W.
- Built in On-Board DC/DC converter
- Single ground PCB

Local Gate Trigger Synchronization

In order to synchronize in time between multiple power modules by a remote gate external trigger synchronization signal, a 100 MHz internal clock is used. A conceptual timing diagram is shown in Fig. 2.

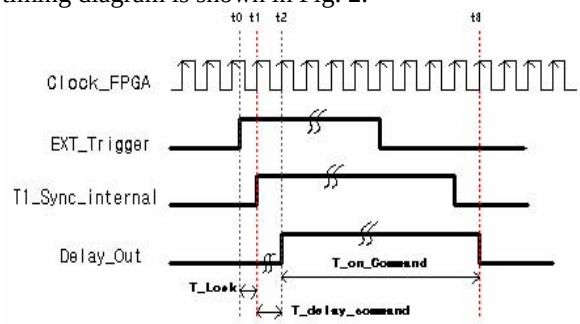

Figure 2: Conceptual trigger timing diagram

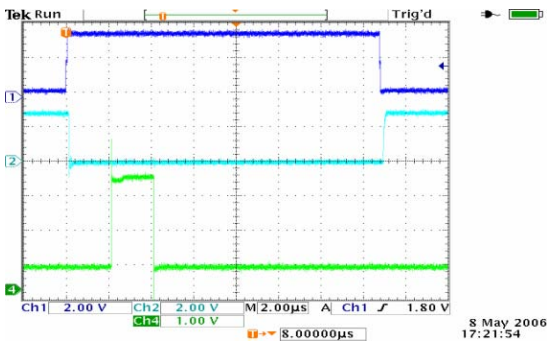

Figure 3 Example of Gate Trigger Synchronization Ch1: Ext_trigger; Ch2: T1_sync_internal; Ch4: Delay_out (Delay: 2 μs, Width: 2 μs)

As the remote gate synchronization signal is received in the PSCB as an asynchronous signal (time t0 in Fig. 2), it will immediately generate an internal signal (T1_Sync_internal in Fig.2) that is synchronized with the FPGA clock at the rising edge as shown in Fig. 2 (time t1 in Fig. 2). Then the PSCB will generate a trigger output signal whose delay and pulse width is determined by an operator's command. The delay and width control resolution is 10 ns. The trigger output is one of the digital outputs of the PSCB. It is aimed to provide as a trigger signal to an IGBT driver circuit. Real scope waveforms of those three are shown in Fig. 3. The output displayed in Ch 4 is a result of 2 μs delay and 2 μs width commands.

Signal ADC

In Fig. 4, a block diagram of the fast ADC structure is shown. The fast ADC has total 8 channels. The maximum input level of the fast ADC is ±1V. A SMA connector is used for the input. The signal is firstly inputted into a differential operational amplifier. A detail circuit diagram of one fast ADC channel is given in Fig. 5. The signal is converted into a 0 to 1 V level and then transferred into the ADC. The signal is then digitized as 8-bit data with a 20 MSample/s rate, while the internal clock runs with 100 MHz rate. The digitizing process is controlled by the FPGA. The digitized data are sequentially stored into RAMs. For each channel, 8 current data are stored in the memory. The data is transferred to an external controller data base with pre-programmed fault events or by external commands. The digitizing process is sized during the data transfer.

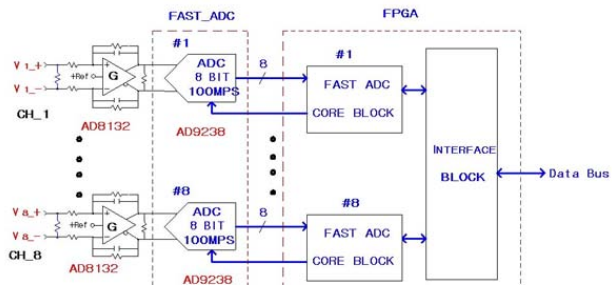

Figure 4: Block diagram of the fast ADC structure.

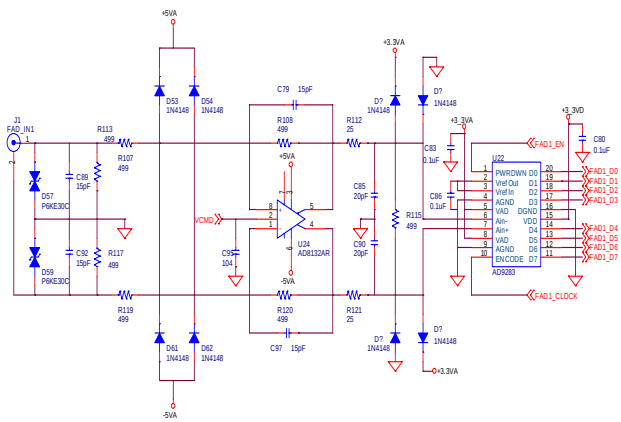

Figure 5: Circuit diagram of a fast ADC channel.

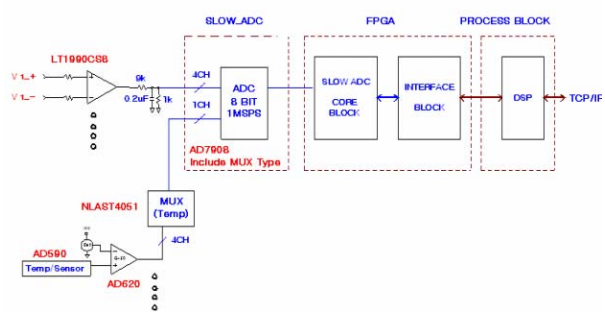

Figure 6: Block diagram of the slow ADC structure.

Fig. 6 shows a diagram of the slow analog interface. The PSCB has an 8-input analog MUX and a slow ADC to sample slowly varying signals such as temperature, air flow, etc. Each trigger synchronization signal pulse cause the MUX to one-step cycle through its inputs. Any event that inhibits the local gate trigger holds the last sample of each waveform in memory. The input signal level of the slow ADC (AD7908) ranges from 0 to +10V.

DAC

A block diagram of the DAC structure is given in Fig. 7. The DAC has 8 channels, and each channel output has a 16-bit resolution. Each DAC 7664 chip has four DAC channels with 0 to ±2.5V output level. The output level is amplified to 0 to ±10V level so that it can be easily adopted as a high precision DC power supply reference level. The FPGA has a core block to control the DAC. Set values of each channel are determined by a command that follows the TCP/IP Modbus protocol.

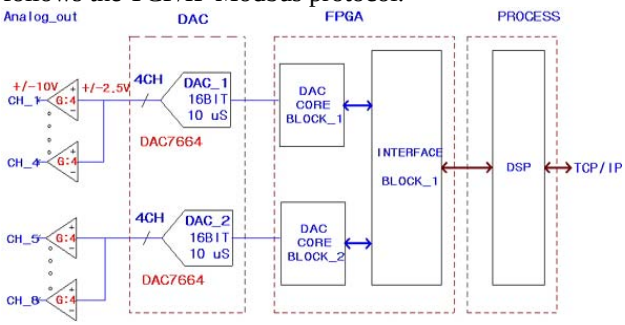

Figure 7: Block diagram of the DAC structure.

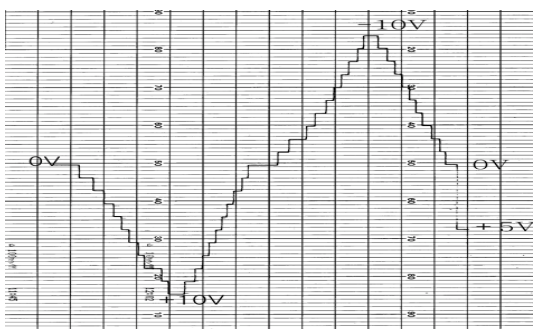

Figure 8: An example of the DAC output graph.

A PSCB DAC output that follows the command of an external control computer is recorded with a Yogogawa LR4100, and the result is shown in Fig. 8. The command varies full output range with one volt step. The DAC output performs well as designed.

Control and Display Screen and Test Result

A prototype PSCB is manufactured and tested with an IGBT induction modulator cell that is constructed at SLAC [1, 2]. In Fig. 9, the channel 2 shows the PSCB gate trigger output, and the channel 1 is an output current signal of an IGBT in the cell. The output current is also recorded with the fast PSCB ADC, and the result is also shown in Fig. 10. The two IGBT current signals are not exactly same signals, and therefore have some discrepancy in waveforms. We however confirmed that the fast PSCB ADC performs very well to reconstruct IGBT switching waveforms. We also confirmed that the sequential data storage in the memory and transfer by a command also works very well. We have not yet successful to acquire slow analog signals due to complexity in software. However, all other functions such as digital input and outputs are successfully tested.

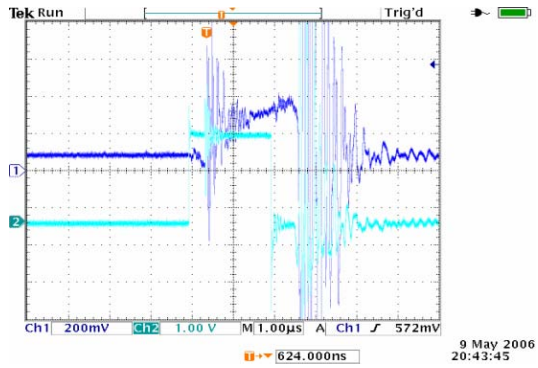

Figure 9: Gate trigger (Ch2) and IGBT current (Ch1).

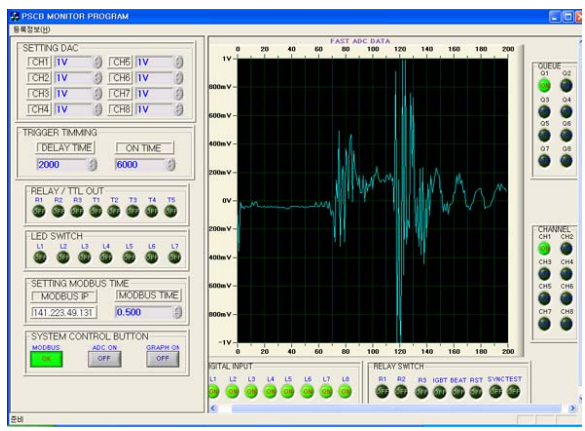

Figure 10: Control and display screen of the PSCB.

CONCLUSION

In-situ and real time diagnostic and control of power modules become extremely important. With an intention of solving such challenging problem, we developed a prototype PSCB. The PSCB is a multi-function, embedded, interlock supervisory, diagnostic, timing, and set-point control board. Preliminary test results shows that the PSCB has a potential to work in many different power system modules. We have a plan to continuously upgrade the PSCB to have simple interfaces, small size, low power consumption, easy swapping, and user friendly software.

REFERENCES

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