COMMISSIONING OF THE DIGITAL TRANSVERSE BUNCH-BY-BUNCH FEEDBACK SYSTEM FOR THE TLS

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Abstract

Multi-bunch instabilities degrade beam quality through increased beam emittance, energy spread and even beam loss. Feedback systems are used to suppress multi-bunch instabilities associated with the resistive wall of the beam ducts, cavity-like structures, and trapped ions. A new digital transverse bunch-by-bunch feedback system has recently been commissioned at the Taiwan Light Source, and has replaced the previous analog system. The new system has the advantages that it enlarges the tune acceptance and improves damping for transverse instability at high currents, such that top-up operation is achieved. After a coupled-bunch transverse instability was suppressed, more than 350 mA was successfully stored during preliminary commissioning. In this new system, a single feedback loop simultaneously suppresses both horizontal and vertical multi-bunch instabilities. Investigating the characteristics of the feedback loop and further improving the system performances are the next short-term goals. The feedback system employs the latest generation of field-programmable gate array (FPGA) processor to process bunch signals. Memory has been installed to capture up to 250 msec of bunch oscillation signal, considering system diagnostics suitable to support various beam physics studies.

INTRODUCTION

The Taiwan Light Source (TLS) of NSRRC is a 1.5 GeV storage ring. Vertical instability was a problem during the early operations of the TLS. It can be suppressed by over-compensating for chromaticity and/or using a vertical transverse feedback system [1]. Two major upgrades of TLS have recently been completed - the superconducting RF cavity (SRF) upgrade in late 2004 and the top-up operation in late 2005. Both upgrades are intended to increase the stored beam current from 200 mA to more than 400 mA and to provide a high-quality photon beam. The SRF upgrade was to eliminate the strong instability caused by high-order modes (HOM) from conventional RF cavities, while the top-up operation was to maintain a constant heat load to the vacuum chamber components. Transverse feedback is essential to exploit the benefits of these upgrades. Transverse multi-bunch instability caused by the resistive wall, the cavity-like structure of the beam duct, and the ions is suppressed by feedback systems. The previous transverse feedback system [1] employed a scheme with one pick-up and one kicker, and its performance was strongly affected by the working tune. The system was upgraded in late 2005 to overcome the problem of tune dependence and improve damping performance [2]. The latest generation FPGA-based feedback processor was adopted. The status and commissioning results of the new feedback system are presented herein.

NEW TRANSVERSE FEEDBACK SYSTEM

A severe transverse instability occurs at the TLS that cannot be controlled by over-compensating the chromaticity without affecting routine operation. The resistive wall and ion-related effects might contribute to this instability. The feedback processor for TLS was originally developed for the SPring-8 [3, 4]. This highly flexible design of the feedback processor led to the easy adoption to TLS applications. Figure 1 presents a block diagram of the system. The new FPGA-based system uses the two-dimensional feedback based on the single-loop scheme proposed by Nakamura [4] to simplify the system. The system consists of a beam position monitor (BPM), an analog front-end (analog demultiplexer), a feedback processor, power amplifiers and kickers. The feedback processor is the key component of the feedback system, and is taken from the design of SPring-8 with minor modifications.

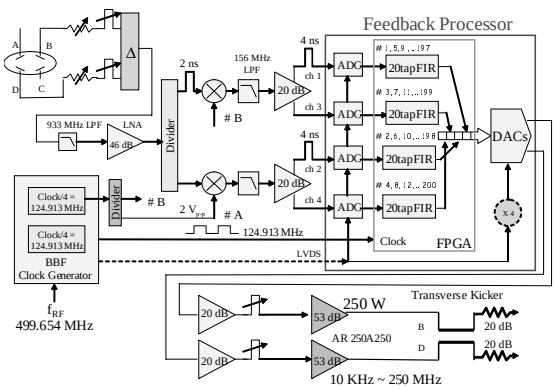

Figure 1: Functional block diagram of transverse feedback system.

The beam signals picked up by the BPM are processed by an analog demultiplexer into a baseband signal and fed

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Contributed to 10th European Particle Accelerator Conference (EPAC 06), 06/26/2006--6/30/2006, Edinburgh, Scotland

Work supported in part by US Department of Energy contract DE-AC02-76SF00515

to the digital feedback processor, where the position oscillation signal of each bunch is converted into digital form and filtered by the FIR filters. The kicker is driven by the filtered BPM signal to dampen the bunch motion. The latency of the system from the BPM to the kicker should be one or two periods of revolution of the ring plus the bunch propagation delay between the BPM and the kicker in the transverse feedback loop. In the four-ADC mode, the feedback processor is operated in four parallel channels of the ADC and the FIR filter. A dynamic range of several mm is required to prevent saturation by the perturbation at injection, or by a large distortion of closed orbit. The 12-bit resolution ADC can fulfil the dynamic range requirement without a correlator (notch) filter. The bunch rate or RF frequency is 499.654 MHz and the harmonic number is 200. The feedback processor and ADCs are operated with a clock frequency of $f_{RF}/4$. The f_{RF} was selected as the carrier frequency of the signal from the BPM electrodes. According to this signal, the frequency band of the beam motion covers from 250 MHz to 750 MHz, which includes all instability modes. The FPGA processor supports a FIR filter of up to 20 taps. Up to 32 sets of FIR filter coefficients can be stored in the internal register of FPGA and are selectable via a USB 2.0 interface or with an external logic input. In the latter case, the switching speed is about 10 nsec. This function makes the system very flexible for use in grow-damp experiments**.** Up to 128 historic Mega-samples of ADC can be stored in the double-data rate (DDR) memory in the feedback processor. Therefore, up to 256 ms of data can be stored in the memory. The latency time of the feedback processor is around 300 nsec. A good frequency response of the FIR filter can easily be achieved using a two-turn delay (800 nsec) in the transverse feedback loop. The frequency multiplier supplies a DAC clock at the RF frequency with a cycle-to-cycle jitter of 50 psec from the ADC clock. When jitter is a problem, the external clock can replace the frequency multiplier as clock source of DACs. The processor is equipped with five DACs - four for the multiplexed FIR filter output and one for multiplexed raw ADC data for diagnostics and tuning. The latency of the multiplexed FIR filter output can be controlled by adjusting the internal delay. Each DAC has complementary outputs. When several kicker electrodes are used for feedback, the delay and polarity of the individual kicker must be tuned. Such tuning is easily performed using these functions and outputs.

This TLS feedback loop consists of one pick-up and one kicker. The feedback FIR filter is linearly combined with vertical and horizontal responses. Bunch oscillation signals are multiplexed into four parallel channels in an analog manner. Delay lines align the four consecutive bunches in parallel sense. ADC with four parallel channels and four FIR filters is used to process the feedback signal. The differential output of the DACs drives two power amplifiers. Figure 2 plots the typical response of the FIR filter. A feedback FIR filter can be designed in several ways. Time domain least square fitting (TDLSF) [4] developed by Nakamura was applied to the current configuration. The FIR filters also compensate for the phase advance between the pick-up and the kickers.

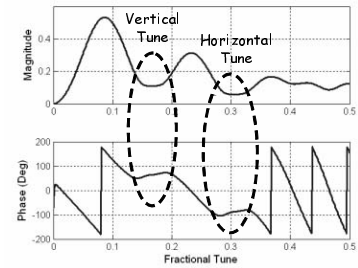
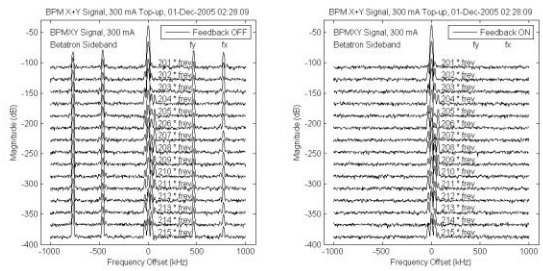


Figure 2: Measured transfer function of the prototype FIR filter designed by time domain least square fitting method.

A compact Flash (CF) card is used as a booting device and stores configuration data of the feedback processor. The USB 2.0 interface is provided to control the processors and to transfer captured data. A device driver of the feedback processor for the Linux kernel 2.4 is developed and its most functions are controllable. The device driver for Linux is available. Control software from the NSRRC and Matlab are installed in a Linux PC to provide a convenient environment for the interface of the feedback processor. Matlab scripts control the accelerator through the existing Matlab interface, the feedback processor via the USB 2.0 interface, and electronic instruments via the IEEE-488 interface. This environment effectively supports various investigations.

COMMISSIONING RESULTS

New transverse feedback was commissioned in late November. Figure 3 (a) shows numerous betatron sidebands without feedback. These betatron sidebands are fully suppressed by the feedback loop, as shown in Fig. 3 (b).



(a) Feedback loop open. (b) Feedback loop closed.

Figure 3: Transverse spectrum form harmonic 201 to 215 at the frequency of revolution frequency, f_{rev}. Strong synchrotron lines are observed near the harmonics at the revolution frequency as the longitudinal feedback was off.

Figure 4 shows the result of a grow/damp experiment and its modal analysis [5, 6]. A damping time of less than 1 msec and an operating current of 300 mA were achieved for all modes in horizontal and vertical plane. Figure 5 shows the growth rate of vertical mode 198. The estimated growth rate for future 400 mA operation is slightly less than 2 ms^{-1}. The damping time including

feedback system is around -6 ms^{-1} for the strongest mode, and stable operation of the transverse feedback system is expected for 400 mA. The onset of the vertical instability is around 40 mA, very close to the vertical instability threshold which is around 20 ~ 30 mA. Typical modal spectrum is shows in Fig. 6. The vertical modal spectrum contains a peak, which may come from ion-related effects. Beam blow-up due to transverse instability is easily identified from the synchrotron radiation profile shown in Fig. 7(a), without feedback. After the feedback loop was closed, the beam was stable, as shown in Fig. 7(b).

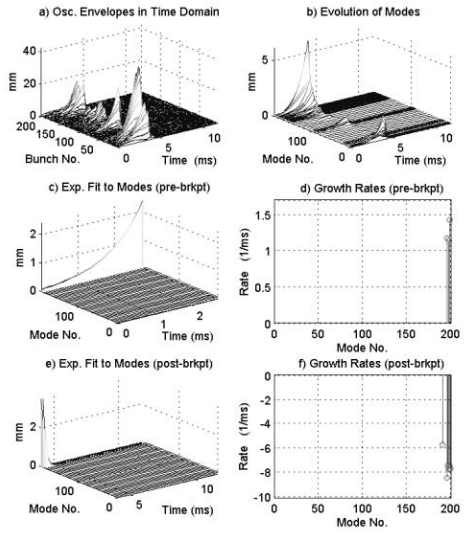


Figure 4: Grow/damp experiment results and growth and damping time fitting results for 300 mA stored beam. The growth rate is about 1.25 ms^{-1} for the strongest mode. The damping rate is around -6 ms^{-1}. Sufficient damping is achieved at 300 mA.

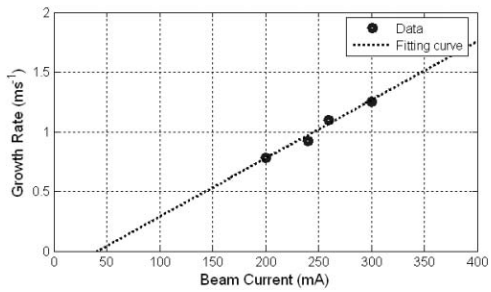
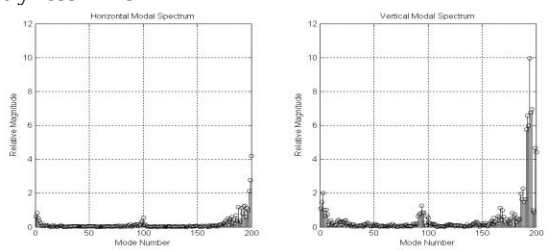
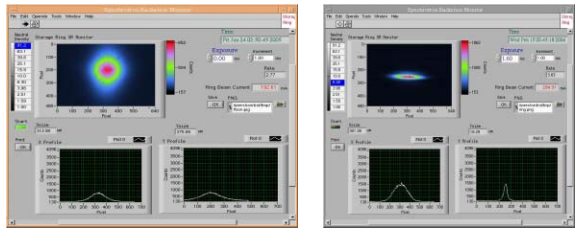


Figure 5: Growth rate of vertical mode #198 as a function of stored beam current. The estimated growth rate is slightly less 2 ms^{-1} at 400 mA.



(a) Horizontal (b) Vertical

Figure 6: Modal spectrum of the typical 300 mA stored beam.



(a) Open loop. (b) Closed loop.

Figure 7: Transverse profile observed by synchrotron radiation monitor. There is no longitudinal feedback at this measurement.

SUMMARY

This report summarizes the preliminary results of the newly commissioned transverse feedback system at the TLS. The transverse feedback loops are presently in service. It was successfully tested at 350 mA. The transverse feedback system not only eliminates instability but also improves the injection efficiency since it enables low chromaticity operation, which is essential for the top-up injection. The system performance and reliability of both loops are constantly being improved. The functionality of the feedback system will be gradually enhanced.

ACKNOWLEDGEMENT

The authors are grateful to Drs. J. Fox, D. Teltymann, and S. Prabhakar for sharing their valuable experience on feedback systems and sophisticated analysis tools. We would like to thank Dr. M. Tobiyama for information on technical aspects of the power amplifiers in the feedback system.

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