Development of Ultra-fast Silicon Switches for Active X-Band High Power RF Compression Systems

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Abstract. We present the recent results of our research on the high power ultra-fast silicon RF switches. This switch is composed of a group of PIN diodes on a high purity silicon wafer. The wafer is inserted into a cylindrical waveguide under TE_{01} mode, performing switching by injecting carriers into the bulk silicon. Our current design uses a CMOS compatible process and the device was fabricated at SNF (Stanford Nanofabrication Facility). 300 ns switching time has been observed, while the switching speed can be improved further with 3-D device structure and faster driving circuit. Power handling capacity of the switch is at the level of 10 MW. The switch was designed for active X-band RF pulse compression systems - especially for NLC, but it is also possible to be modified for other applications and other frequencies.

Keywords: RF switch, pulse compression, semiconductor, PIN diode.

1. INTRODUCTION

RF pulse compression systems are commonly employed to match the longer pulses from the RF sources with comparatively lower power to the loads which require shorter but higher power pulses. Such loads include, but not limit to particle accelerator structures and RF undulators. Since the development of the SLED (SLAC Energy Doubler) [1], several pulse compression schemes have been studied. Active pulse compression systems using high power RF switches have attracted research interest in recent years. Theoretical studies [2] have shown that high efficiency and small system size can be achieved simultaneously in active pulse compression systems. This idea has inspired our research interests in ultra-fast high power RF switches, although there are a lot of other potential applications.

The SLED II pulse compression system employs high *Q* resonance delay lines behind an iris to accumulate RF energy from the incoming pulse, and then the incoming pulse is reversed 180° in phase, so the reflected pulse from the input and the emitted RF from the delay line can add constructively to form a higher-power pulse. In an active compression system, the iris is replaced by a switch, which allows the RF energy stored in the delay lines to be fully discharged in one delay cycle so that higher intrinsic efficiency can be achieved.

The switch used in this application should have high power handling capability, fast switching time and low insertion loss. To observe the pulse compression, the switching time must be shorter than the round trip time of the resonant delay line –

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which is 400ns in our setup; while in a practical system, a fraction of the round trip time is required. The insertion loss of the switch will reduce the efficiency of the pulse compression system significantly. To attain higher efficiency than the SLED II system, the switch should have less than 10% loss during the charging cycles.

Tamura and Tantawi have demonstrated a semiconductor PIN diode switch capable to handle 12MW RF power [3]. The switch was implemented with a PIN diode array active window. The switch is operated at the TE_{01} mode in circular waveguide. This mode has no radial electric field, which gives the possibility to leave a full gap in the waveguide for the active window and vacuum sealing etc without RF leakage. The PIN diodes are fabricated on a 4 inch high purity and high resistivity silicon wafer. The P and N doping lines are on different sides of the wafer in radial direction. During the operation, a forward bias is applied on the diodes first, injecting carriers into the silicon wafer to make it reflective to RF; then high voltage reverse bias is applied to remove those carriers and switch the wafer transparent to microwaves. But the speed of switching from reflective to transparent is very slow, on the order of 100 microseconds, which is not acceptable for the pulse compression application.

In the rest of this paper, our recent research results on the ultra-fast high power RF semiconductor switches will be discussed. Same as Tamura's design, the switch works in a circular waveguide under TE_{01} mode, using PIN diodes to inject carriers into silicon wafers. The switch works in a narrow band at 11.424 GHz. The major efforts of our research are focused on the improvement of switching speed and insertion loss. A specially designed low-loss circular waveguide Tee is used in our setup, allowing us to tune the transmission and reflection coefficients of the switch with very low losses. Several approaches including planar structure with bulk silicon wafers, planar structure with silicon-on-insulator (SOI) wafers, and 3-D structure have been studied. Planar structure devices with both bulk and SOI wafers have been fabricated by the authors and tested at low power. 300ns switching time has been observed on bulk wafer devices. Nonetheless, the fabricated planar SOI switches are not working properly because the quality of the SOI wafers cannot meet our requirement. Simulation on 3-D structure devices shows that sub-100ns switching is possible. Other possible applications will also be discussed.

2. DEVICE DESIGN AND FABRICATION PROCESS

The schematic layout of the switch window is shown in Fig. 1. The window is inserted into the gap between two 1.3 inch waveguides. The P/N doping region and metal lines are radial, so they won't cut E-field under the TE_{01} mode. The PIN diodes form a narrow ring at the peak E-field radius inside the waveguide and the silicon will reflect microwaves most efficiently when carriers are injected. There is a narrow metal ring inside the diode ring, which provides bias for N doped lines when metal connection from outside of the diode ring is not practical. The metal ring can minimize the reflection from the silicon wafer when the diodes are off, and assist reflection when the diodes are on so the switch requires less injected carriers. The silicon inside the metal ring can be cut to further reduce insertion losses. The 1.3 inch diameter of the waveguide is close to cut off, which can reduce the carriers density needed for reflection and increase the switching speed, but compromises power handling capacity

and RF losses. Floatzone silicon wafers with 500 micron thickness are used to build the switches, although thinner wafer will have lower loss.

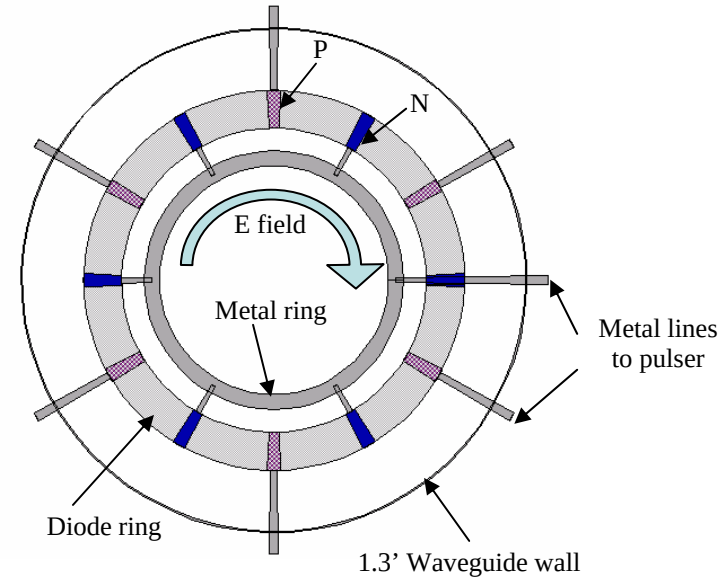

FIGURE 1. Schematic layout of the active window, top view

The structure is simulated with HFSS. When diodes are off, the window has 3% loss and 97% transmission, compared to almost full reflection without the metal ring. When diodes are on, assuming a carrier layer with 50 micron thickness is formed under the wafer surface, transmission is less than 1%; the losses will be 10% if carrier density is $5\times10^{16}/cm^3$ and 3% if carrier density is $5\times10^{17}/cm^3$.

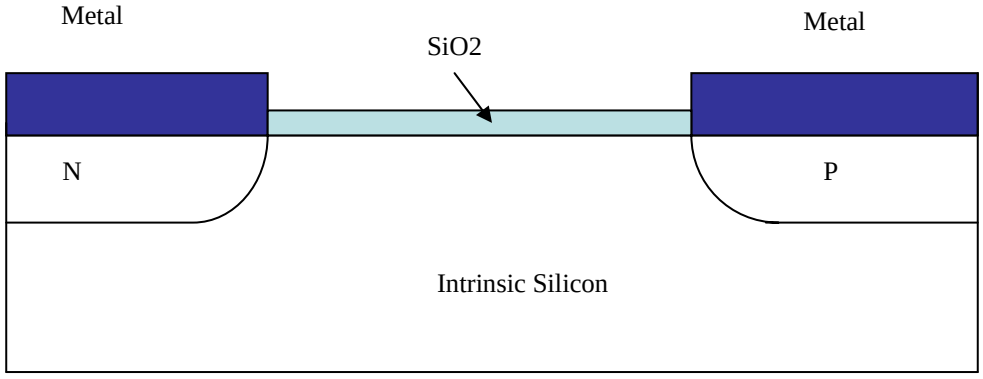

FIGURE 2. Structure of the Planar PIN Diode

At the diode level, we have chosen planar structures instead of Tamura's double side structure. This structure is compatible with the widely used silicon CMOS process, which is available at Stanford Nanofabrication Facility (SNF). The P/N doping was completed with ion implantation and followed by a short anneal. Fig. 2

shows the structure of planar PIN diode. SOI silicon wafer structure is similar, but the device layer is much thinner, with a 1 micron silicon oxide layer and 450 micron silicon handle layer beneath. Devices based on both SOI and bulk wafers are fabricated. The length of the diodes (distance between P and N doping region) ranges between 50 and 100 micron, optimized for switching speed under certain available current pulse. For SOI structure, the device layer thickness is 50 micron.

The fabrication processes of the diodes are simulated with Tsuprem4, and then the electrical properties of the diodes are simulated with MEDICI, using the results from Tsuprem4 [4,5]. Simulation results show that, for devices with 60 μm length powered by a 1 kV pulser with 1 Ohm internal resistance and 30 ns rise time, a 50 μm carrier layer with carrier density averaged at $1\times10^{16}/cm^3$ can be formed in about 100 ns, and reach $5\times10^{16}/cm^3$ in about 300 ns. In the SOI structure, the carrier distribution is limited in the device layer and does not have the tail as in the bulk wafer device. Nevertheless, both simulation and test results showed that the SOI devices will not make significant difference in switching speed and losses.

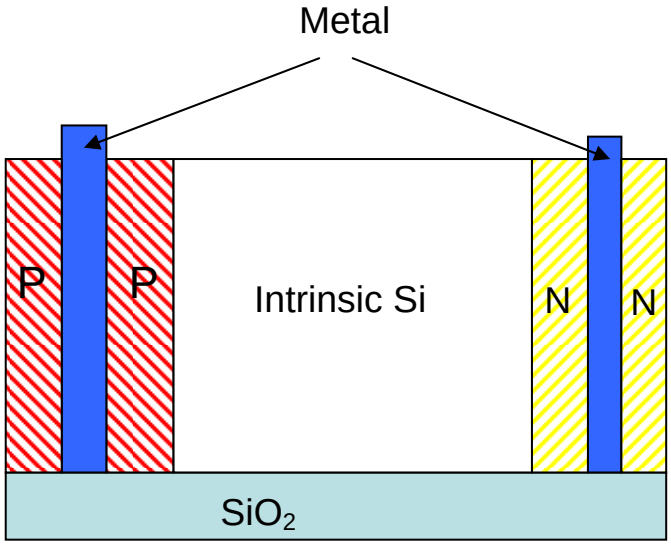

FIGURE 3. Structure of the 3D SOI PIN Diode

FIGURE 4. Fabricated active window.

To enhance the switching speed further, the 3D structure shown in Fig. 3 is desirable. This 3D structure can inject carriers more uniformly into the intrinsic silicon, making the switch much faster. Our simulation shows that with same power supply, $10^{16}/cm^3$ average carrier density can be achieved in less than 50 ns (20 ns more than the assumed power supply rise time), and $5\times10^{16}/cm^3$ in about 70 ns. However, the fabrication of this device is complicated when compared to planar devices. A deep trench in the silicon needs to be etched for doping, and then the trench needs to be filled with metal, which has not been successfully performed yet.

Planar structure devices with SOI wafers and bulk silicon wafers are both fabricated by the authors at SNF. Fig. 4 shows one of the fabricated switches.

3. LOW POWER TEST SETUP AND RESULTS

The switches have been tested at 11.424 GHz with low power. Two switch setups were used. One is the one-pass setup, with the active window assembly connected with wrap-round mode converters at both ends. The mode converters convert from TE_{01} mode in WR90 rectangular waveguide into TE_{01} mode in 1.5inch circular waveguide, so it can be connected to other testing equipment with WR90. The test window assembly includes tapers to match from 1.5 inch to 1.3 inch circular waveguide. This directly characterizes the active window. The other setup is the switch module shown in Fig 5. The front of the switch assembly is connected to the 3rd port of a circular waveguide Tee, and a movable short plunge is connected to the back. This setup allows tuning the switch for low losses. By adding some spacers between the Tee and the switch, the on-state transmission coefficients can be tuned. The off-state transmission coefficients are tuned by the movable short. In the low power test,

wrap-round mode converters are also used on the other two ports of the circular waveguide Tee.

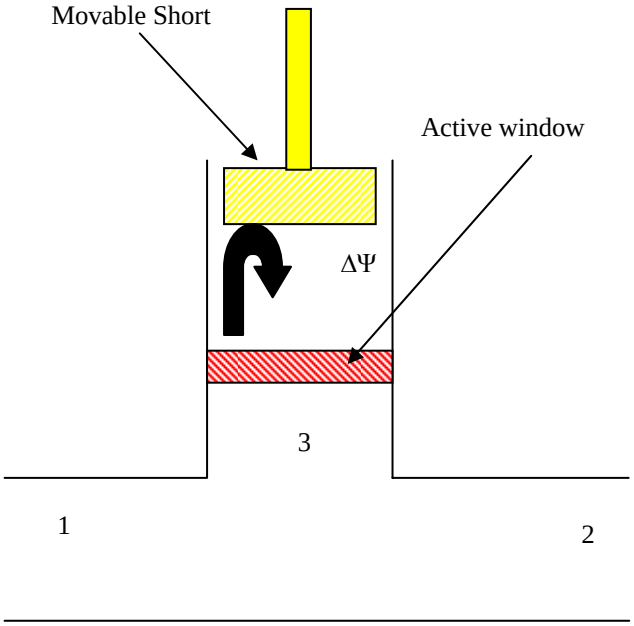

FIGURE 5. Switch Module

3.1. The Circular Waveguide T

In our future pulse compression tests, this switch module will be used to tune the transmission coefficients to the desired value. The RF input/output will be connected to the port 1 of the Tee as shown in Fig. 5, while port 2 will be connected with the low-loss resonant delay lines. A low-loss circular waveguide Tee junction power divider has been specially designed and machined for our test setup. This Tee is composed of a TE_{20} mode rectangular Tee and 3 circular-to-rectangular mode converters. Figure. 6 shows the model assembly of the circular waveguide Tee. With a movable short on the 3rd port, the loss is measured in the range of 1% to 2%, depending on the position of short plane. A large portion of this measured loss is in the wrap-round mode converters connecting to the network analyzer.

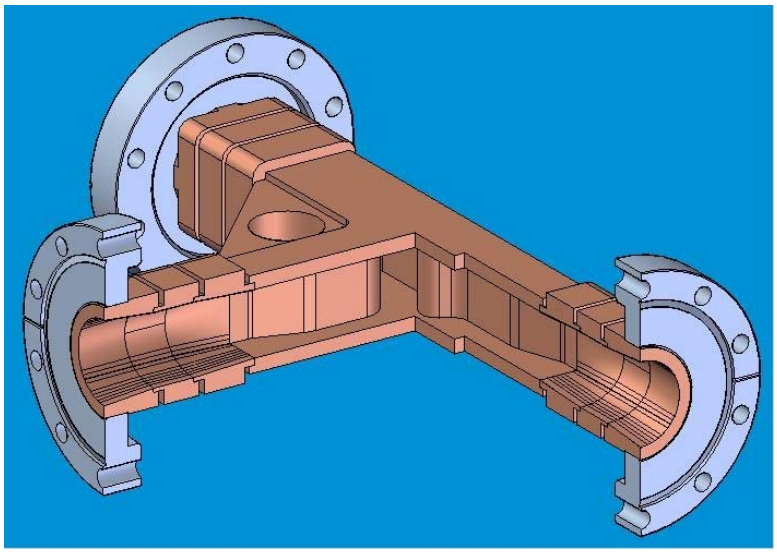

FIGURE 6. The circular waveguide T (By courtesy of R. B. Reed)

3.2. Cold Test

Cold test of the switch is performed to characterize the switches at off state. A network analyzer was used in the test. For the one pass setup, we have S_{11}=0.44 when a hole is cut in the center; for wafers without holes in center, S_{11} is about 0.6. For the wafer with hole, it is off from the full transmission design. The reason is that the waveguide gap width in the wafer holder is larger than the number we used in our original simulation. The later simulation using the actual waveguide gap width has better agreement with the test result. The loss is 10% for the first batch of wafers we fabricated, and it is reduced to 6% in the second batch due to shorter anneal time. Considering the loss in the mode converters and the wafer holder, it is in line with simulation results.

The switch module with circular waveguide Tee was characterized with a network analyzer after the on-state reflection coefficient has been tuned to about 0.38 in the low power test. This is the optimized on-state S_{11} for the pulse compression system. Measurements have been made with the movable short at different location. The optimized location with the desired S_{11}=0.83 has about 7% loss.

3.3. Low Power Test

Low power test has been performed both with one pass setup and the module setup. Pulsed power meter was used to measure the input and the transmitted/reflected power through directional couplers. The switch is powered by a home made circuit, using one IXYS EVDD408 evaluation board driving 2 IRGPS60B120KD IGBT transistors. The current output of this circuit is monitored by a 0.2 Ohm low inductance resistor. At 1KV, the current output rises to 300 A in about 40 ns, and then rises to 800A in 300 ns.

Figure 7 shows the time response of switch module with bulk silicon switch. Two current pulse power supply boards are used in parallel. Switch time is about 300 ns.

The loss is measured at about 15%. A 300 ns switching time also has been observed in the one pass setup.

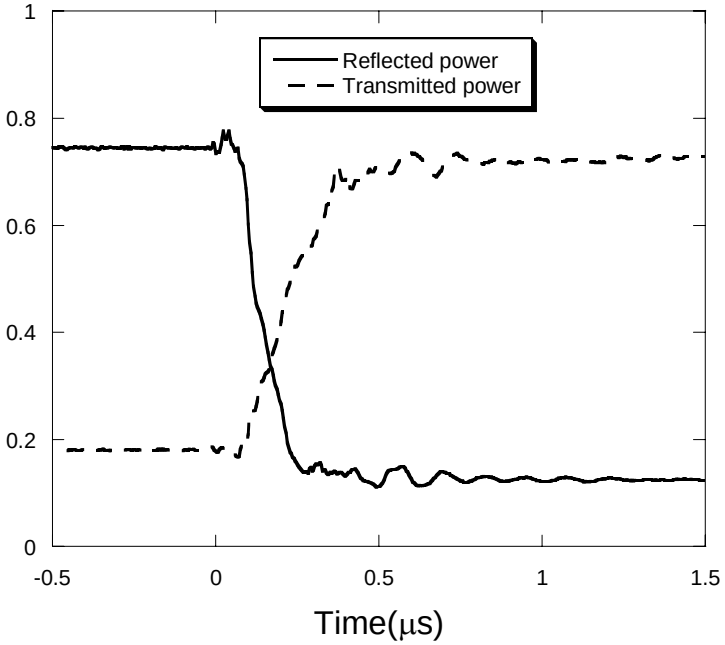

FIGURE 7. Time response of the switch module with bulk silicon switch.

DISCUSSION

Our research has demonstrated 300 ns switch time for a bulk silicon X-Band RF switch, with about 7% off-state loss and 15% on-state loss. The results are in line with our simulation results. The loss and switching speed can be improved by reducing the gap in the wafer holder as well as increasing the current of power supply. Planar structure SOI devices will not enhance the speed and loss significantly. To achieve sub-100ns switching time, 3-D structure with deep trenches is a possible solution, although the metallization technique for the trenches needs to be studied. A pulse compression experiment with 400 ns resonant delay lines will be performed in the future. The power handling capacity of these switches also needs to be characterized.

Another potential application of this semiconductor switch is on pulsed superconducting RF accelerator structures, like in the International Linear Collider (ILC). Although those structures do not need pulse compression systems, extracting the stored RF energy out of the structures between pulses is mandatory to reduce the wall loss inside the structure. Since the superconductor RF structures typically work at liquid Helium temperatures, the cryogenic system needs about 600 J power to remove 1 Joule heat generated by the wall loss [6]. The semiconductor switch is a good choice for that extraction function. Since most of those superconducting structures are working at lower frequency like L-band, the loss in the wafer can be much less. The required switch time is not as critical as in the pulse compression systems. The size of the devices will be larger, so the power handling capacity will be higher. However, the size of devices also limits the lowest frequency. In case that the 4 inch silicon wafers

are used, the lowest frequency can be handled is about 1.3 GHz, with alumina filled in the circular waveguide.

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