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SPEAR3 INTERMEDIATE DC MAGNET POWER SUPPLIES*

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Abstract

The Stanford Synchrotron Radiation Laboratory (SSRL) has successfully commissioned SPEAR3, its newly upgraded 3-GeV synchrotron light source. First stored beam occurred December 15, 2003 and 100mA operation was reached on January 20, 2004. This paper describes the specification, design, and performance of the SPEAR3 DC magnet intermediate power supplies (IPS) that consist of tightly-regulated (better than ±10ppm) current sources ranging from 60 A to 500 A and output powers ranging from 2.4kW to 22.5kW. A total of 69 IPS are in successful operation. The SPEAR 3 upgrade performance and reliability requirements mandated new power supplies for both the SPEAR3 storage ring, and for the booster-to-SPEAR3 transport line. IPS are widely used at SPEAR3 to power single quadrupoles, dipoles, families of quadrupoles and sextupoles, and also Titanium sublimation pumps. IPS topology allows them to be series operated for those magnet strings requiring higher voltages. A compact 19" standard rack-mounted design is common to all the units. These are off-line, switch-mode, operating at 16 kHz to reduce space and provide for fast output response and high efficiency.

1 INTRODUCTION

The Stanford Synchrotron Radiation Laboratory (SSRL) has successfully commissioned SPEAR3, its newly upgraded 3-GeV synchrotron light source [1].

The Power Conversion Department (PCD) [2] at the Stanford Linear Accelerator Center (SLAC) was responsible for defining - jointly with SSRL - the topology of the DC magnet intermediate power supplies (IPS), their operating requirements, as well as working on the procurement process, pre-installation testing, installation, and commissioning. On-site installation of the IPS began mid-2003. Testing started in November and was finished by mid-December [3]. Table 1 summarizes the basic characteristics of the IPS.

Based on the success of several hundred IPS in operation at PEP-II [4], SSRL/PCD mutually determined the SPEAR3 IPS would use similar specifications whenever possible. A modern design and common components would also improve the mean-time-to-repair (MTTR) [5].

This paper describes outside procurement aspects, in-house testing, and commissioning of the IPS. Also described is the method used to stabilize the IPS output current control loop. Long-term stability measurements are also shown.

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Table 1: SPEAR3 DC Magnet Intermediate Power Supply Ratings.

Magnet	*Volts*	*Amps*	*P(kW)*	*PS Qty*
BTS Line				
Septum	50	300	15.0	1
Dipole Bends	45	500	22.5	4
Quadrupoles	80	60	4.8	2
Storage Ring				
Titanium pumps	40	60	2.4	4
Quadrupole singles	100	100	10.0	44
Sextupole strings	100	150	15.0	2
Quadrupole strings	125	80	10.0	4
Quadrupole strings	150	100	15.0	6
Quadrupole strings	200	75	15.0	2

2 GENERAL ASPECTS

All IPS use a Bitbus [6] controller for interface, control, and accurate output current regulation. See figure 1 for details. Internally, the IPS operate as 500-ppm voltage sources. Their voltage control loops have a 3-dB small-signal bandwidth greater than 1 kHz, which is enough to compensate for input line changes and transients. The external, highly-stable, precise, and accurate Bitbus-based current control applies a programming reference to the IPS output voltage regulator for desired output current.

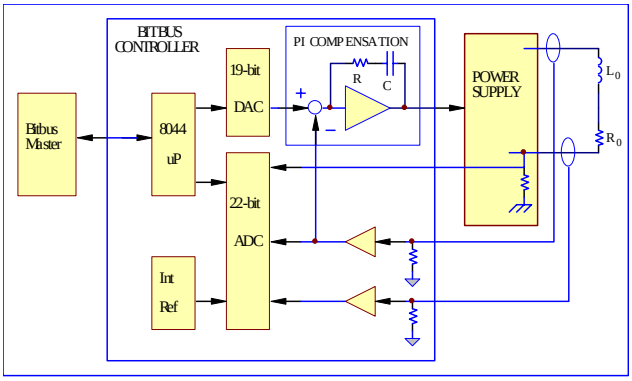

Figure 1: Basic Topology for Bitbus-Controlled IPS.

During field-testing, the parameters of the proportional-integral (PI) compensation circuit, internal to the Bitbus controller, are determined and the overall system (IPS and load) is tuned to exhibit a 3-dB current control loop bandwidth of 10Hz, which is sufficient to correct the slow magnet resistance variations due to temperature changes, and the drifts in the IPS internal voltage control loop.

All IPS are equipped with latched interlocks to detect abnormal internal conditions, such as input voltage out-of-range, heatsink over-temperature, output DC overcurrent, primary overcurrent, and load ground fault. On the IPS front cards, LED indicators are provided for each one of these signals.

A Programmable Logic Controller (PLC) sums the interlocks external to the IPS. The Bitbus controller receives that summary of external interlock information and turns the IPS off under abnormal conditions such as magnet over-temperature or cooling-water flow loss.

3 POWER SUPPLY TOPOLOGY

The IPS are off-line and have a 16-kHz H-bridge inverter driving a step down class H (220°C) transformer followed by a high-frequency rectifier stage and two -40dB/decade low-pass filters. Units with 2.4kW to 4.8kW power ratings have 208VAC, 3-phase input, with efficiencies greater than 85%. All other higher power IPS have 480VAC, 3-phase inputs, presenting, at rated current, efficiencies greater than 90%, and power factors of 0.94. Fig. 2 shows their basic power topology. A resistive step-start system limits the inrush current during power on.

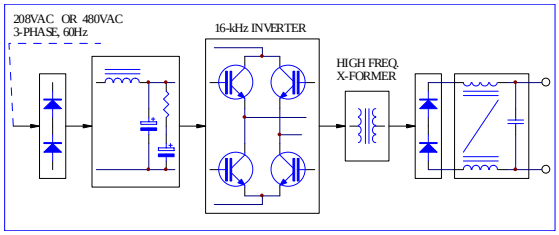

Figure 2: Intermediate PS Basic Power Topology.

4 PROCUREMENT ASPECTS

SSRL/PCD jointly specified [7] the minimum requirements, the topology and required performance, as well as the details on the interface with the control system. A twenty-year of continuous-operating lifetime was specified. In order to simulate the effects of transportation, every first article of each power rating was to be subjected to a 1 hour, non-operating sinusoidal vibration sweep from 10Hz to 100Hz at 2G.

A 19" standard rack mounted modular design was the best option. This allowed operation of an IPS similar to the PEP-II PS, thus reducing the required inventory of spare units. The IPS were designed to be series-connectable, thus keeping a rack-mounted modular design up to about 45kW of output power. All IPS are air cooled.

During the procurement process, several manufacturers participated in the bidding process. Technical and cost considerations dictated manufacturer selection. For the majority of the units the price was only US$ 0.50/W. Before fabrication authorization, the selected manufacturer conducted a design review with SSRL/PCD representatives. All outstanding issues were resolved as a prerequisite for fabrication release. Delivery of the units began in March 2003 and ended in August 2003.

In terms of mechanical arrangement, the IPS have a rack-mounted design based upon an NEMA1 chassis, and are standard 19" width, and 22" deep. Heights vary from 5.25" (3U), 8.75" (5U), to 14" (8U). Provision was made for easy access to replace power components.

Prior to shipping the IPS to SLAC, the manufacturer adjusted and tested the frequency response on the internal voltage control loop for all units. Requirements were for a 3-dB small-signal bandwidth greater than 1 kHz. Fig. 3 shows a typical step response to a +5% change in the voltage reference. In this figure, CH1 is the reference signal and CH2 is the measured output voltage in the transition from 31.5V to 33.75V.

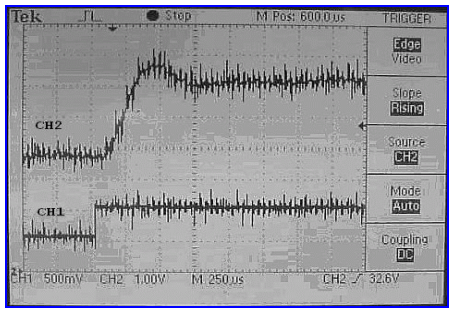

Figure 3: Step Response on a 45V 500A IPS.

PCD internally inspected every IPS for loose mechanical and electrical connections upon arrival. PCD then tested every IPS as an integral part of the destination system with appropriate interface controls. The manufacturer made long-term (24-hour) current stability and component temperature rise tests at the factory on one IPS of each voltage/current rating. PCD repeated the stability tests on-site.

5 COMMISSIONING

As shown in figure 1, the IPS current control loop stability is provided by a PI compensation circuit through the Bitbus controller. Values for the gain and time constants are adjusted during the field-testing phase.

Here follows a short description on the method used to measure the parameters for tuning the current control loop, once the IPS are connected to their final loads.

1. The system comprised by the IPS and its magnet load is left running for a burn-in time of approximately 30 minutes at the operating current, so that the load reaches its thermal stability.
2. At this point, we measure the load resistance R_0, and the IPS static voltage gain: K_{PS}.
3. By adding a small-signal 10-Hz sinusoidal wave to the reference to the IPS voltage loop, we measure both the AC component at the IPS output voltage and the corresponding load current ripple, to determine the load inductance L_0.
4. The output current transducer gain (K_{CT}) is given by the ratio of its output voltage/primary current.
5. Once the parameters L_0, R_0, K_{PS}, and K_{CT} have been determined, the PI controller parameters R_2 and C_2 are calculated and adjusted.

In order to provide for a 3dB small-signal bandwidth of 10Hz at the current control loop and assure a critically damped response, the Bitbus controller R_2C_2 compensation time is adjusted to be equal the time constant of the load circuit (L_0/R_0). Fig. 4 shows the basic block diagram for the current control loop system.

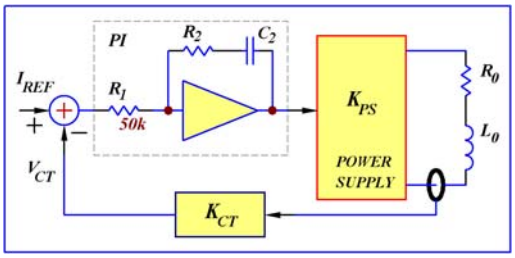

Figure 4: IPS current control loop block diagram.

Based on the above diagram, the PI controller transfer function (G_C) is given by:

$$G_C(s) = K_C \cdot \frac{1}{s} \cdot \frac{(sR_2C_2 + 1)}{s}; \qquad K_C \equiv \frac{1}{50k \cdot C_2}.$$

The load transfer function (G_L) is given by:

$$G_L(s) = K_L \cdot \frac{1}{\left(s\frac{L_0}{R_0} + 1\right)}; \qquad K_L \equiv \frac{1}{R_0}.$$

The overall open loop transfer function (G) will be:

$$G(s) = K \cdot \frac{1}{s} \cdot \frac{(sR_2C_2 + 1)}{1} \cdot \frac{1}{\left(s\frac{L_0}{R_0} + 1\right)},$$

where, by definition $K \equiv K_C \cdot K_{PS} \cdot K_L \cdot K_{CT}$.

Adjusting the time constant $R_2C_2 = L_0/R_0$ on the PI controller so as to cancel the pole created by the load, the open loop transfer function now becomes simply:

$$G(s) = K\frac{1}{s}$$

which yields this 1st order closed loop transfer function:

$$\frac{V_{CT}(s)}{I_{REF}(s)} = \frac{1}{\left(s\frac{1}{K} + 1\right)},$$

which exhibits a cut-off frequency: $2\pi f_c = K$.

Parameters on the PI controller can then be calculated as follows:

$$C_2 = \frac{1}{50k \cdot R_0 \cdot 2\pi f_c} \cdot K_{PS} \cdot K_{CT}; \qquad f_c = 10Hz.$$

$$R_2 = \frac{L_0}{R_0} \cdot \frac{1}{C_2}.$$

Fig. 5 is a typical plot on the final IPS current control loop frequency response.

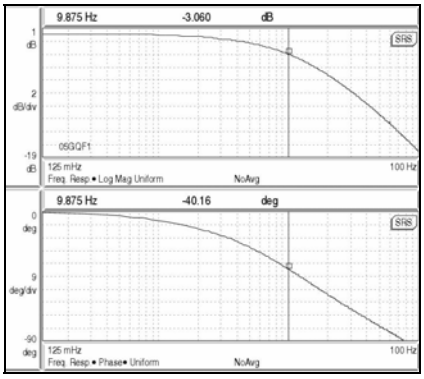

Figure 5: IPS typical current loop frequency response.

Diurnal stability measurements were repeated by PCD to verify that, indeed, the IPS performed within the specified 100ppm current deviation limit. Figure 6 presents a stability plot over more than an 11-hour period on one of the systems that employ two series-connected 45V - 500A IPS, working at a 300ADC current output. Measurements were taken every 2 seconds.

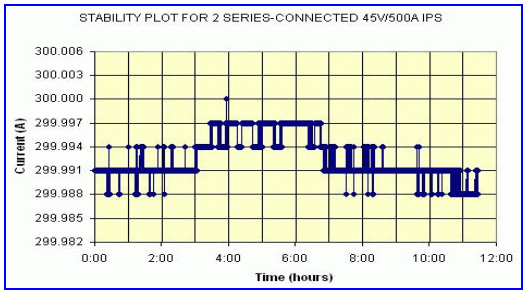

Figure 6: IPS stability measurements (1 div = 10ppm).

6 ACKNOWLEDGMENTS

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7 REFERENCES

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