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DESIGN CONSIDERATIONS FOR A SILICON/TUNGSTEN ELECTROMAGNETIC CALORIMETER FOR A LINEAR COLLIDER DETECTOR

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We discuss some issues relevant for a highly granular silicon-tungsten electromagnetic calorimeter, such as those currently being designed for a future linear collider detector. An important issue is the interplay between the silicon pixels and readout electronics. Here, we propose an integrated solution.

1. Introduction

Accurate jet reconstruction and excellent jet energy resolution are widely considered to be prerequisites for calorimeters at a future linear collider (LC) detector. Current designs[1] strive to push jet reconstruction to new levels of performance. An essential function of the electromagnetic calorimeter (ECal) in such designs is the separation of jet energy depositions due to photons from those due to charged particles. This calls for a dense, highly granular (in 3-d) ECal. A natural technology is alternating tungsten and silicon layers. Tungsten has a small Molière radius (9 mm) and the silicon can provide practically any transverse segmentation. Hence, one has the possibility of providing a high-quality image of the energy depositions.

Such a silicon-tungsten system would have $\sim 10^8$ silicon channels (pixels). Clearly, this calls for a compact, economical readout. In this brief report, we introduce a scheme for an integrated front end readout of a silicon-tungsten ECal. It is discussed in the context of the SD detector concept for the NLC, although it may in part be applicable elsewhere.

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2. Silicon and Readout Configuration

Since we are still far from a final technical detector design, the current SD design concept[2] should be considered fluid, the parameters being educated guesses based on existing simulation studies. Both barrel and endcap of the SD ECal consist of 30 longitudinal layers each of tungsten and silicon. The tungsten layers have thickness $t_W = 2.5$ mm ($\approx 0.7X_0$). The interleaved readout layers are also set to $t_g = 2.5$ mm thickness, comprised of 0.3 mm of silicon, 2 mm of (G10) motherboard, and a small air gap. The transverse segmentation of the silicon is 5 mm $\times$ 5 mm. With this segmentation, the number of detector pixels to be read out is about 50 million. We may expect the cost of these relatively simple silicon detectors (compared to strip trackers) to be less than \$2 per cm^2 by the time they are purchased in quantity for a LC detector, making a silicon-tungsten ECal feasible. But we also have to provide a simple, rational electro-mechanical detector and readout configuration. So to control cost and complexity, we seek an integrated configuration, where one channel of electronics serves a large number of pixels, and the electronics is compatible with the detector mechanical structure.

To reduce cost, we start with the largest silicon wafer readily available, which for now we assume to be of 6 inch diameter. Figure 1 depicts the central region of a possible detector on such a wafer. The hexagonal silicon pixels are 5 mm across, giving about 1000 pixels per 6 inch wafer. Metallization on the wafer connects the pixels to an array of bump bonding pads. A single 1000 channel readout chip is bump bonded to this array.

Figure 2 provides a cross-sectional view of the connections between the wafer metallization, the readout chip, and a G10 motherboard. Only ~ 10 lines are required on the motherboard per chip – power, silicon bias, a multiplexed digital output, and various control lines. We assume these connections are wire bonds. An important design consideration is the minimization of the readout gap, since the effective Molière radius of the ECal is $R_M^W(1 + (t_g/t_W))$, where $R_M^W \approx 9$ mm is for tungsten only.

The bump bonding procedure has become rather standard in recent years for pixellized detectors in high energy physics. The relatively large pixel size for our application allows for a relaxed bump bond pitch of ~ 250 μm, roughly an order of magnitude from current limits. In our case, the pitch is driven more by the area required by the readout chip, assuming 0.25 μm technology.

Thermal management of the detector is critically important because the electronics are embedded in the calorimeter in this approach. The best arrangement (for minimizing dead spaces and gaps) would be a fixed temperature heat sink at one edge of the ECal structure, and conduction cooling through

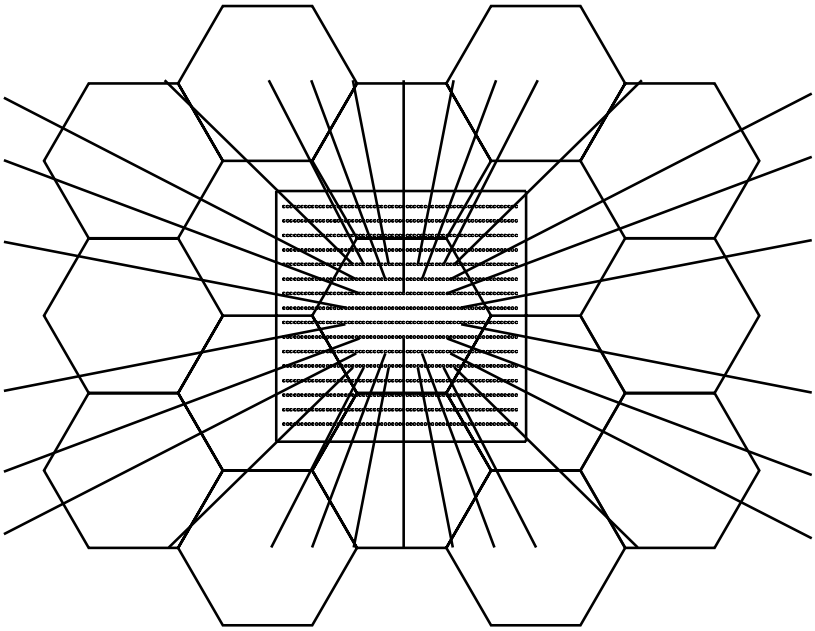

Figure 1. The center of one 1000-pixel silicon wafer showing the bump bond array at the center for the single readout chip. A few representative traces from pixels to the bump bond array are shown.

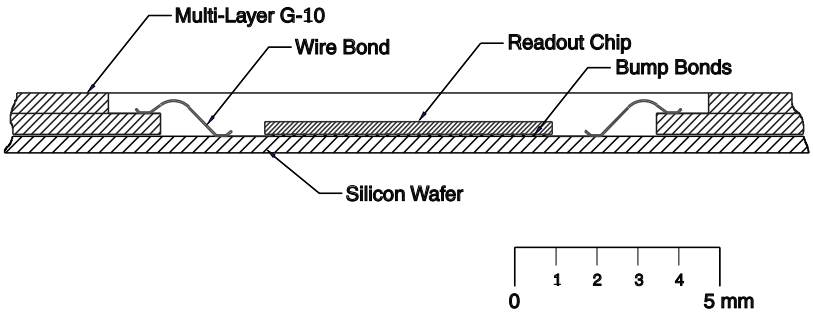

Figure 2. Cross-sectional view in the vicinity of the readout chip.

each layer to this heat sink. Thus the maximum thermal path would be about 1 meter. The conduction layer might be a thick copper ground plane in the G10 motherboard, or even a separate copper layer approximately 1 mm thick. This approach requires very aggressive control of the average power of the read out chips. The small accelerator duty cycle at a linear collider plays an important role here, allowing a large average power reduction if power pulsing of

electronics is employed. For NLC, if the turn on transients can be managed, then power pulsing should reduce the front end power by a factor of 1000. For the TESLA LC design, the duty cycle is an order of magnitude larger, possibly requiring more elaborate cooling[3].

We use the charge amplifier of the GLAST tracker[5] as an existence proof of an applicable low noise, low power front end design. Assuming the back end power can be made small compared to the preamps, a full chip at NLC would average about 2 mW. We estimate that this power would cause $\Delta T \approx 1°$C using a 6 oz copper ground plane in the G10. This should be fine, as would another factor of 2 or 3 in the power. However, achieving these levels for the average power while keeping the rather high performance standards will be a fundamental engineering challenge.

3. Dynamic Range and Resolution Requirements

Each ECal pixel must be sensitive to a large dynamic range, from MIPs to Bhabha electrons at the full beam energy. We have employed an EGS simulation which incorporates[4] the subtleties in simulating thin silicon sampling layers to evaluate this. We find that the ratio of 500 GeV Bhabha to MIP is at most 2000 for pixels near shower maximum. Because of the exponential transverse falloff of shower energy with distance, using smaller pixels does not decrease the dynamic range significantly. This is illustrated in Figure 3. Again using the GLAST chips as an example, the noise would be ≈ 300 rms electrons.

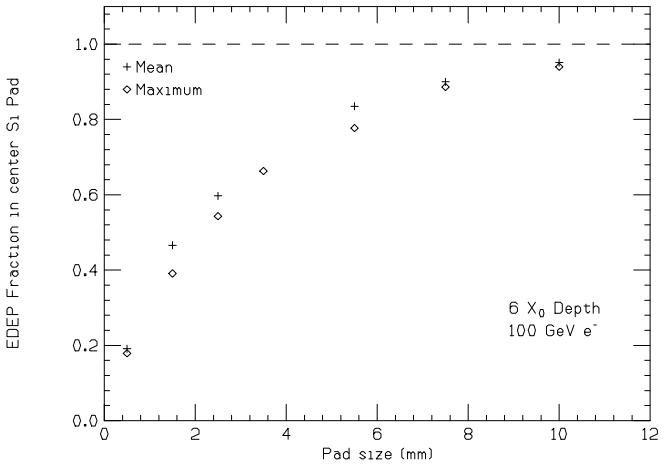

Figure 3. Energy deposition in the central pixel of a silicon layer at shower maximum, expressed as a fraction of the deposited energy in the entire layer, as a function of the pixel size (in mm). Based on an EGS4 simulation with 100 GeV incident electrons.

The requirements for an excellent S/N for MIPs and the large dynamic range leads to a readout element with a two-gain analog stage followed by a multiplexer and 12-bit ADC, effectively providing two overlapping 12-bit ranges. It may be possible to go to fewer than 12 bits with further study. A schematic of a front end electronics channel is shown in Figure 4.

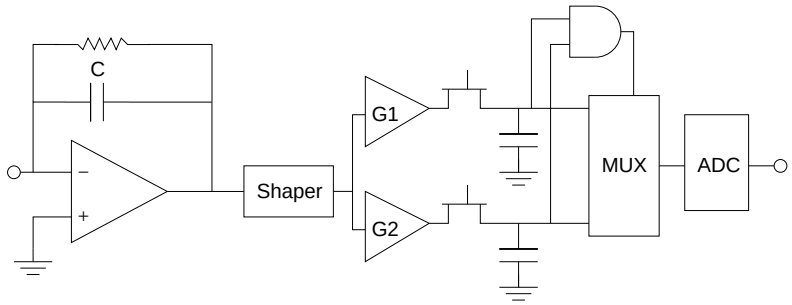

Figure 4. Schematic front end electronics channel. We anticipate $C \approx 10$ pF and $G1/G2 \approx 15$ for a 12-bit ADC. An additional capacitor $\approx C$ will be required for calibration.

4. Plans

We wish to develop this design in staged prototypes, starting with single chips and wafers to demonstrate the integration approach, and leading to construction of a full-depth module for testing in a beam of both electrons/photons and hadrons.

Acknowledgements

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