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CAMAC MAGNETOSTRICTIVE READOUT SYSTEM USING SCHOTTKY MEMORIES*

Boris Bertolucci

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

A magnetostrictive readout modular system using fast TTL memories is described in this paper. The main characteristics of this system are its expandability, its simple logic configuration, its high recording speed and its capacity of 15 sparks/wand with a word length of 16 bits per spark.

I. Introduction

A CAMAC magnetostrictive readout system using fast TTL memories has been designed and built to be used with the spark chamber in the magnetic detector of the Stanford positron-electron asymmetric ring (SPEAR) at SLAC. The overall system (Fig. 1), for this particular application, includes 164 wand amplifiers and zero crossing detectors, 41 4-channel time digitizer ("ANNA") modules, 2 crate controllers and a processor. The modular configuration of the system, however, permits expansion of the number of channels, the only restriction being the 7 crate limitation of the particular crate controller used.

An external 20 MHz crystal clock is distributed to all the modules and each module has its own synchronous counter, so no fast data signals transfer occurs between the modules. A fast independent 16 bit memory for each wand is used; this results in a simpler, more direct encoding, and more straightforward readout than a previously reported large memory system.[1]

When an event triggers the spark chamber, a start signal is generated enabling the modules to accept data. Two fiducial sparks on each wand, in addition to sparks due to particle tracks, are provided for time reference (zero time) and are registered into the memories as the first and last data word.

The system is completed by a test generator which, through the bridged TEST input, controls the correct functioning of the memories, and an x-y display scope for test-reference purposes.

In this article only the time digitizer module and the processor will be discussed.

II. The Time Digitizer ("ANNA")

The time digitizer (Fig. 2) is a CAMAC 4-channel single width module, with bridging clock, start and test inputs and 4 data inputs. All the readout functions utilize the standard CAMAC dataway. Each channel is capable of recording 15 sparks.

The 20 MHz clock, which is always running, is used to synchronize the input signals (start, data, test) and as a time base, when counted into the synchronous counter.

A start signal opens the clock gate enabling inputs and memories and allowing a 16 bit synchronous counter to start counting (time base). When a spark is detected in a wand, a Write (synchronous) signal transfers the content of the counter into a 16 × 16 bit fast memory (Intel P3101).

At the end of the cycle (synchronous counter overflow) an all-zeroes-word (last word) is written in the memories as a control for the Q response during readout. The clock gate is then closed and the inputs inhibited until the next start pulse. A 4 bit ripple counter is used to address the memory locations and it is incremented after each data input to accommodate many sparks. If overflow occurs (15 spark/wand) the corresponding input is gated off.

The digitizer furnishes also an X-line (Fig. 3) output that will be used by the processor to detect the presence of a module in the various bin locations during readout.

An important characteristic of this module is the fact that no buffer memory has been used between the synchronous counter and the memories; this reduces the hardware and simplifies the control system and, in conjunction with the high speed TTL memories used, data can be recorded at full clock speed.

Notice should be given to the fact that the least count at the clock rate of 20 MHz corresponds to a distance of .25 mm in space from a wand velocity of 5 mm/μsec.

The spark chamber wand system has a spark pair resolution of 2 mm, while the electronics could resolve a pair .25 mm apart that is 8 times better.

III. The Synchronous Counter

One of the most important parts for the correct operation of this system is the synchronous counter. On cascading two or more stages of Signetics 8284 synchronous counters the frequency of 20 MHz can be barely reached. This speed limitation is mainly determined by the Carry-Out output of the first stage, used to enable the following stages, that has a typical delay of 30 nsec from the clock pulse.

To speed up the counter, the CO output of the first stage must be anticipated. For this purpose (Fig. 4) two Schottky circuits (typical propagation delay: 5 nsec) have been used: a 3 input positive AND gate (74S11) and a JK flip-flop with a typical setup time of 3 nsec (74S112). We were able to run this configuration of the counter up to 35.3 MHz.

A timing diagram at 25 MHz is shown in Fig. 5. The values (in nsec) are the typical values according to Signetics "Digital 8000 series TTL/MS1." It can be easily noticed that while CO has already failed to set up the CE of the next stages, Q (74S112) gives a setup time of 35 nsec which is considerably more than the typical setup time required (15 nsec).

IV. The Processor

The processor (Fig. 6) is constructed in conventional chassis form with components connected by wire-wrap. It interfaces the branch highway to the Sigma 5 computer I/O and contains processing logic to generate one wire address in a 32 bit computer word and a D/A converter for oscilloscope display.

At the end of the cycle (3.3 msec after the start pulse) the processor reads out all the word counters, registers them into a 16 × 64 bit memory and calculates the total number of sparks registered during the event. This number is transferred, for reference, to the computer. After this first data word has been accepted, the processor, under computer control, sequentially reads all the memory locations that contain some information and packages them into a 32 bit (computer word) buffer memory along with the wand

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address. The read cycle ends when all the data memories have been transferred or when a computer memory overflow has flagged.

The processor is completed by error checking systems. During spark computation the system checks the presence of at least 2 words (fiducials) per wand and for word counter overflow and flags the failures. During readout the processor uses the X-line to detect the presence of an "ANNA" module in the crate, and skips over empty locations, and the Q-line to check if all the data from a particular wand has been read correctly. At the end of the readout cycle the scope displays the event automatically.

Figure 7 shows the timing diagram of the overall system operations and Fig. 8 the word format.

V. ANNA System Tester

In a system of this size and complexity it is important to have a convenient, reliable method of on-line testing. Of course some degree of overall testing is inherent in reading and verifying fiducials for each wand. However, separate routine testing of the readout electronics will further improve system operation, and will of course be invaluable in system debugging and maintenance in the event of failures. To this end a test input was included in each ANNA module which simply OR's the test signal into each of the four signal inputs.

A digital system tester is now being designed which generates test signals under computer or manual control to simulate an event. Thus it tests the ANNA modules, the crates, crate controllers, the processor, the scope display, the computer and its software, and cabling. Two modes of operation are available: 1) a multiple spark dynamic simulation mode, in which up to 15 simulated sparks are generated with a programmed starting point, but with a fixed separation of 400 nsec (8 clock pulses) and 2) a memory writing mode, in which an arbitrary pattern of 16 bits can be written into any memory location in ANNA. This facility is included primarily for memory exercise tests such as 101010... etc.

Verification is normally performed by the computer via readout of the processor, but it is expected that major errors can also be detected visually on the oscilloscope. This latter facility, together with manual operation of the tester, provides a self-contained overall system test facility.

VI. Acknowledgements

The author wishes to thank Dale Horelick for valuable discussions; Paul Arechiga for his greatly appreciated help in debugging and prototype work and Fred Rosche for his work on the scope display.

VII. Reference

1. R. G. Friday and K. O. Mauro, "New Digitizing and Memory System for Wire Spark Chambers," IEEE Trans. Nucl. Sci., Vol. NS-19, No. 1 (February 1972).

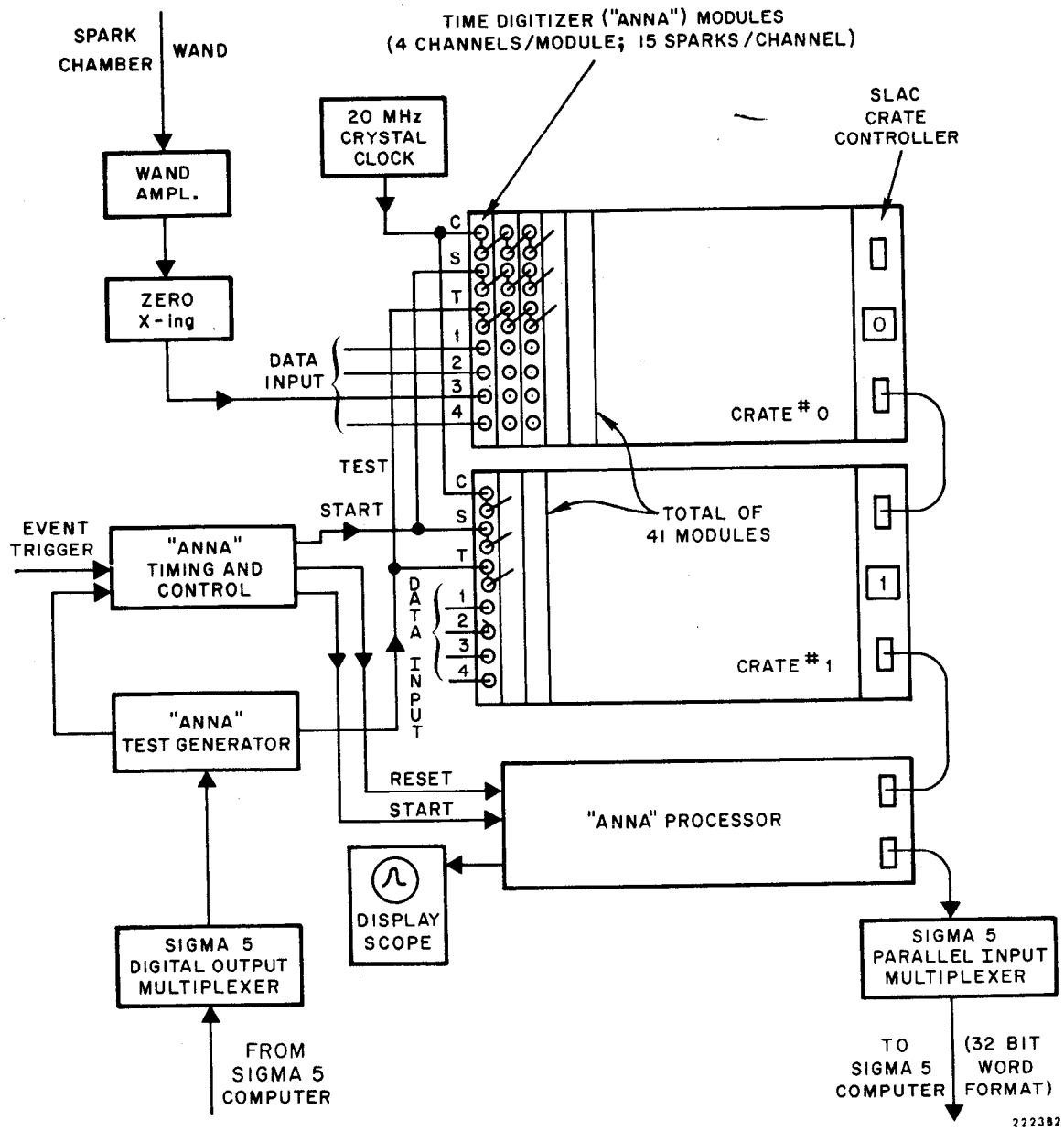

FIG. 1--Overall system.

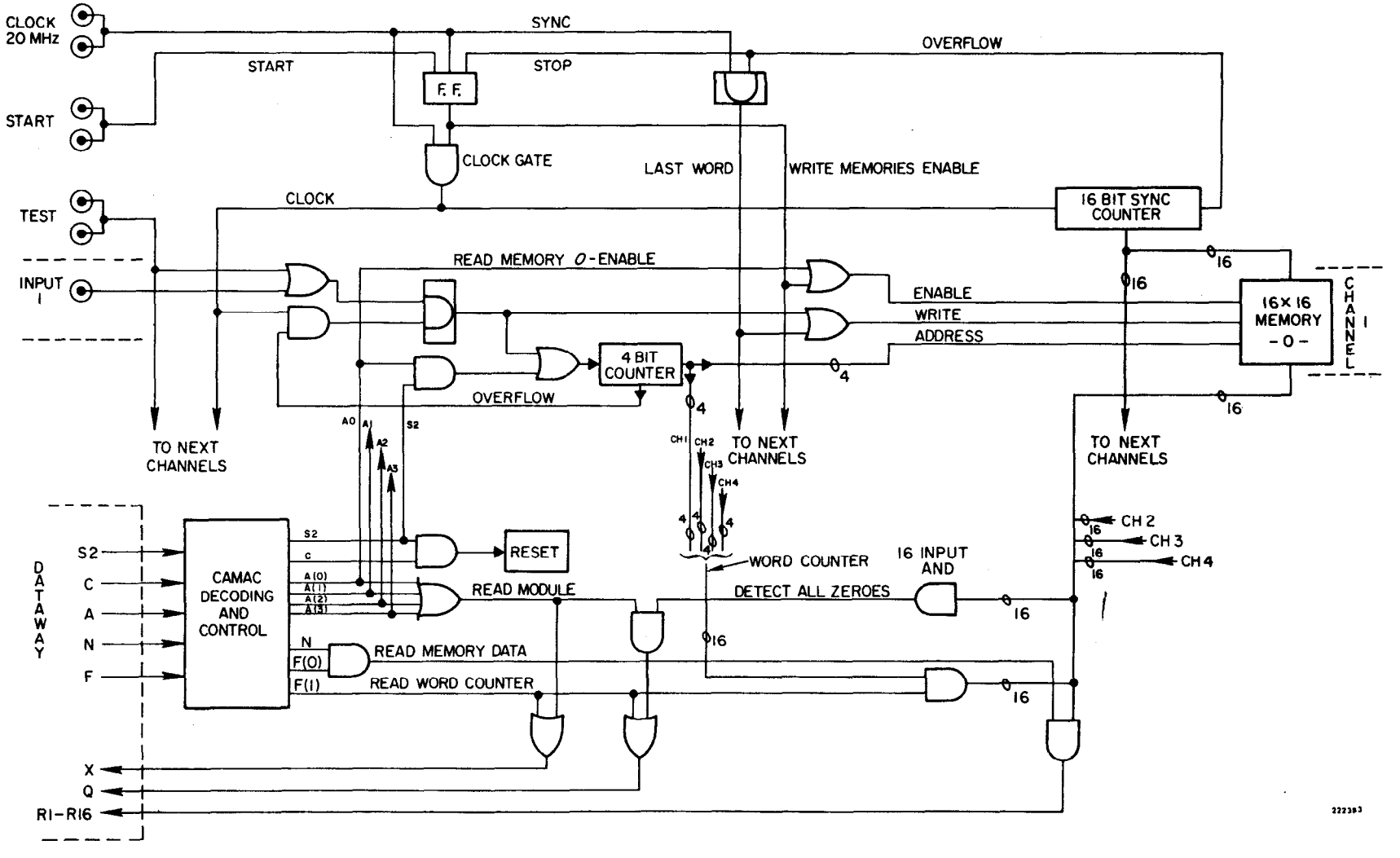

FIG. 2--Time digitizer.

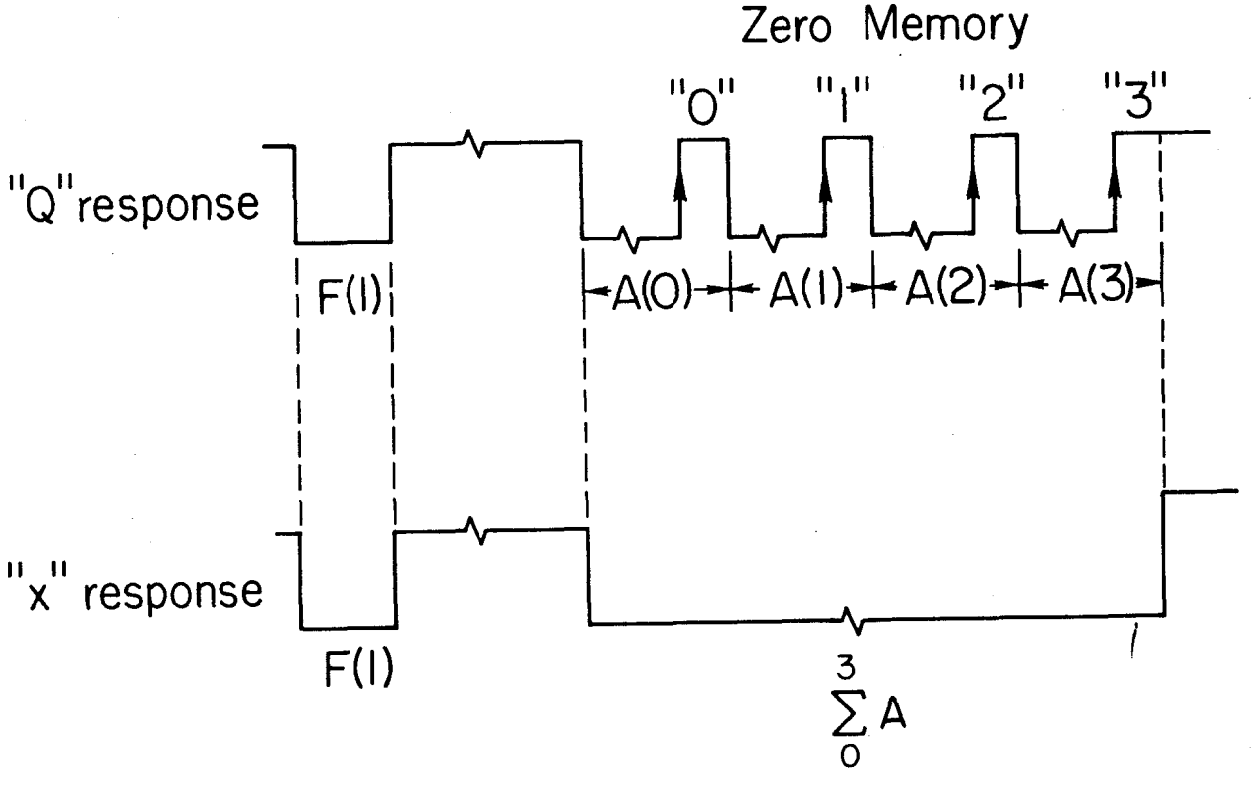

FIG. 3--Q and X response.

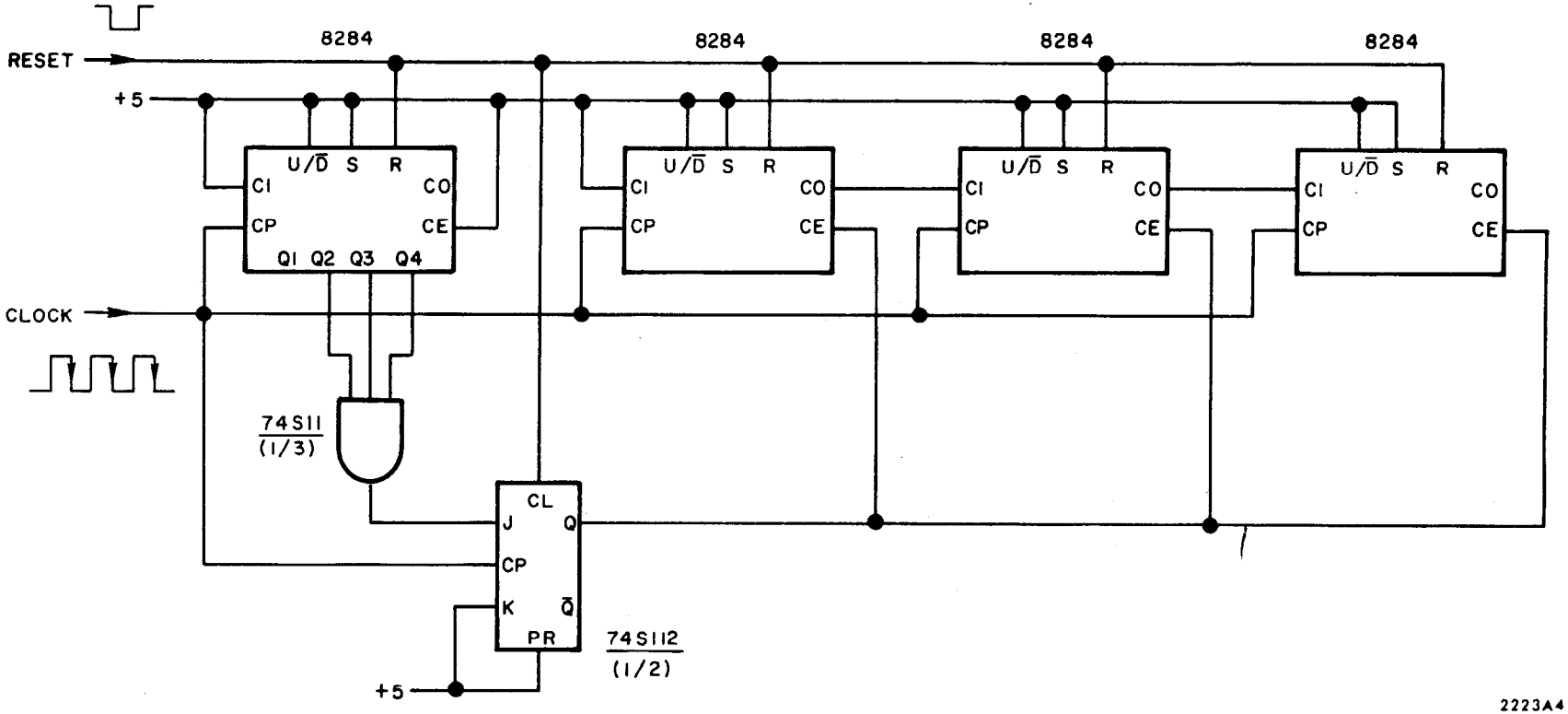

FIG. 4--Synchronous counter.

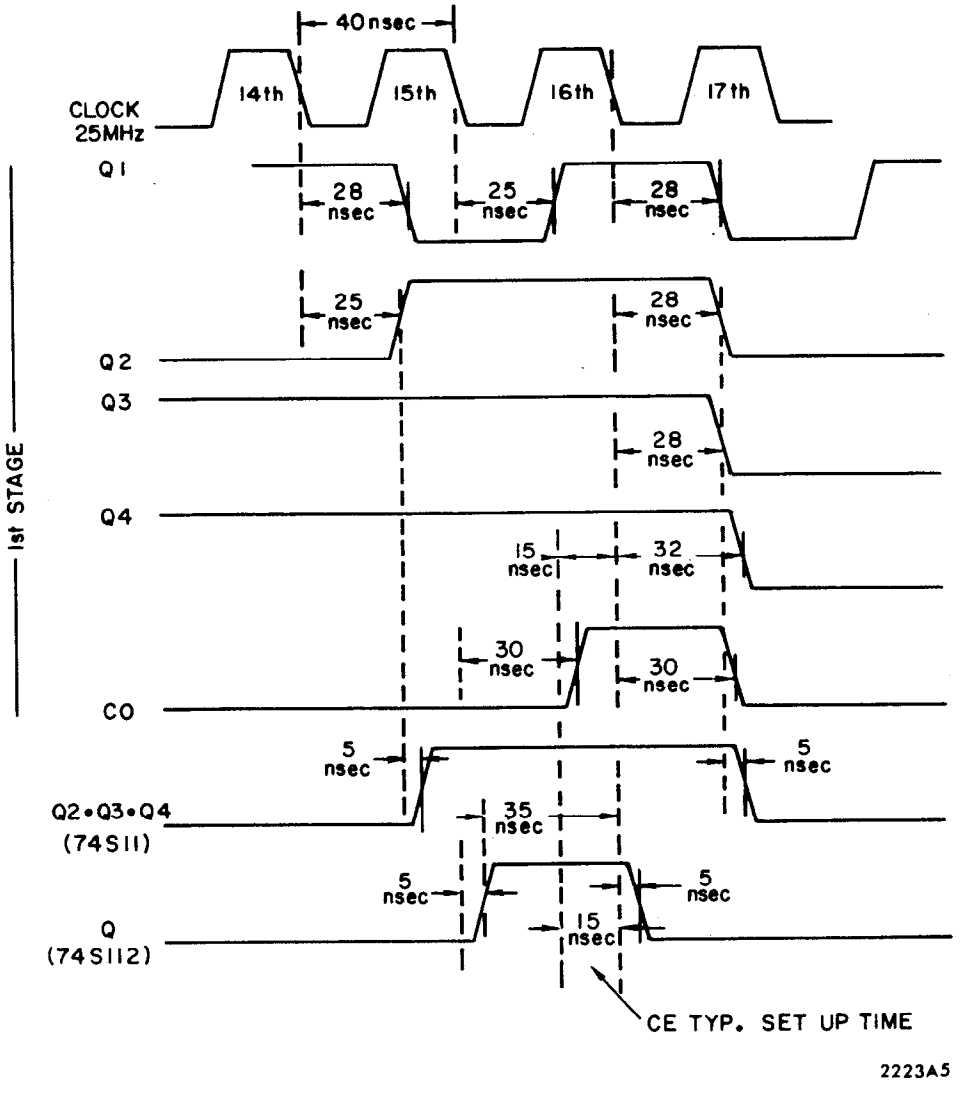

FIG. 5--Synchronous counter timing diagram.

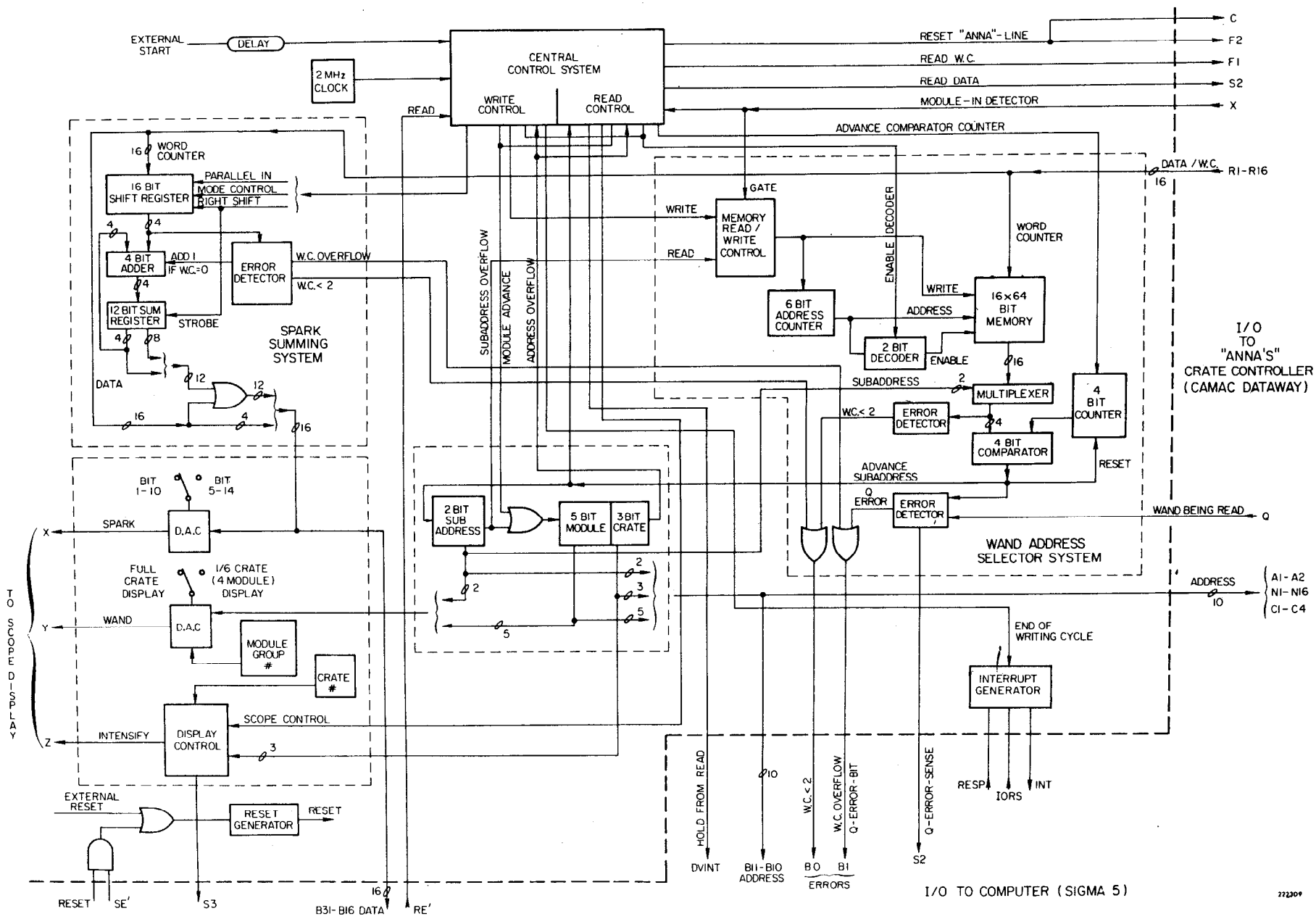

FIG. 6--Processor block diagram.

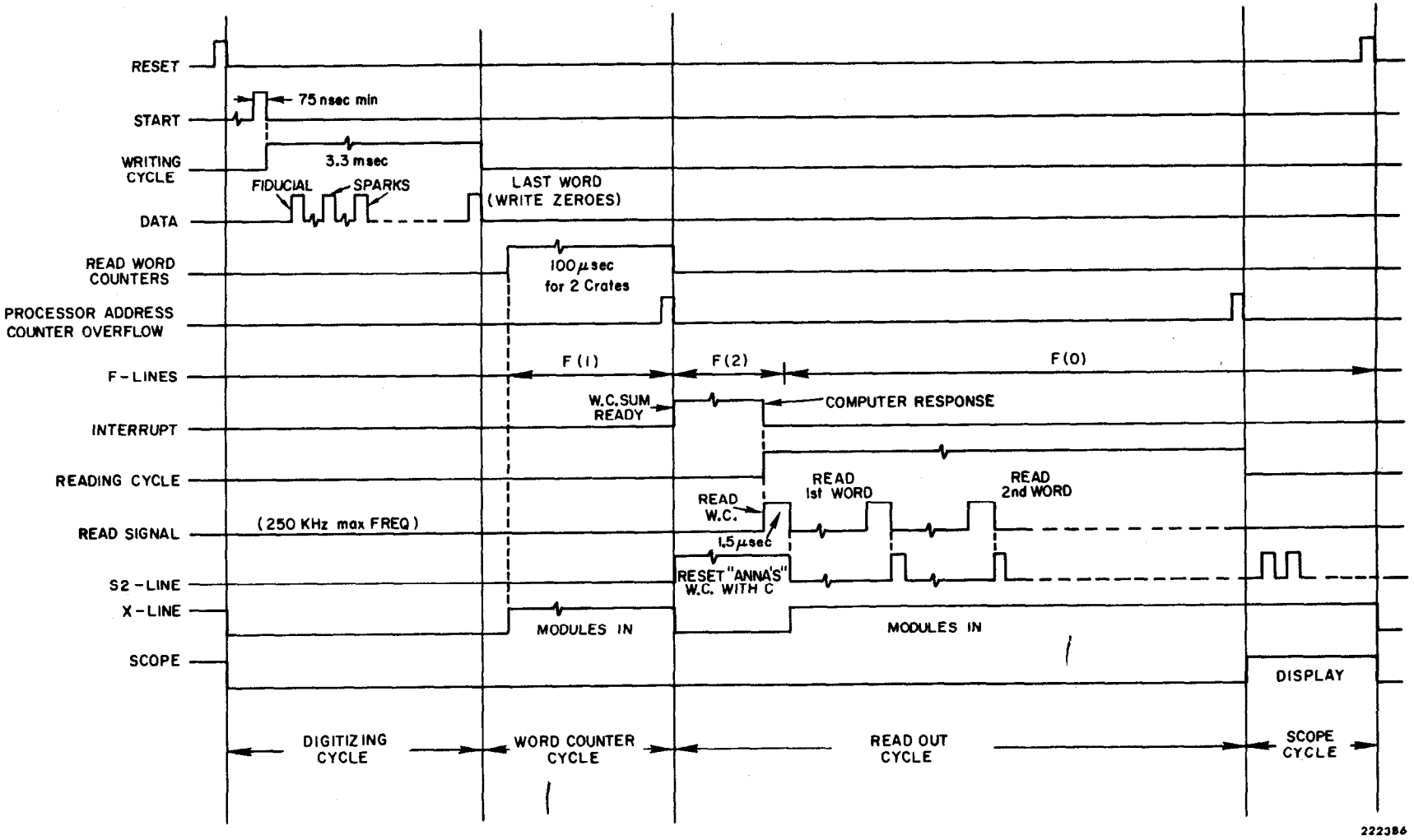

FIG. 7--Overall timing.

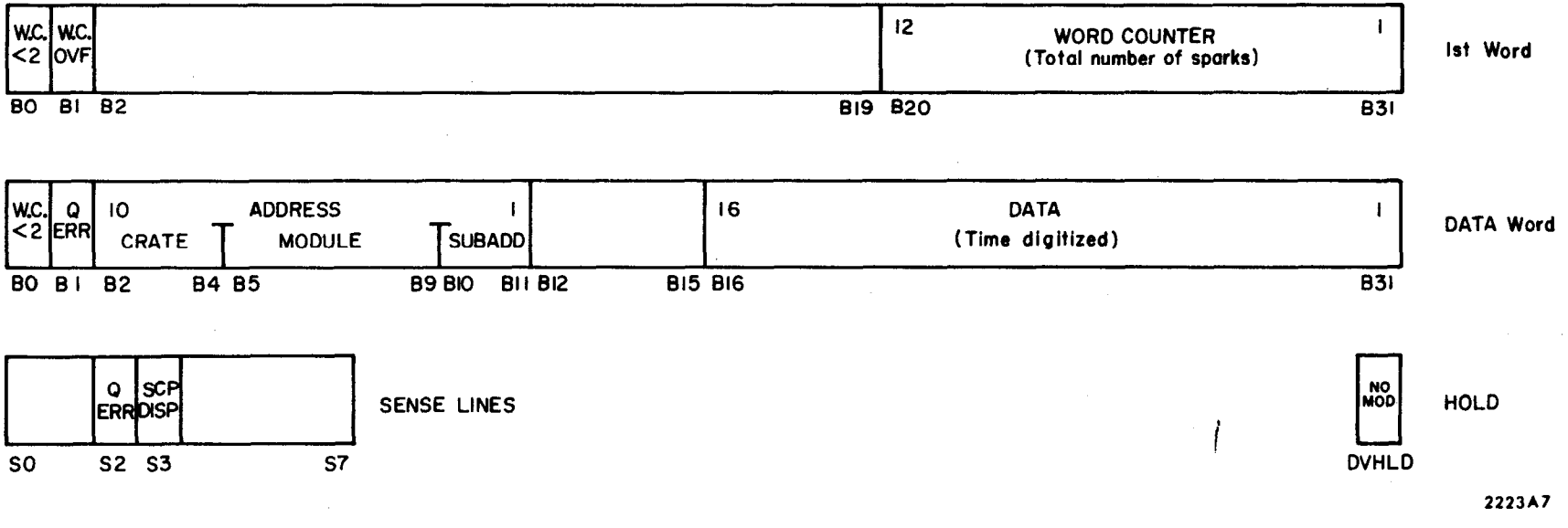

FIG. 8--Word format.