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A HYBRID INTEGRATED CIRCUIT FOR MULTIWIRE PROPORTIONAL CHAMBERS*

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1. Introduction

Since November 1970 an inter-Laboratory group has been supporting the development of a hybrid integrated circuit for multiwire proportional chambers. The details of the origin of this effort are given in an earlier publication.[1] The laboratories and personnel involved in continuing the support of this effort are NAL (M. Atac), LBL (H. Steiner and F. Kirsten), LAMPF (R. Martin and H. Thiessen), ANL (T. Droege), BNL (E. Platner), University of Chicago (T. Nunamaker), University of Illinois (L. Koester), and SLAC. These eight laboratories are purchasing prototype units for evaluation in order to stimulate development of an economical, versatile circuit.

To date, as reported earlier,[2] the major effort has centered around two companies, Fairchild Semiconductor of Mountain View, California, and Texas Instruments of Dallas, Texas. Although others have since become involved in developing hybrids, these more recent efforts will not be covered in this report.

With both the above named companies, an effort to obtain operational prototypes meeting a joint Laboratory specification,[3] i.e., 1 mV input sensitivity, matched controllable thresholds, matched controllable time delays, and parallel readout gated latches, has been continuing for the past 1-1/2 years. These efforts recently came to fruition when Fairchild Semiconductor delivered its first operational hybrid prototypes. These units have been given an initial evaluation at SLAC; a discussion of the device and its performance are the subject of the remainder of this paper.

2. General Specification

A block diagram and timing diagram of the functional circuit are shown in Figs. 1 and 2 respectively. The (revised) joint Laboratory specification is summarized in Table I.

In the original specification, packaging and separation of functions was not dictated, but various possible options were recognized.

3. Fairchild Hybrid

The Fairchild hybrid has been designed in two sections, a 4-channel amplifier section, designated SH0997, and a 4-channel delay-gated-latch section, designated SH1153.

The circuits are shown in Figs. 3 and 4; Fairchild's specifications are summarized in Tables II and III.

The package outline is shown in the photo of Fig. 5. For comparison, a pair of units representing 4 complete channels is shown beside a circuit board containing 4 discrete channels of the identical circuit. The form factor of the hybrid is improved by X4 or X5 over the discrete circuit; in addition, the thickness is such that individual units can be placed side by side on 8 mm centers (4 chamber wires spaced by 2 mm).

The initial prototypes were made with printed card edge contacts on 50 mil centers. This will mate with a Winchester CDXD2427 or equivalent connector (single row of 40 pins). An optional format to the card edge contacts is a row of wire pins which could mate directly with individual contact pins or solder holes.

The pin connections for the 2 units are given in Tables IV and V.

4. Tests and Results

An initial evaluation of most of the important parameters has been made on 3 - SH0997's and 2 - SH1153's. The basic tests include the following:

a. Amplifier time delay as a function of input amplitude
b. Sensitivity of threshold to power supply
c. Temperature sensitivity
d. Threshold tracking
e. Monostable delay tracking
f. Monostable temperature drift
g. Crosstalk for ± signals
h. Fast gating characteristics
i. Current requirements.

The important results are summarized below.

Typical waveshapes at various points are shown in the photos of Figs. 7 through 12b.

Figure 7 shows the fast OR output together with the direct output from a single channel. For this photo, the fast OR output is driving 50 Ω, ac coupled, and the direct output is loaded with a 500 Ω pullup.

Figure 8 shows the maximum crosstalk on an adjacent channel with a (-) overdrive of 40 dB over threshold. For a (+) signal of equal amplitude, there is no detectable crosstalk whatever.

Figure 9 shows the shape of the fast OR output and the monostable OR output, both driving 50 Ω. The latter output cannot quite drive a full TTL level into 50 Ω, which accounts for the roughly 3-volt amplitude.

Figure 10 shows the monostable output variation as a function of control voltage. Note that the maximum voltage applied was 10 V; whereas a control voltage of at least 14 volts is possible. The latter should correspond to a monostable delay of $\leq$ 250 ns.

Figures 11a, 11b, 12a, and 12b show the monostable matching between 4 channels in the 2 different devices, and at 2 different control voltages, 5.00 and 10.00 volts. Note that in fabrication the units were matched to 400 ns at a control voltage of 7.00 volts. Note also that for these measurements, the same front-end (SH0997) was used, with a constant input signal of -10 mV.

Figure 13 shows the time delay from input to fast OR output as a function of amplitude for a fixed threshold reference input of -100 mV, for all 12 channels of 3 units. The curves show the two extreme (high and low) channels. The reference setting of -100 mV theoretically corresponds to an input threshold setting of -1 mV; note however that most of the thresholds lie around 3 mV. Lowering the reference voltage to zero was seen to drop some of the thresholds to a stable -1 to -1.5 mV (see one point shown for illustration). If a +1 mV reference was applied, however, some channels became unstable, indicating that a zero threshold had indeed been reached. The pulse used for this test had a 5 ns risetime and was differentiated through a 10 pF series capacitor.

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The explanation for this behavior is that the individual channels are not as well nulled as they should be (the nulling requires a laser trimming operation), and there is a 1.5 to 2 mV spread in the actual thresholds. The reason for this mismatch is due primarily to inherently poor resolution in the particular laser used to trim the units; however, Fairchild is implementing a much better laser system and feels there will be no difficulty in guaranteeing the -1 mV minimum sensitivity specification in future units.

Figure 14 shows the result of sliding a 30 ns write gate over the trailing edge of the monostable and observing the direct latched outputs of all 8 channels of 2 units. For this test the same front end, signal level, and control voltages were used in both cases, while the logic units were interchanged. The noteworthy points are:

a. All the curves have the same width to within 1 ns
b. All curves for each unit are grouped to within about 5 ns
c. The two units have a group mismatch of about 5 ns
d. A single channel could be set with a minimum write gate pulse of approximately 10 ns. (This pulse had rise and fall time of 1 ns.)

Again, a similar explanation to that concerning the laser trimming of the front ends is in order, and future matching will be even better than shown. Note however that even though this measurement is made at a control voltage of 10.00 V, rather than at the matching point of 7.00 V (400 ns), the total delay variation is still within specifications. It should also be noted that the trimming was done observing the pulse width, rather than the total delay from monostable trigger to trailing edge; thus a small error due to differences in propagation delay may account for the group mismatch noted between the two units. (The matching procedure has been corrected for future operations.)

Other Measurements

Several additional measurements should be noted:

a. Threshold vs. reference voltage. At a setting of -1000 mV, corresponding to a threshold of -10 mV, all channels agreed to within 1 dB (~ 10%). At the other extreme, as shown in Fig. 13, the spread between all channels at -100 mV reference was 3-4 dB due to the mismatch discussed earlier. In general, if the low end matching is improved, it appears that all thresholds will track to within 1 dB, and that the control will be quite linear with control voltage.

b. Threshold vs. power supply voltage. The front-end power supplies were varied to -7.20, -6.80 for the -7 volts and to 5.20, 4.80 for the +5 volts. The worst change was a 2-3 dB decrease in threshold at 4.80 volts. The other variations caused changes of 1 or 2 dB. All channels behaved in a similar fashion and no instabilities were observed.

c. Temperature tests. One set of units (SH0997 No. 2 and SH1153 No. 4) were operated at 20°, 35° and 50°C. The maximum change in threshold on any channel over this range was -1 dB on channels 1 and 4. Channels 2 and 3 showed no change. For the monostable, channels 1 through 4 varied by +6, +6.5, +6 and +7 ns respectively over the range of 20 to 50°C, at an overall delay of 365 ns. This corresponds to +2% change in 30°C, well within the desired specification.

d. Power consumption. Both units together consume about 40 mA at -7 V and 230 mA at +5 V, or 356 mW per channel. The packages appear to run slightly warm to touch, but well within capabilities for a ceramic substrate. Note that any large system will have to handle heavy currents (e.g., 575 A at +5 V for 10,000 channels) and should provide for the movement of cooling air through densely packaged circuits. In view of such large currents, distribution systems will have to be well designed in order to assure good regulation at the device. It is particularly important that the analog section voltages, as well as the threshold and delay control voltages, be well regulated.

5. Problems Noted

Two problems were noted, neither of which appears difficult to correct. The first is that the SH0997 outputs were narrower than intended and had difficulty triggering the SH1153. This is apparently due to the shaper one-shot 30 pF capacitor coming out smaller than anticipated. The units were made to work for these tests by adding a 20 pF capacitor externally. This problem is being solved in future prototypes by correcting the size of the internal capacitor.

The second problem was that the Read gate did not function, such that the gated outputs were always present. This was traced to an internal bonding error and the problem has been corrected.

6. Cost

SLAC has initiated a Request for Proposal to Fairchild Semiconductor, as well as to several other companies, requesting formal price and delivery based on estimated quantities from a large group of Laboratories. This proposal gives firm prices valid for a 1-year period, which may be obtained by any Laboratory referencing the quotation. In large quantities, prices are under $7/channel. For purposes of comparison, a detailed cost estimate of the discrete version at the 10K channel level indicates a cost of $7-$8.65/channel, depending upon whether IC sockets are used.

It should be remembered when making comparisons of this sort that discrete boards must be checked, debugged and calibrated after fabrication; whereas the hybrids are individually tested and calibrated on the assembly line. The laser trimming operation accounts for a significant portion of the cost of the hybrid; hence the equally significant cost of testing and setting discrete boards should always be considered.

7. Summary and Conclusion

From the performance data measured, it appears that the SH0997 and SH1153 prototypes come very close to meeting all the significant points of the joint Laboratory specification. The major exception noted, that of non-ideal matching of thresholds, appears to be a question of procedure and not a fundamental limitation. This is reinforced by the fact that Fairchild is maintaining the 1 mV minimum sensitivity specification. Similarly, the problem of the fast OR width and the Read gate error appear easily soluble.

The operation of the SH1153 appears to meet all significant specifications. In both units, all signals are exceptionally clean and inter-channel crosstalk appears insignificant for either polarity of overdrive.

With the corrections noted, it appears that future units should meet or exceed all the major points of the joint Laboratory specifications for proportional wire chamber integrated circuits.

8. Acknowledgements

The hybrid development began as a joint Laboratory project and therefore many individuals have made important contributions. In addition to those Laboratory members mentioned in the Introduction, others deserving mention are F. Sauli of CERN, J.-L. Pellegrin and D. Horelick of SLAC, and R. Lanza of MIT. At Fairchild Semiconductor, the

principal contributors in the Hybrid Group are S. Smith, R. Lesea, and C. Puleston. Also deserving thanks are R. Ricks for his early contributions to the design; and G. Voget and J. Rapaich for their continuing support. The important work of O. Fleisher of SLAC's Purchasing Department is gratefully acknowledged. E. Cisneros of SLAC deserves special recognition for his assistance in evaluating and testing of circuits throughout the course of this project.

9. References

1. R. S. Larsen, "Interlaboratory Development of an Integrated Circuit for Multiwire Proportional Chambers," IEEE Trans. Nucl. Sci., NS-19, No. 1, p. 483ff (February 1972).
2. Ibid.
3. "Multiwire Proportional Chambers. Preliminary Specifications for a Monolithic Integration of the Wire Electronics," Lawrence Radiation Laboratory, Berkeley, California, November 20, 1970. (Revision 1, SLAC, September 1972).

TABLE I

Summary of Specification

I. Amplifier	
Input	-1 mV to -100 mV, negative; $T_F \sim 20$ ns, $T_R \sim 200$ ns
V_T	-1 mV to -10 mV ±10%; T.C. 1%/°C 0° to 70°C
Positive signals	Insensitive to +100 mV signals
Protection	No damage for 100 pF at ±5 kV through 2000 Ω
Gain	1 mV change gives full output
Fast out	Width 30 ± 10 ns, < 10 ns T_R, T_F, delay ≤ 40 ns ± 20%
II. Monostable Delay	
Output pulse	Adjustable 200 ns to 1 μs; T_R, $T_F \leq$ 10 ns
Propagation delay	$T_{PD} \leq$ 40 ns ± 20% from FAST out
Temperature coefficient of width	< ±.05%/°C
External R C trim	Optional
Power supply coefficient of width	≤ ±1% for ±10% change
Duty cycle	≤ 50%
III. Gated Latch	
Minimum write gate width	≤ 20 ns
Minimum coincidence curve	≤ 40 ns
IV. General	
Outputs must be wire OR-able	
No unusual cooling requirements	
Direct out and gated out must be TTL compatible	
Operating range 0° to 70°C	

TABLE II

SH0997 Specifications

Input Polarity:	Negative only. Positive pulses will be ignored.
Input Coupling:	External ac coupling is recommended. The minimum permissible dc resistance to ground from any input is 200 kΩ.
Threshold Range (external):	-1 mV minimum to -200 mV maximum.
Threshold Drift (internal):	±10 μV/°C typical; ±20 μV/°C maximum.
Input Impedance:	2.2 kΩ typical, 2 kΩ minimum.
Differential Input Sensitivity:	500 μV typical, 800 μV minimum.
Amplifier Gate Setup Time (delay to enable):	18 ns typical, 28 ns maximum.
Amplifier Gate Release Time (delay to inhibit):	14 ns typical, 24 ns maximum.
Amplifier Gate Fan-In:	4 standard TTL loads.

Propagation delay to line driver output:	
@ 2 mV Differential Input	@ 10 mV Differential Input
20 ns minimum	20 ns minimum
35 ns typical	30 ns typical
45 ns maximum	40 ns maximum
Propagation delay to channel output:	
@ 2 mV Differential Input	@ 10 mV Differential Input
15 ns minimum	15 ns minimum
33 ns typical	30 ns typical
43 ns maximum	38 ns maximum

Line Driver Output (any pulse input active):	.6 V maximum @ 110 mA sink.
Line Driver Output (all inputs inactive):	7.0 V maximum (externally applied).
Channel Outputs:	TTL Fan-out = 10, Voh = 5.0 V, typical, Vol = .5 V maximum
Line Driver Output Pulse Width[a]:	
15 ns minimum	
20 ns typical	Measured @ 1.0 V
25 ns maximum	
Channel Output Pulse Width[a]:	
5 ns minimum	
15 ns typical	Measured @ 1.0 V
25 ns maximum	

Power Input Requirements:

Name	Accuracy	Typical Current Drain
+5 Null	±10 mV	40 μA
-7 Null	±10 mV	40 μA
+5 Analog	±100 mV	105 mA
-7 Analog	±100 mV	40 mA
Threshold	±2% Relative	(50 kΩ)

Typical Power Consumption is 200 mW per channel, maximum 300 mW.

[a]Measured with 500 Ω pullup load on each channel output, and 47 Ω connected from the line driver output to +5 V.

TABLE III

SH1153 Specifications

Minimum Write Gate Pulse Width:	45 ns maximum, 25 ns typical
Write Gate Setup Time:	25 ns maximum, 15 ns typical
Write Gate Release Time:	2 ns maximum
Minimum Read Gate Pulse Width:	50 ns maximum
Read Gate Setup Time:	30 ns maximum
Read Gate Release Time:	20 ns maximum
Minimum Reset Pulse Width:	50 ns maximum, 25 ns typical
Reset Pulse Propagation Delay to Direct Outputs:	60 ns maximum
1-Shot Recovery Time	300 ns maximum
1-Shot Control Voltage (V_c) Range:	+2 minimum to +20 maximum
1-Shot Pulse Width Range:	.25 μs maximum to 1 μs minimum
Pulse Width at V_c = 7.000 V	392 minimum to 408 ns maximum
Temperature Coefficient of Pulse Width at V_c = 7.00 V:	.05%/°C typical, 0.1%/°C maximum

Power Input Requirements:

Name	Accuracy	Typical Current Drain
1-Shot Control Voltage	--	Input Impedance greater than 1.5 kΩ
+5 Digital	±250 mV	120 mA

Typical Power Consumption:	200 mW per channel
Maximum Power Consumption:	300 mW per channel

TABLE IV

SH0997 Pinouts

Pin Number	Pin Designation	Pin Number	Pin Designation
1	N/C	40	N/C
2	N/C	39	N/C
3	Line Dr. Out	38	N/C
4	Line Dr. Com	37	Ch 4 In
5	Amplifier Gate	36	N/C
6	Ch 1 Out	35	Ch 4 Com
7	Ch 2 Out	34	N/C
8	Ch 3 Out	33	N/C
9	Ch 4 Out	32	N/C
10	Digital Ground	31	Ch 3 In
11	Threshold Input	30	N/C
12	-7 null	29	Ch 3 Com
13	+5 null	28	N/C
14	+5 analog	27	N/C
15	-7 analog	26	N/C
16	Analog Ground	25	Ch 2 In
17	Ch 1 Com	24	N/C
18	N/C	23	Ch 2 Com
19	Ch 1 In	22	N/C
20	N/C	21	N/C

TABLE V

SH1153 Pinouts

Pin Number	Pin Designation	Pin Number	Pin Designation
1	Direct 2	40	Gnd
2	Direct 1	39	N/C
3	Gnd	38	Ch 1 In
4	Direct 4	37	N/C
5	Direct 3	36	N/C
6	Read	35	Ch 2 In
7	Gated 2	34	N/C
8	Gated 1	33	N/C
9	Gated 4	32	Gnd
10	Gated 3	31	N/C
11	Gnd	30	N/C
12	Reset	29	Ch 3 In
13	Gnd	28	N/C
14	Write	27	N/C
15	+5 Digital	26	Ch 4 In
16	N/C	25	Gnd
17	Mono Out	24	V_c
18	N/C	23	N/C
19	N/C	22	N/C
20	N/C	21	N/C

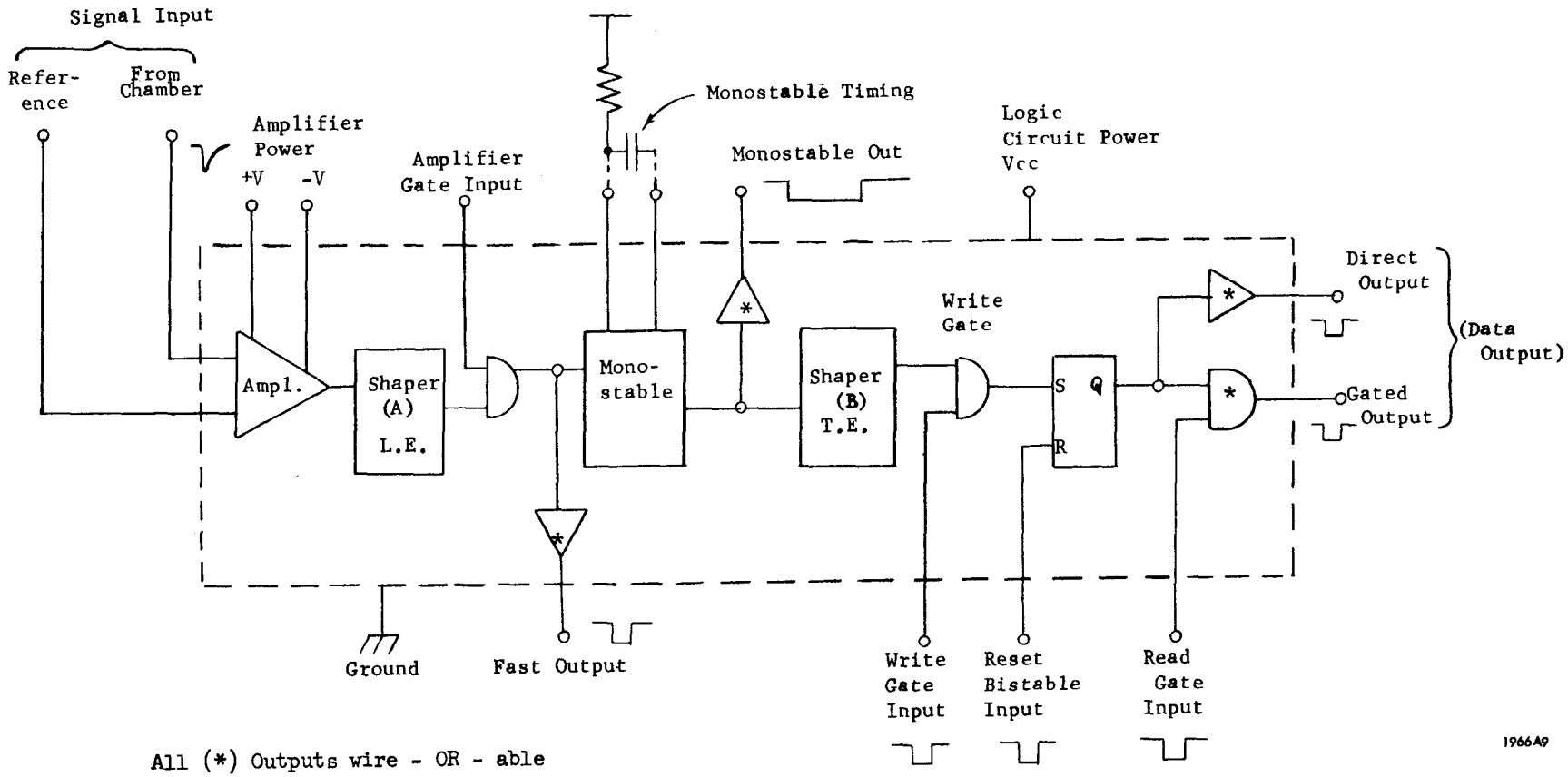


FIG. 1--Functional block diagram.

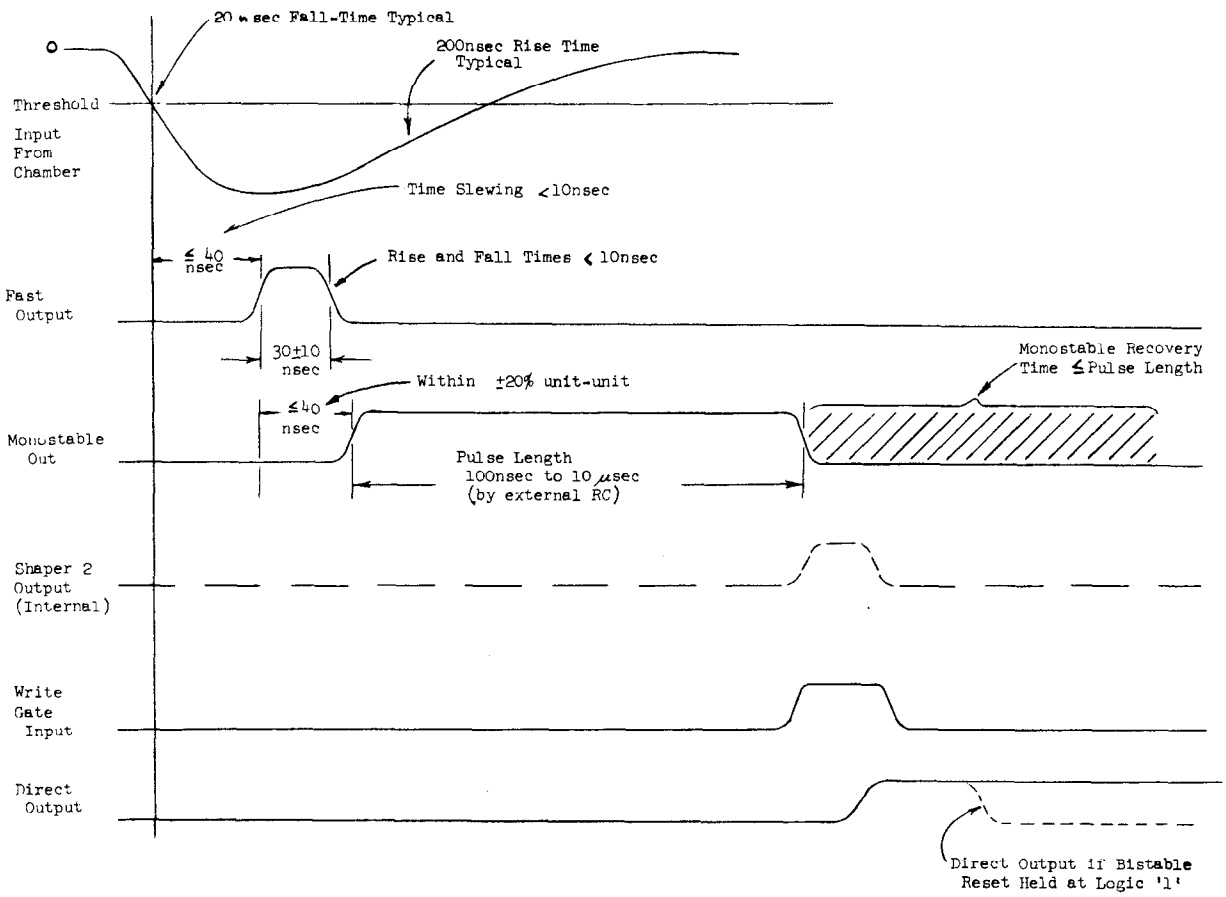
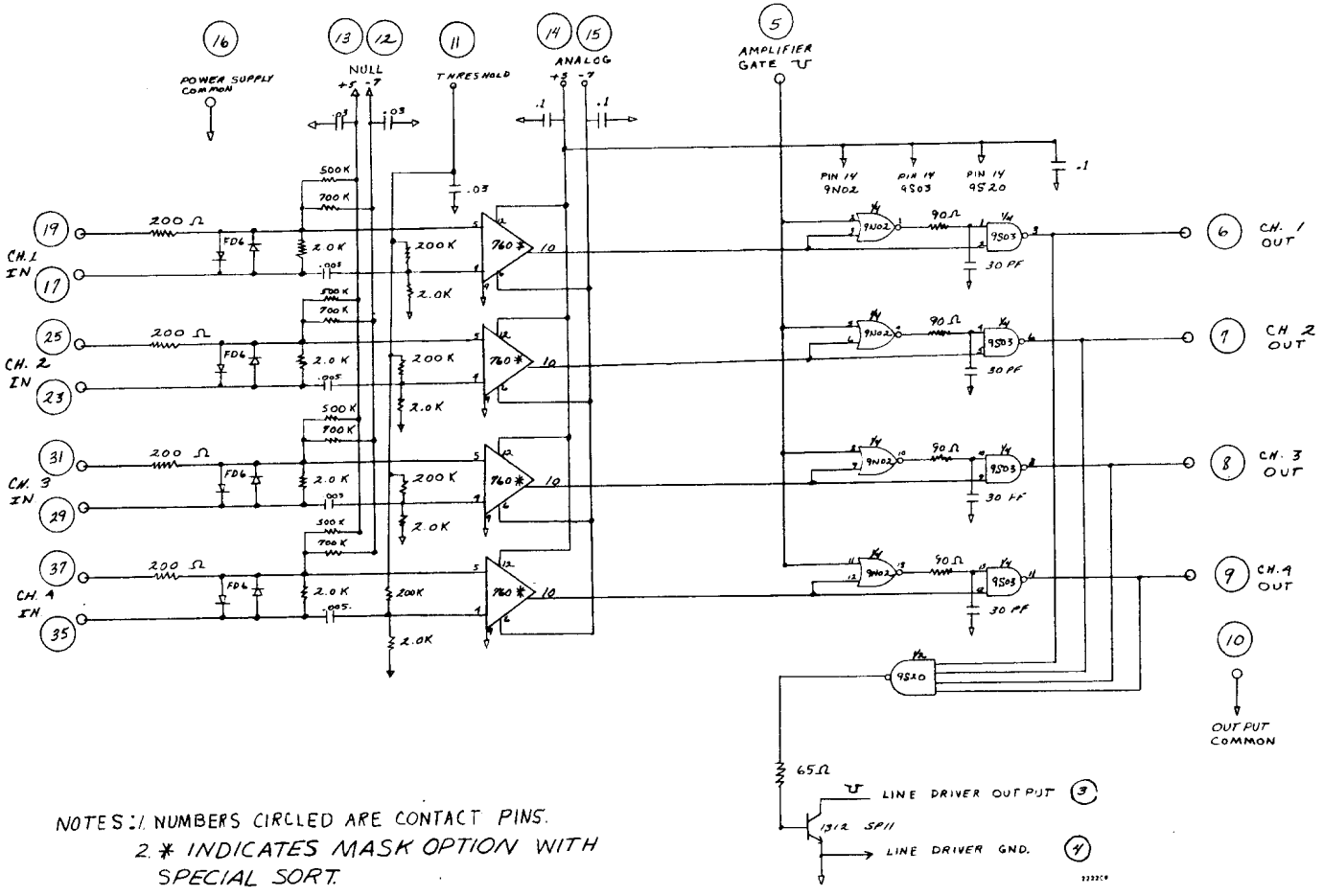
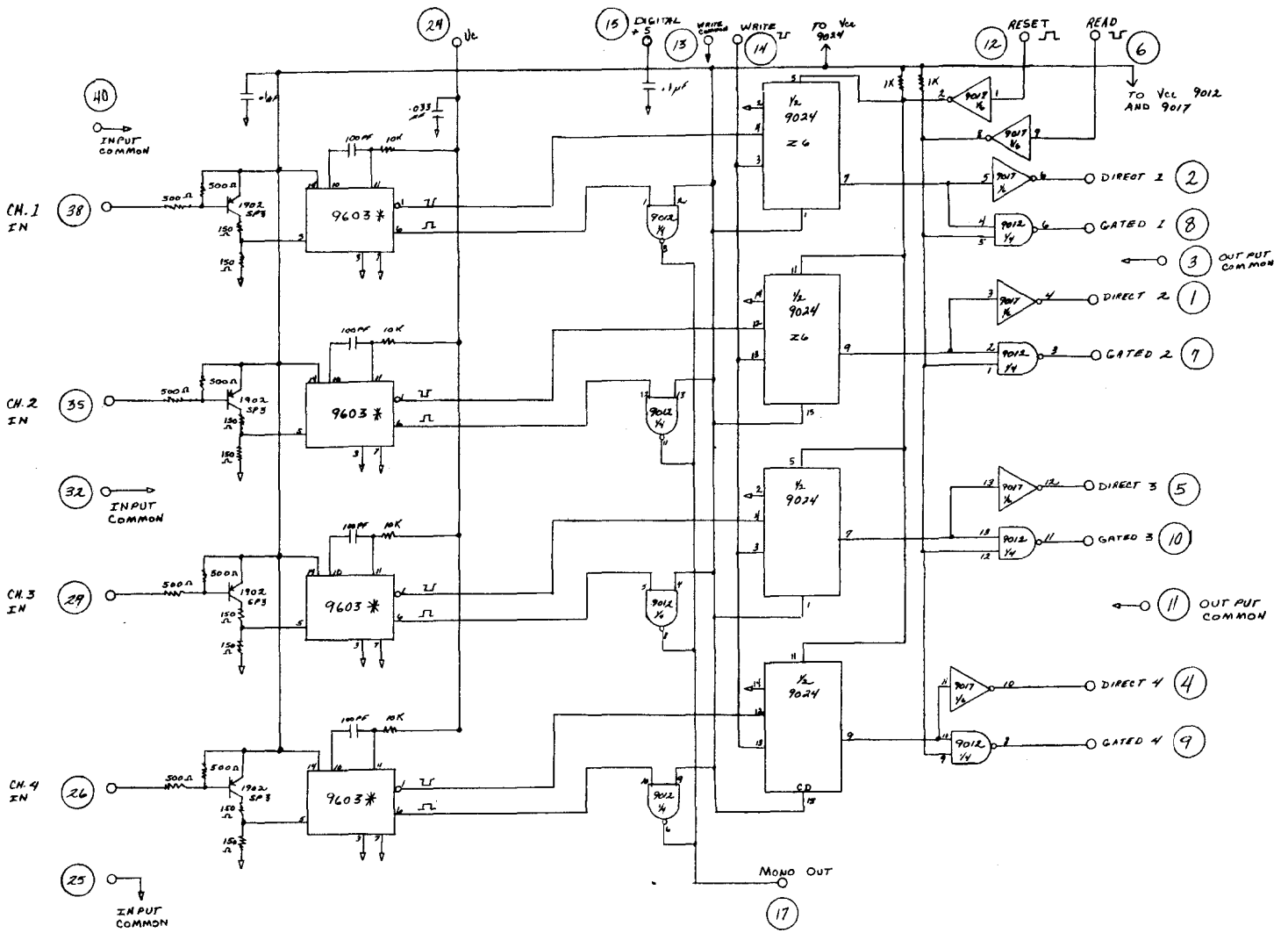


FIG. 2--Timing diagram.



NOTES: 1. NUMBERS CIRCLED ARE CONTACT PINS.
2. * INDICATES MASK OPTION WITH SPECIAL SORT.

FIG. 3--SH0997 circuit.



NOTES: 1. NUMBERS CIRCLED ARE CONTACT PINS.
2. * INDICATES SPECIAL SORT.

FIG. 4--SH1153 circuit.

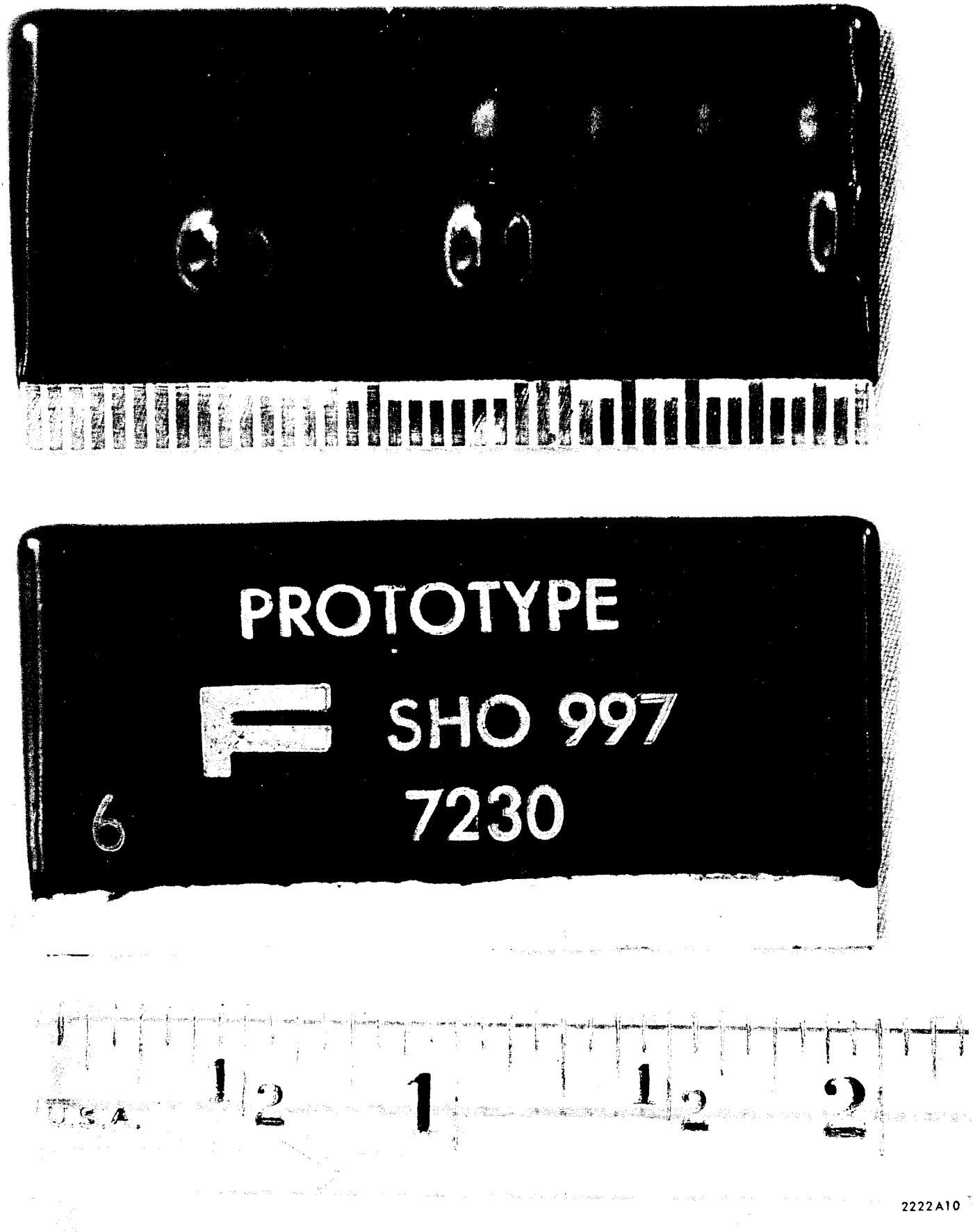


FIG. 5--Physical package.

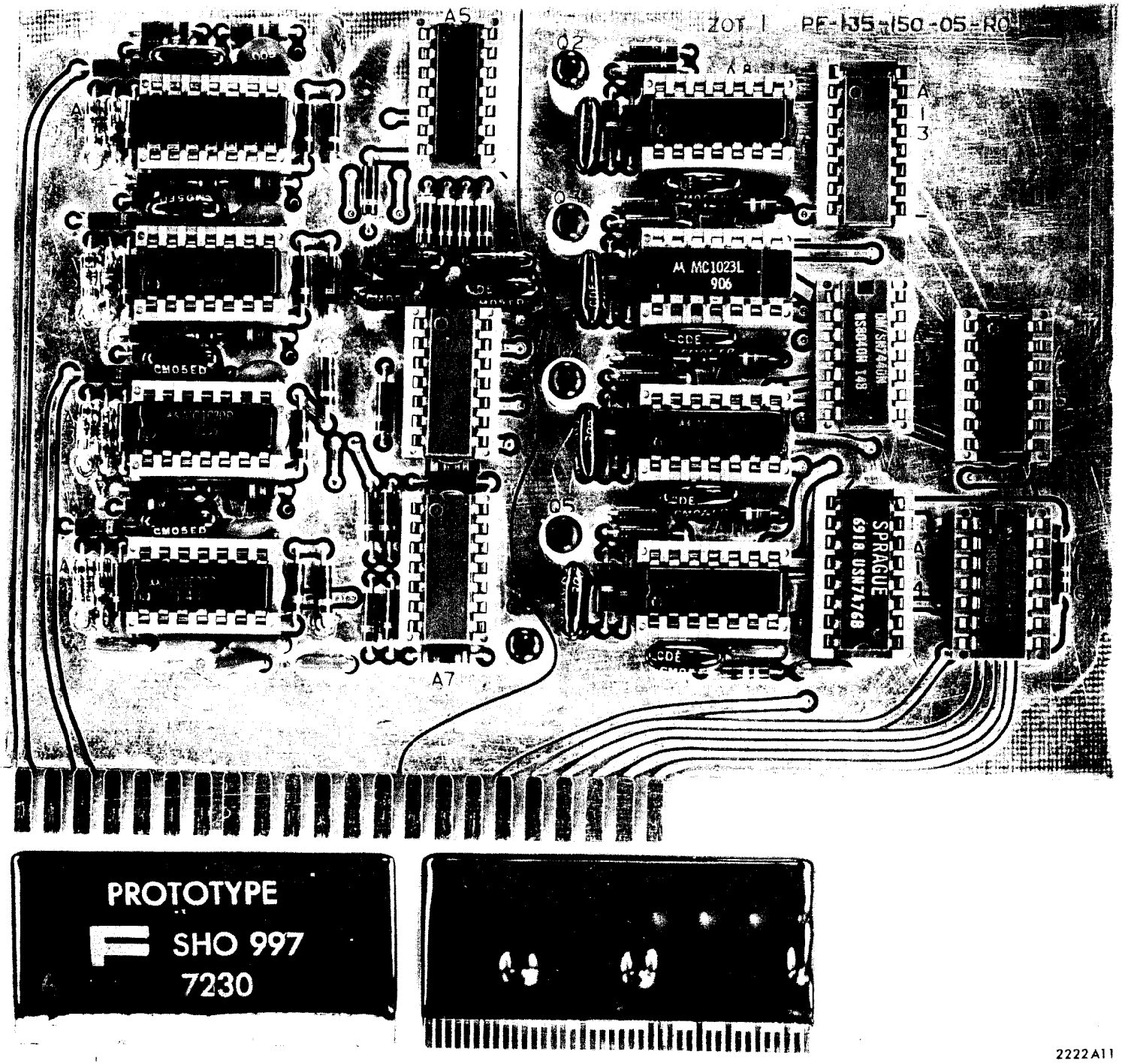
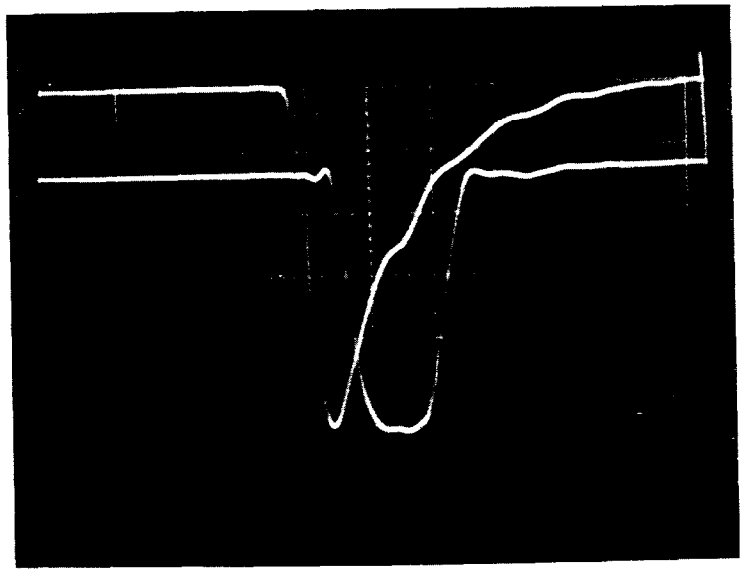
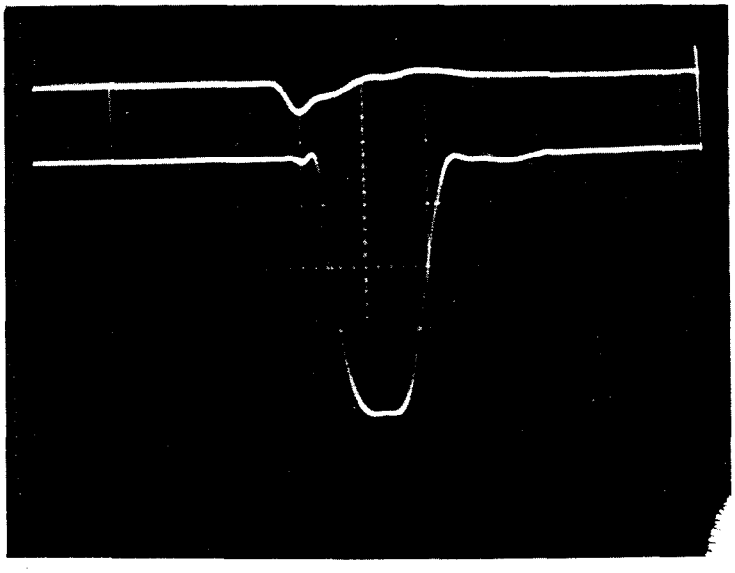


FIG. 6--Comparison with discrete circuit.



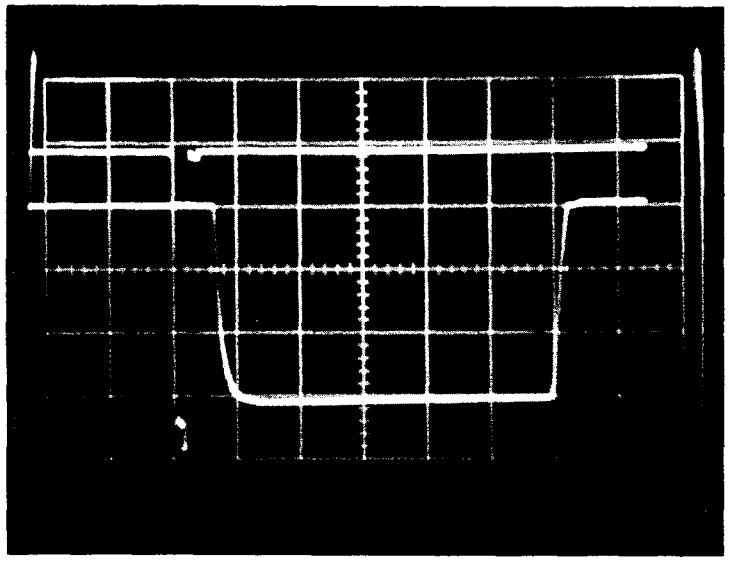
UPPER-DIRECT OUTPUT, SHO997 #6 CH4
LOWER-FAST OUTPUT (50Ω)
H = 10 nsec/cm V = 1V/cm 2222A2

FIG. 7--Fast OR and direct outputs.



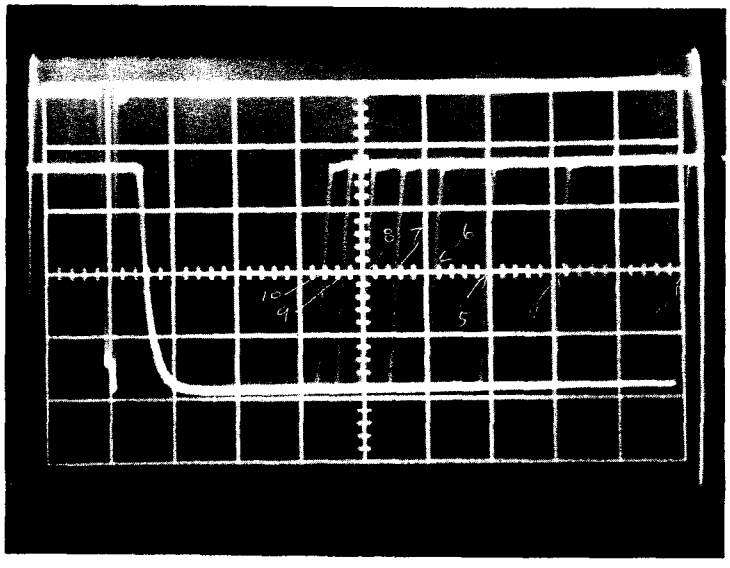
UPPER - MAXIMUM DIRECT OUT CROSSTALK,
SH0997 #6 CH 3
LOWER - FAST OUTPUT (50Ω) CH 4
H = 10 nsec/cm, V = 1 V/cm 2222A3

FIG. 8--Fast OR and crosstalk.



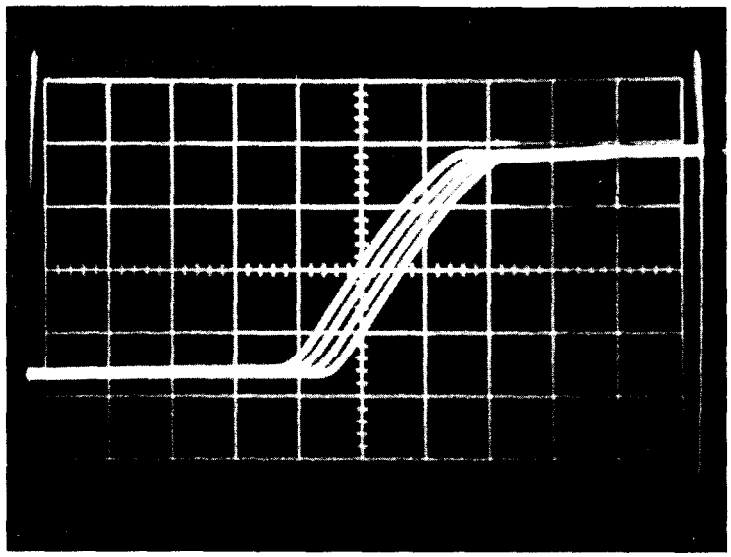
UPPER - FAST OUT (50Ω) SH0997 #7 CH 1
LOWER - MONOSTABLE OUT (50Ω) SH1153 #4 CH 1
H = 100 nsec/cm, V = 1 V/cm, V_C = 4.00V 2222A.4

FIG. 9--Fast OR and monostable outputs.

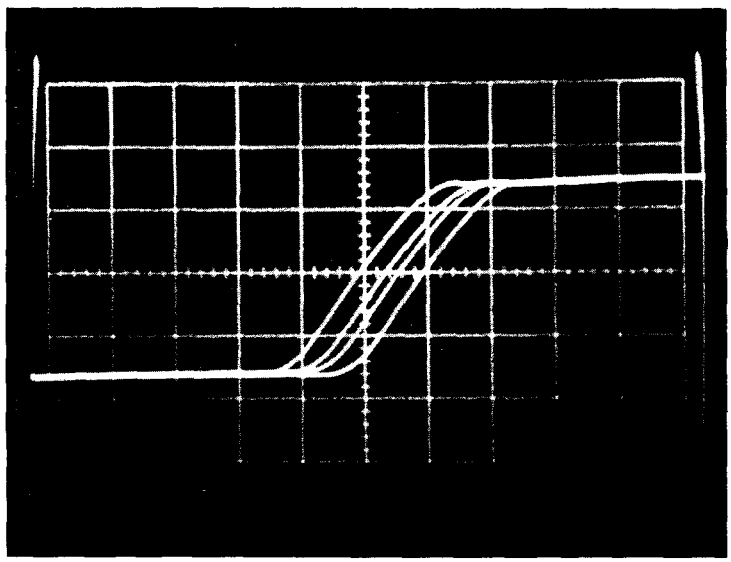


MONOSTABLE OUT vs CONTROL VOLTAGE
SH0997 #7, SH1153 #4 CH 1
H=100nsec/cm, V=1V/cm 2222A5

FIG. 10--Monostable output vs. control voltage.



MONOSTABLE TIMING AT V_C = 10.00V
(#7, #4) CH 1 - 4
SIGNAL IN - 10 mV Tpd = 365 nsec
H = 10 nsec/cm V = 1 V/cm

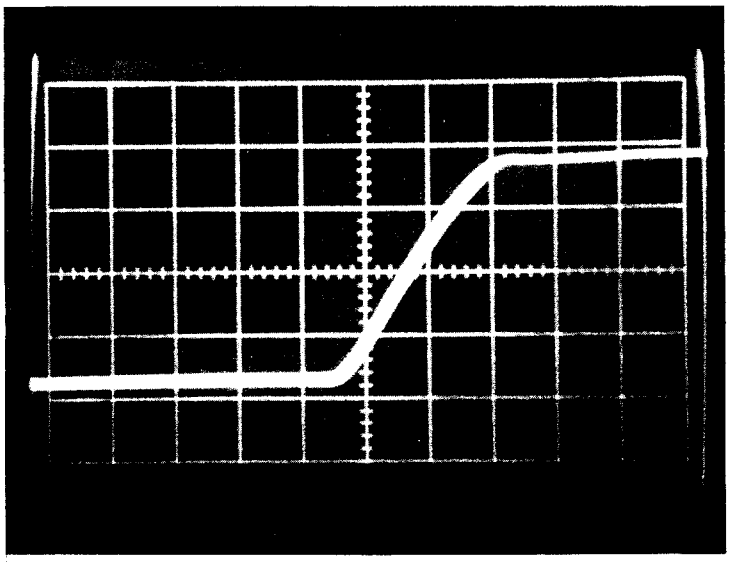


MONOSTABLE TIMING AT V_C = 5.00V
(#7, #4)
Tpd = 650 nsec

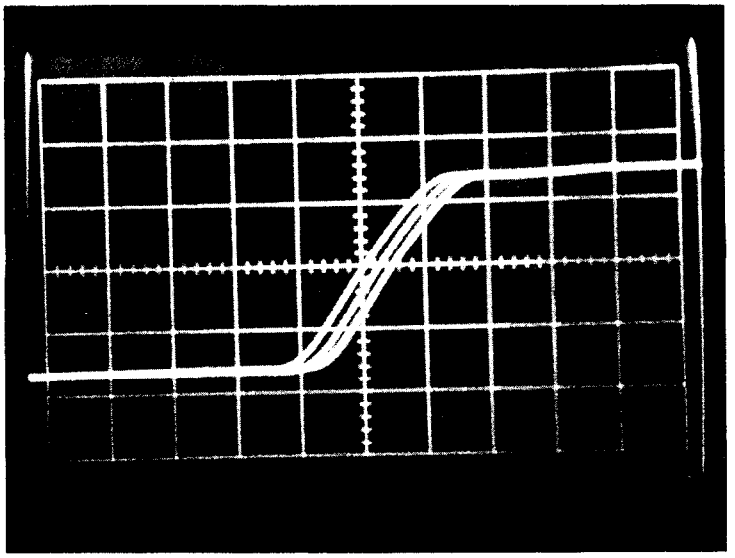
2222A6

FIG. 11a--Monostable timing waveforms.

FIG. 11b--Monostable timing waveforms.



MONOSTABLE TIMING AT V_C=10.00V
(#7, #1) CH 1-4
Tpd=365 nsec



MONOSTABLE TIMING AT V_C=5.00V
(#7, #1)
Tpd=650 nsec

2222A7

FIG. 12a--Monostable timing waveforms.

FIG. 12b--Monostable timing waveforms.

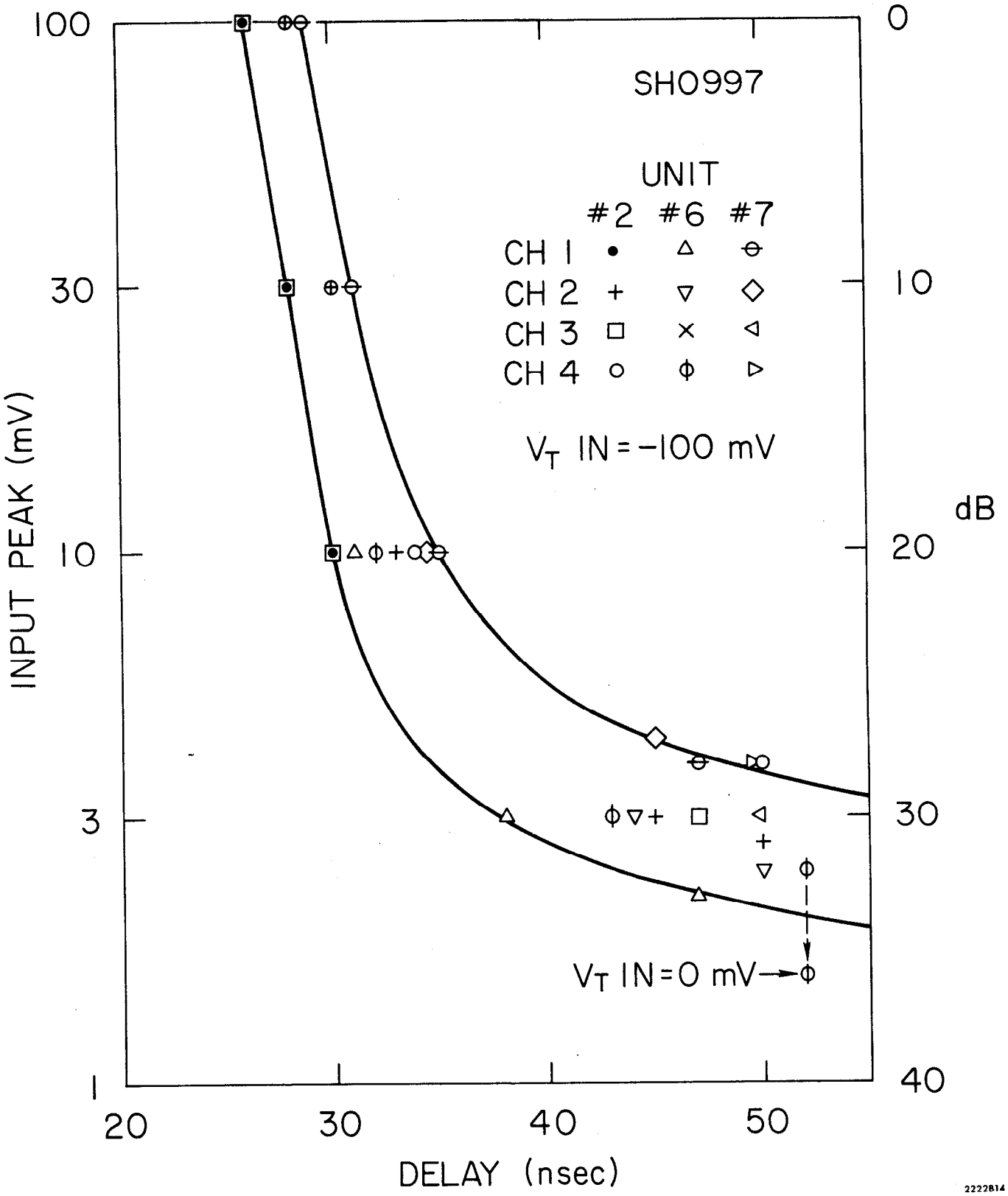


FIG. 13--Time delay vs. input amplitude.

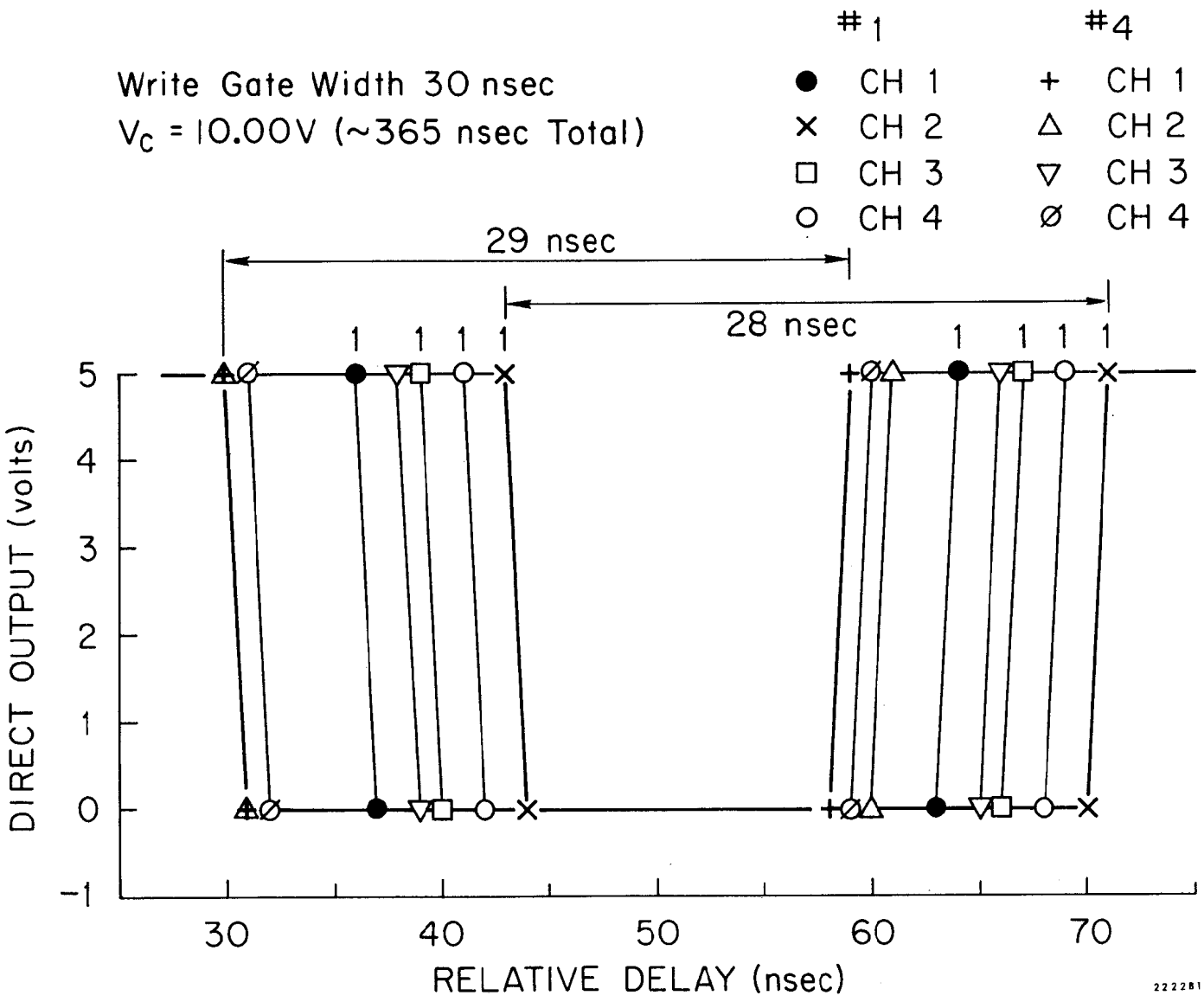


FIG. 14--Write gate delay characteristic.