

AN 8-CHANNEL SAMPLE-AND-HOLD WITH MULTIPLEXED ANALOG OUTPUT*

A. K. Chang and R. S. Larsen

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

Abstract

An economical 8-channel sample-and-hold unit, serially addressable with multiplexed output, is described. The unit accepts clipped inputs of 5 nsec (nominal) FWHM; the positive overshoot of the clipped pulse is rejected. The outputs are held to ± 1 mV for ≥ 1 msec, and are linear to $\pm 1\%$ from 30 mV to 1 V. The output sensitivity is 10 mV per picocoulomb of input charge.

Introduction

A general requirement in large counter experiments is to measure the charges from a large number (say N) of scintillator counters (i.e., photomultiplier tubes), and to present such information to a digital computer for analysis. Two general methods are available: method A uses N sample-and-hold channels, each equipped with its own ADC; method B uses N sample-and-hold channels sharing a single ADC. The advantages for method A are:

1. Conversion times for the ADC's are less critical, hence cheaper ADC's can be used.
2. Since all the analog-to-digital conversion can be done in parallel, demand on the hold time stability of the sample-and-holds is much less stringent.
3. No analog multiplexing is necessary.

The disadvantages for this method are:

1. Relatively costly due to ADC costs.
2. Requires digital multiplexing in the computer readout.

The advantages for method B are:

1. Saves (N-1) ADC's, and in the case when N is large, this saving is significant.
2. Because only a single ADC is involved, one can afford to use a high quality ADC.

The disadvantages are:

1. Requires analog multiplexing.
2. Much more stringent requirement on hold-time stability.

In the interest of lower cost the second method, that of using a single ADC for N sample-and-hold channels, was chosen for a particular experiment at SLAC. An economical 8-channel sample-and-hold unit for this purpose has been designed. The unit has been successfully used in an experiment requiring approximately 70 channels of charge digitization (see Fig. 1).

General Description

The general specifications for the unit are shown in Table I. Each sample-and-hold channel accepts gated clipped inputs of 5 nsec (nominal) FWHM. The unit is specifically designed to reject the positive portion of the clipped pulse, a feature which was not available in commercial units. The input signal is sampled and held to ± 1 mV over a time interval of ≥ 1 msec. During this hold time, the analog outputs are multiplexed through an 8-channel FET multiplexer which is serially addressable through an 8-bit shift register. The fast gate and pre-trigger inputs, and the multiplexed signal output, are high

TABLE I

Specifications

1. Signal Input:
Amplitude -1.5 V maximum into 50Ω
Inputs may be clipped
Positive inputs rejected
Width 5 nsec nominal
50 nsec maximum
2. Fast Gate Input:
Amplitude -800 mV (NIM level)
Impedance 1 K Ω
Width 50 nsec maximum
3. Trigger Input:
Amplitude +5 V pulse (standard TTL level)
Width 0.5 μ sec nominal
Timing same as fast gate or
adjustable internal delay
4. Multiplexed Output:
1 V maximum (nominal) on 8 channels
Impedance 190Ω (limited by FET multiplexer)
Sensitivity 10 mV/pC of input charge
Linearity $\pm 1\%$ nominal, 30 mV to 1 V
5. Digital Inputs:
Clock, Reset, Shift In, Shift Out
Standard positive TTL levels
6. Packaging: 8 channels in a 2-width NIM module
7. Power Requirements:
350 mA at + 12 V 130 mA at - 24 V
240 mA at - 12 V 300 mA at + 6 V
110 mA at + 24 V

impedance so that additional modules may be daisy-chained as shown in the system block diagram in Fig. 2. After each event, the computer reads the N channels serially by sending a read clock pulse to the modules. The delayed pre-trigger is used to reset the sample-and-holds. Metal film resistors and bias compensating diodes have been used to assure good temperature stability. Parts cost per channel in small quantity production is approximately \$75.

Circuit Operation

A simplified circuit schematic is shown in Fig. 3. Fast clipped signals about 3 nsec to 15 nsec wide and up to 1 V peak amplitude pass through a buffer with approximately $\times 1.2$ gain. After the buffer is a fast diode gate, the driver circuit of which is transformer coupled and can accept gates up to 50 nsec wide. This is followed by another stage with a gain of about 7. After this is a current source driving the sampling capacitor C1 through diode D1. The charge is isolated by D1 so that the waveform at the input of A1 is a pulse with a decay time constant of about 18 μ sec.

At this point, the area of the stretched pulse represents the integral of the input signal. This signal is now passed through an amplifier A1, the output of which is ac coupled and restored; and an integrator A2, which is restored by a separate clamp. This combination of clamped capacitors avoids the need for dc coupling of the stretched signal.

A1 has a voltage gain of 2 and lowers the drive impedance to effectively provide a high current (or charge) gain at the input of A2. The coupling capacitor, C2, is restored to ground by clamp S1 after each operation.

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The second integrator, A2, provides an output pulse which is flat to ± 1 mV for ≥ 1 msec. The FET clamp, Q1, restores the integrating capacitor, C3, when a measurement is not in progress. This holds the input of A2 essentially to zero volts. The output offset of A2 due to all effects is less than 1 mV. R1, which controls the input offset current balance, provides an adjustment on the "flatness" of the output signal. The hold time is determined by the timing resistors and capacitors of the one-shots. Therefore, hold time can be easily changed. The output of A2 feeds into a FET multiplexer which is serially addressable through an 8-bit shift register. R2 provides a convenient means of adjusting the overall gain of the circuit.

Figures 4 and 5 show the circuit in greater detail. Some circuit elements justify more discussion here.

1. Front End Buffer and Fast Gate

In order to provide input impedance matching for clipped input signals, a common emitter first stage was chosen over the common base version. The complementary pair Q1 and Q2 have low bias currents and draw higher currents for larger signals. R7 and R52 provide a pedestal-free adjustment for the fast gate.^{1,2} C13 and C14 are added (if necessary) for the same purpose. The gain of this stage is

$$\approx \frac{R9}{R3} \times \frac{R13 \parallel R18}{R11} \approx 1.2$$

2. Pre-Integrator

Q4 and Q11 provide a high current gain to the integrating capacitor C16. For the negative part of the signal, Q4 and Q11 have an initial high voltage gain

$$\approx \frac{R23}{R24} \times \frac{R55}{R54} \approx 190^*$$

and therefore very quickly turn D16 "on", hence charging C16. At this point, the voltage gain drops to approximately 7 for a 5 nsec input signal. Therefore the threshold voltage is:

$$V_T = V_D / \text{GAIN} \quad \text{where} \quad V_T = \text{input threshold voltage} \\ V_D = \text{diode turn on voltage} \\ \text{GAIN} = \text{overall voltage gain} \approx 200^*$$

Since Q4 and Q11 have a final voltage gain of 7 when charging C16 some bandwidth limiting occurs, especially for the narrowest pulses. The net result is that in practice, the minimum attainable threshold is about 10 mV.

For the positive part of the signal, D15 clamps the output of Q11 to one diode drop, thereby making this a unipolar integrator. $C16 \times R4$ gives a decay time constant for the pre-integrated signal of approximately 18 nsec.

Circuit Performance

The linearity of a typical channel is shown in Fig. 6. Note that the useful operating range is 30 mV to 1 V for a 5 nsec input signal. The output pedestal is about 10 mV. Note that for an 8 bit ADC, with 1 V as maximum input, the incremental change per bit is 3.9 mV, which means the digitization accuracy at this point is no better than $\pm 13\%$, and gets progressively worse as the signal gets smaller. Therefore, the non-linearity of the sample-and-hold circuit at the lower end actually coincides with the limit of resolution of the ADC.

*In actuality, these values are considerably lower for the type of input signals discussed. Bandwidth limitation causes slower rise time and therefore results in lower voltage for narrow signals.

The gating characteristic is shown in Fig. 7 for both clipped and unclipped signals. The shape of the curve for a clipped signal is influenced by the finite amount of feed-through of the positive portion of the pulse.

Conclusion

The circuit described represents an economical approach to the problem of measuring pulse charge in large counter experiments. Economy has been achieved primarily by utilizing high packaging density and the sharing of timing and gating circuits.

Acknowledgements

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References

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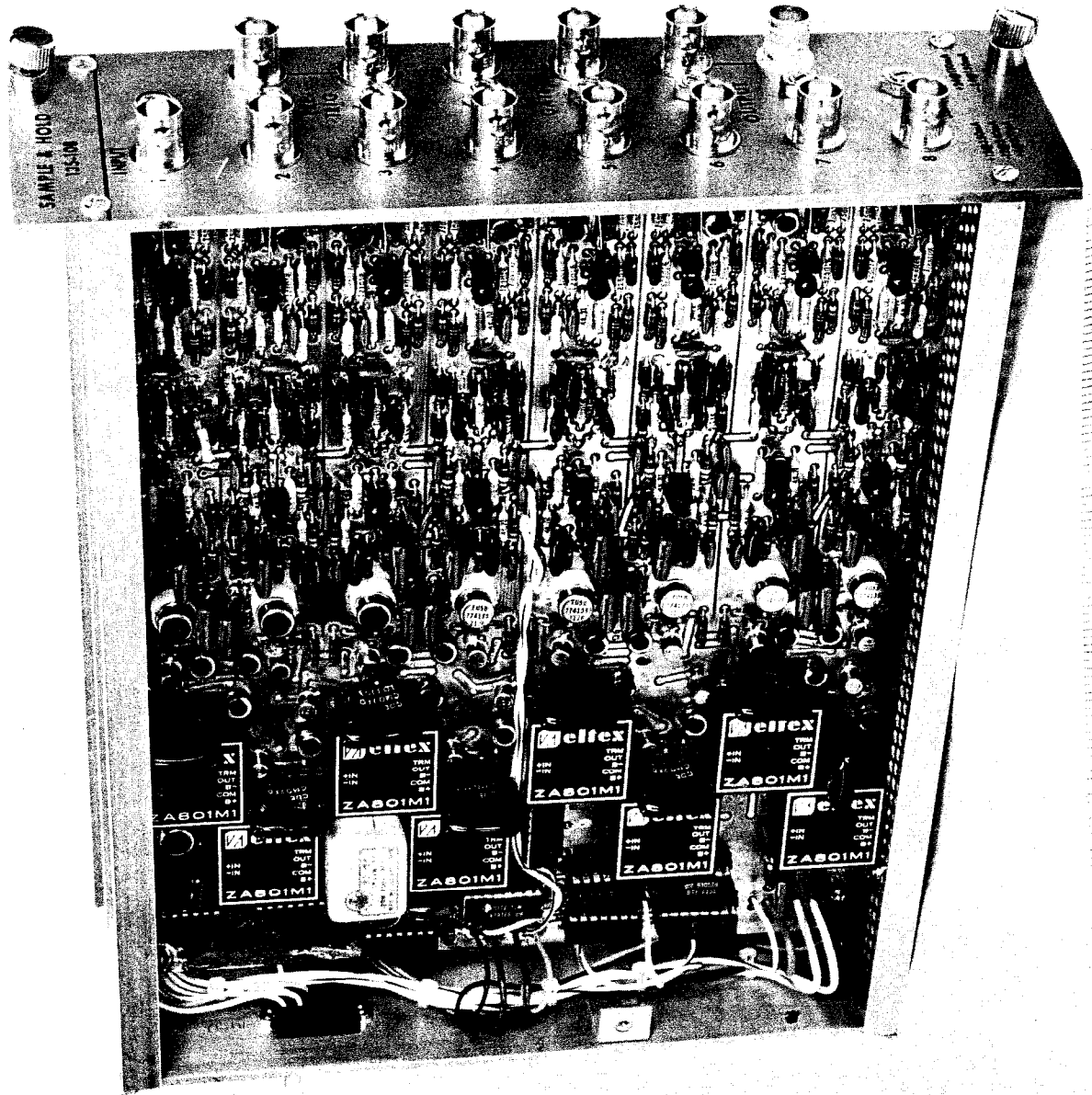


FIG. 1--8-channel sample-and-hold unit.

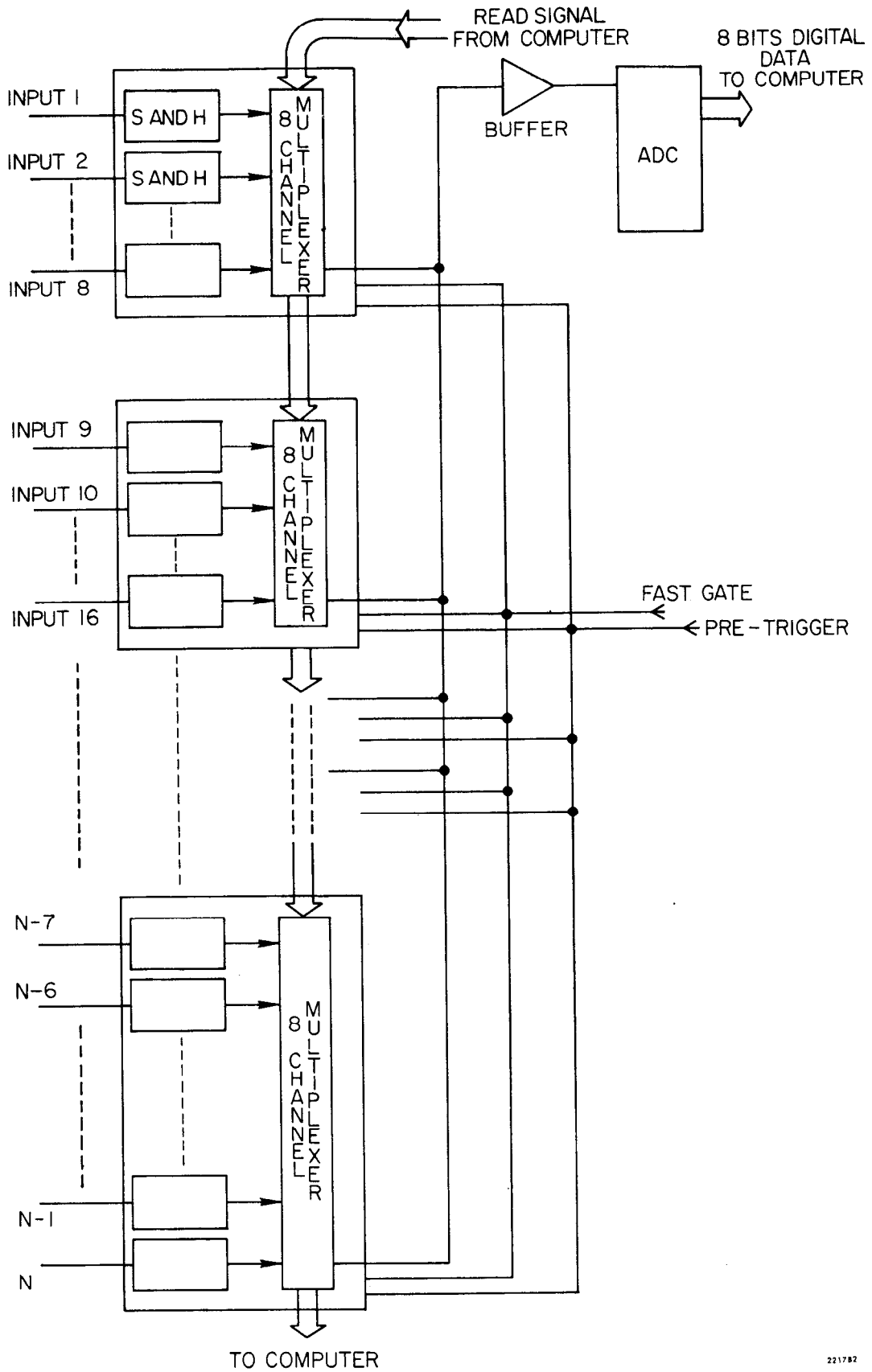


FIG. 2--System block diagram.

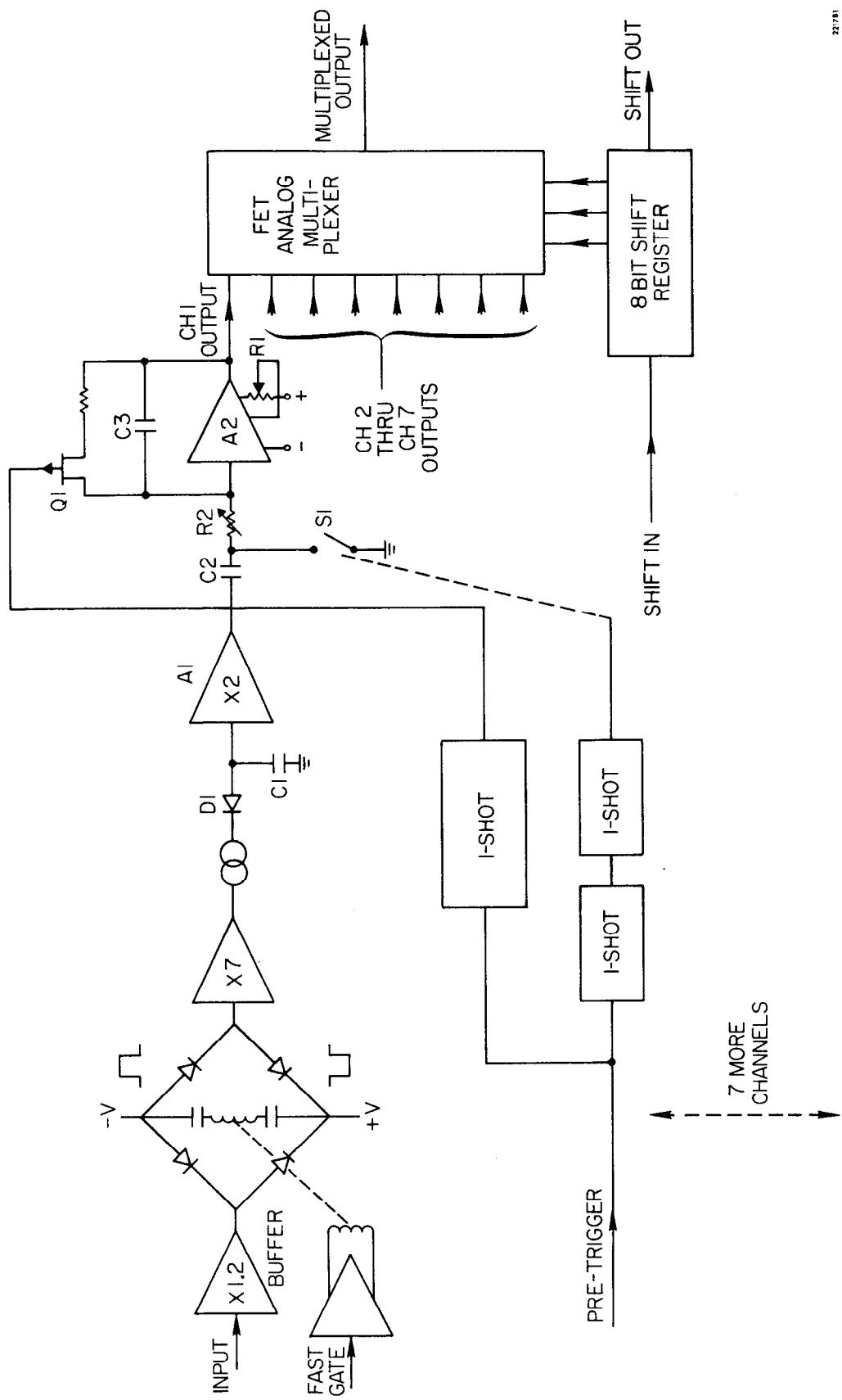


FIG. 3--Simplified schematic of 8-channel sample-and-hold.

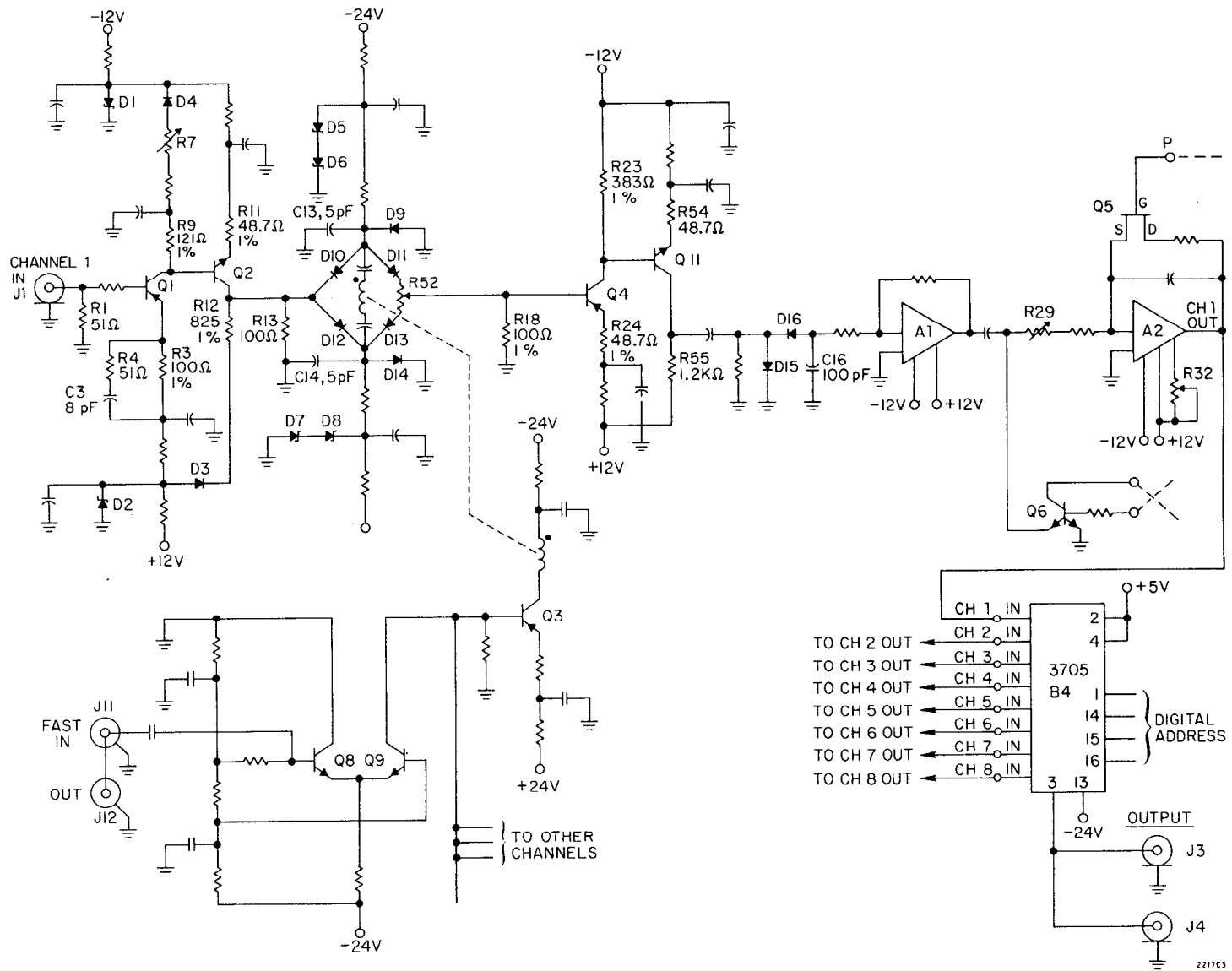


FIG. 4--Detail circuit - part 1.

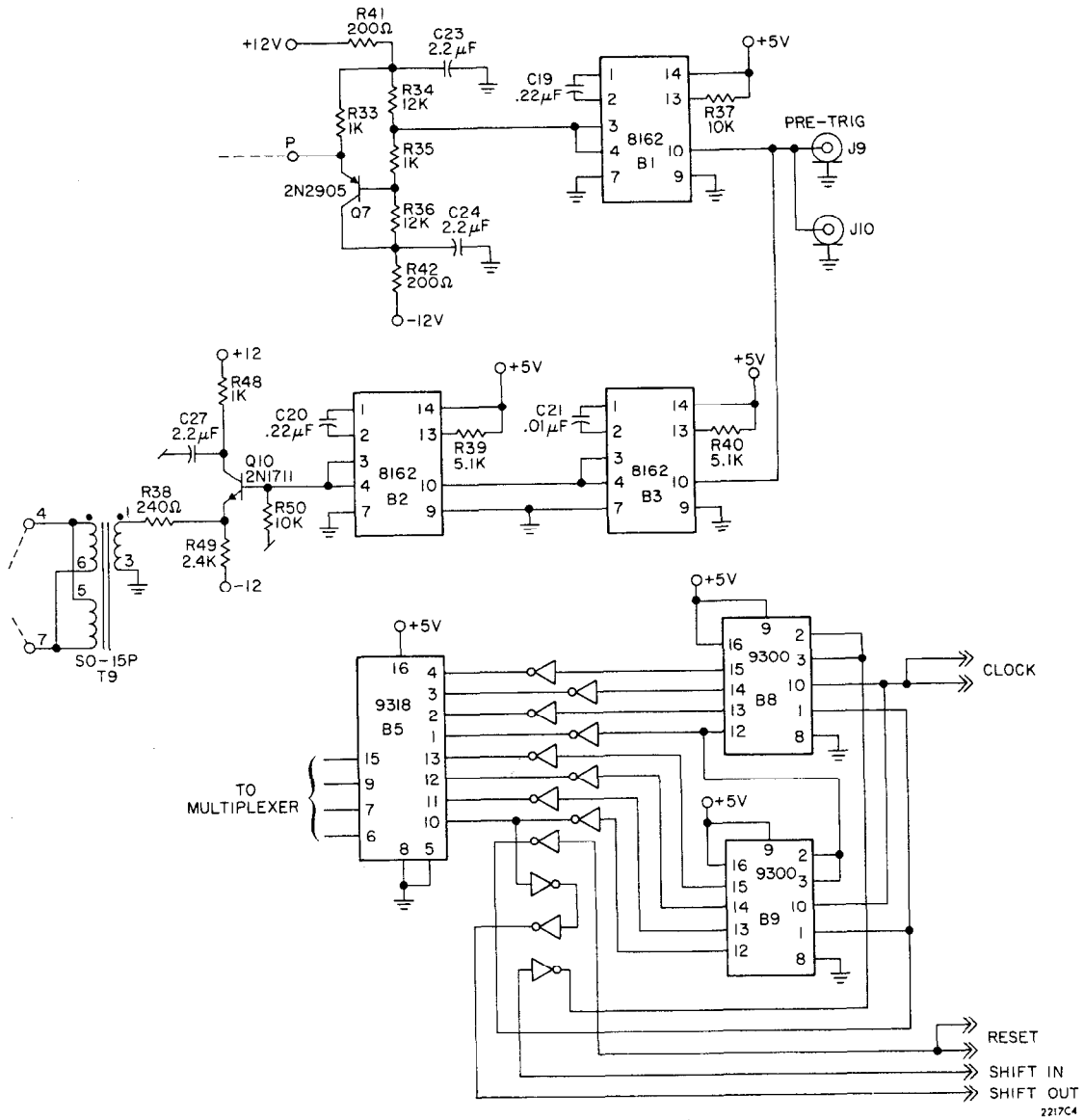


FIG. 5--Detail circuit - part 2.

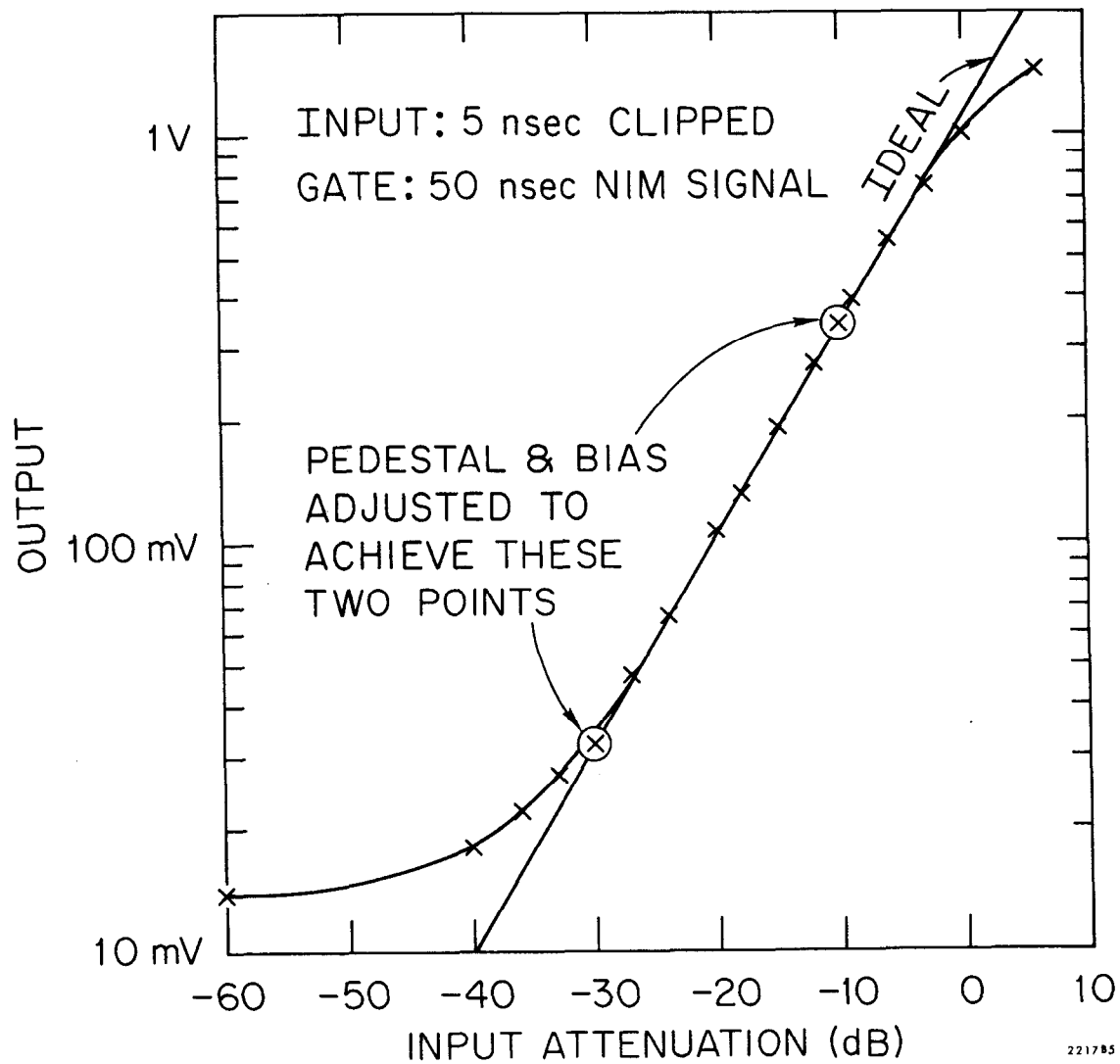
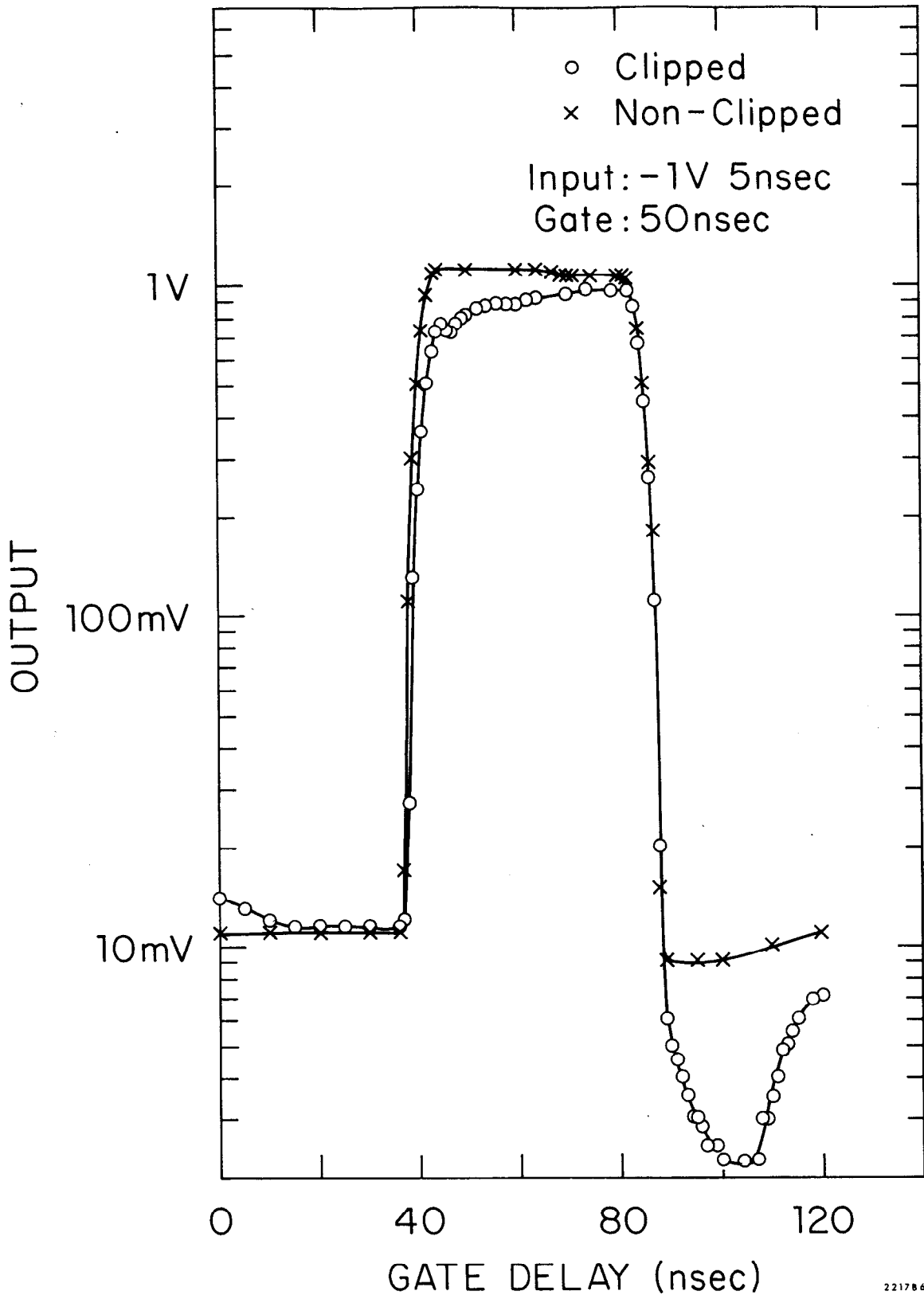


FIG. 6--Linearity curve for a typical channel.



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FIG. 7--Gating characteristics for a typical channel.