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VERSATILE, MODULAR READOUT SYSTEM FOR CAMAC SCALERS*

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Summary

A display and readout system for CAMAC scalers will be described which has been in use at SLAC for over a year. Flexibility and versatility are the keynotes of the system, which includes a modular quad display unit employing highly readable Nixie tubes. Other units which may be connected to the expandable bus include an X-Y scope display and a preset count module.

The system employs a simple, but versatile CAMAC crate controller. Capability for connection to computers is included, and the system has been interfaced to several different computers.

Background

The introduction of CAMAC and commercial CAMAC scalers[1] provides an ideal medium for expansion and/or modernization of scaler systems. A display and readout system for standard CAMAC scalers has been conceived, built, and used at SLAC for over a year. The following ground rules and guidelines have been used in developing this scanning system.

1. The system should be versatile and modular to satisfy different user requirements and varying system sizes. Use of high impedance bus structures for scalers and displays is a good way to achieve this goal.

2. The equipment should be capable of stand-alone operation as well as operation with computer control.

3. The approach should be simple and dedicated to the single purpose of scaler readout. In other words "dedicated" crates (scalers only) and "dedicated" crate controllers are permissible.

4. Every effort should be made to ease the transition from Nixie display scalers (TSI)[2] to CAMAC blind scalers. However, the additional complication of combining the two systems during the transition phase is not worthwhile.

5. Since different computers are involved, the design should minimize the system committment to computer interfacing, and simply provide the capability for computer access to data and control of the CAMAC modules.

6. System interactions should be minimized so units function independently, and failure of a single modular scaler or readout will not completely disrupt the system.

7. The design should allow maximum settling time of all data and control lines to permit maximum cable lengths. The scanning rate should be as slow as possible consistent with human eye speed of response (30-60 refreshes/sec).

8. Built-in verification capability should be included.

9. Capability for hard copy of data should be included.

Considerable time was spend evaluating several approaches to the problem of scaler readout in the context of these guidelines, particularly the area of digital display (Item 4 above). The system that is described here evolved from these ground rules and has been successful in meeting all new requirements during the first year of operation. It is now widely used throughout SLAC.

Basic Concepts of System Organization

The system is organized around a master control unit which generates sequential CAMAC addresses and sends them onto a CAMAC bus; the returning parallel binary data is converted to BCD data and sent together with BCD channel addresses onto a BCD bus. In this way both data inputs (scalers and crates) and readouts (or data processors) can be expanded in modular fashion. Q-scan control is used; that is, the Q response from the addressed module controls the CAMAC address generator and is used to decide if the data should be converted and sent to the BCD bus or the CAMAC address advanced to the next module.

Computer control of the system is accomplished by a single disable line in the CAMAC bus which discontinues the scan and turns off all the open collector drivers in the master controller. The computer can then generate CAMAC CNAF codes at the available CAMAC bus interface and retrieve data or perform other CAMAC actions.

Figure 1 shows the overall configuration of the system with all of the existing options shown. The master controller is connected to up to 7 crates via a CAMAC bus which is described in detail in Fig. 2. The BCD output is transmitted to readouts via the BCD bus shown in detail in Fig. 3.

The basic display unit is a quad (4 channel, 8 digit/channel), Nixie display with arbitrary channel selection from 1 to 1000 using three thumbwheel switches. These units connect to the BCD bus and can be expanded with no interaction on each other or on the master controller. Leading zero suppression is optional. By generating BCD code 10 in the master controller and sending it on the appropriate BCD lines, the corresponding digit is blanked.

Other units that can be connected to the bus include an X-Y scope display for monitoring all channels, and a preset count module for normalization of data.

Interface and control for the HP562A or 5050B printers is an optional capability and is located in the master controller, in order to simplify interactions on the BCD bus.

The disconnect unit shown in Fig. 2 allows the scaler display system to run asynchronously in a CAMAC bus containing other crates which may include data gathering devices such as ADC's, latches, etc. The bus is only unified when the computer desires access to data in the scaler crates. Such a coordinated system is now running in the new SPEAR magnetic detector at SLAC.

The verification module located in the CAMAC crate simulates a quad scaler, and generates known data for system verification and test purposes.

Master Controller

Figure 4 is a block diagram of the master controller which contains the sequential CAMAC address generator, the serial binary-to-BCD converter[3] with zero suppression logic, the BCD address counter, the control system, line drivers and receivers, and the optional interface and control for the printer.

All timing and control resides in this unit, and if Q=1 the entire system runs as if all crates were full of 16 channel scaler modules. No handshake techniques are used; the

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controller is set to run at the speed of the slowest component, the LeCroy 559A Display Generator, which takes about 600 μsec to display each channel.

Some details of the operation phases are shown in the overall timing diagram, Fig. 5. Note that the operations are overlapped, or phased; that is, while address N is sent out over the CAMAC bus to retrieve data N, address N-1 data is sent over the BCD bus, and address N-2 data is currently being displayed. In this way maximum settling time is permitted for all address and data lines, equal to the basic cycle rate, instead of sequentially performing operations within the cycle time framework. Note that there is a BCD strobe signal which is sent to all readout units, just ahead[4] of the time for BCD address and data to change. This signal loads data into all readout registers, and provides the clock signal for the LeCroy 559A. Although not illustrated there is a BCD reset at the end of the scanning cycle that resets the channel counter in the LeCroy 559A.

Auxiliary, but useful features of the master controller include manual or electrical reset of all channels, electrical inhibit of all channels, and provisions for manual testing of all channels using F(25). Setting a front panel switch to "TEST" generates F(25), crate 7, module 31, which selects all scaler channels in the system. All channels then accumulate one count for each input pulse sent to the controller from an external test generator which produces known codes.

Crate Controller

A minimal crate controller was designed to connect 7 crates together on a CAMAC bus, and provide the necessary N line decoding and line driving. At the time of this design the type A crate controller was not yet officially adopted. In addition, the ground rules permitted a dedicated system, so the design of a special crate controller was justified. On the other hand, a sufficiently general crate controller was designed so it possibly could be used in other CAMAC systems. For example, a write capability was included, although the scalers have no use for this feature.

The crate controller design shown in Fig. 6 repeats all Dataway signals on the CAMAC bus, and includes no flip-flops or other timing elements. High impedance receivers and open collector drivers are used. Note that all L signals are tied together to produce a single L demand in the CAMAC bus. Separate inputs for gating (I line) and clear are provided.

Due to the general interest in simple, low cost crate controllers, a detailed schematic is shown in Fig. 7. This crate controller has in fact been used in several other CAMAC systems at SLAC.

Quad Display Unit

The choice of conventional sideviewing Nixies for display was a trade-off between cost, size, legibility, reliability, availability and simplicity. Of course, they also ease the transition from TSI to the CAMAC scalers. Other displays evaluated included gas panels, LED's, X-Y oscilloscope, and television raster scan. The X-Y oscilloscope was retained as an optional part of the system due to its ability to display a large number of channels economically, with flexibility to adjust to various situations.

A block diagram of the quad display unit is shown in Fig. 8. High impedance receivers are used on all address and data lines. The design is organized around a parallel internal bus which repeats the BCD address and data. Comparators indicate when the desired channel data is on the bus and the data is strobed into latches by the BCD strobe. A separate common enable line is provided to turn on all channels simultaneously for test purposes.

BCD code 10 is the zero suppression code, and the SN74141 drivers blank the appropriate Nixie tube when this digit is received.

X-Y Scope Display

The LeCroy 559A display generator contains all the circuitry for displaying 160 channels of 8 digit BCD data on an X-Y scope, using a 7 segment format. Since the BCD bus is negative true, an interface module is necessary to provide positive true data for the LeCroy 559A. In addition, data storage is necessary. Furthermore, if zero suppression is operating, the interface must convert the leading zeroes (code 10) to code 0, since the LeCroy generator already contains circuitry to suppress leading zeroes.

Figure 9 shows a block diagram of the interface unit for the LeCroy 559A.

Preset Unit

A scanning type system is somewhat limited for presetting due to the inherent timing errors. However, due to the particular SLAC beam characteristics and available counting rates, a preset unit connected to the BCD bus turns out to be feasible. Furthermore, preset errors can be monitored by displaying the final preset count.

The schematic of the unit shown in Fig. 10 permits arbitrary channel selection, 1 to 1000, and a preset count of 1 to 9 times 10^N. True and false TTL and 12 volt levels are provided at the output to gate discriminators, etc. Due to the modular design several presets may be connected to the BCD bus for more complex experiment control.

Verification Module

The CAMAC verification module simulates data from a quad scaler to test and verify overall system operation. Subaddress 0 generates $000\cdots0_2$, and subaddress 1 generates $11111\cdots1_2$. These test both logic levels of the CAMAC Dataway, crate controller, binary to BCD converter, etc. Subaddress 2 and 3 generate an arbitrary code selected by 24 front panel switches. These are used to test system wiring and cabling, and to test for shorts in the CAMAC Dataway, etc.

A schematic of the unit is shown in Fig. 11. Note that a clear input turns off all outputs to ease overall verification when the system is cleared.

Packaging Considerations

Each unit was independently packaged according to the number of IC's, size limitations, number of units to be built, and function within the system.

The master controller contains about 90 IC's without the printer interface, and about 120 IC's with the interface. It is constructed with conventional wire wrap in a 19" wide unit, 3-1/2" high, as shown in Fig. 12 without the IC's inserted.

The crate controller contains about 40 IC's in a double-width CAMAC module as shown in Fig. 13. Two printed circuit cards are used, one with the read-write circuitry; the other with the control buffering, N-line decoding, etc.

The quad display unit contains about 70 IC's. A large printed circuit card (motherboard) carries the internal bus along with the line receivers, data latches, and address comparison circuitry. Four separate plug-in cards contain the Nixie tubes and drivers. For the two levels of display two motherboards are used; interconnections are made by multi-conductor flat cable and connectors. Figure 14 shows a photograph of this construction technique.

The LeCroy 559A interface module and the preset unit are both of wire-wrap construction in double width NIM modules, since they do not connect to the CAMAC Dataway and are associated with existing NIM modules. (The LeCroy 559A is packaged in NIM.) The verification module is double width CAMAC using wire-wrap, but a printed circuit card might be more appropriate here.

A photograph of the system is shown in Fig. 15, although it does not include all of the available units.

Experiences and Future Plans

The modular system described here has been successful in meeting the varying demands of several experimental groups at SLAC, and appears to be slowly replacing the TSI scaler banks. All variations in system configuration have been used, with the quad Nixie display the common factor. These units have been very successful and the 1/2" character height seems to be the optimum standard for all users and their experimental layouts. The leading zero suppression has been popular, and is universally used so far. Addressability of the channels is useful, but most users prefer to leave assignments fixed once they are selected. Partially as a result of this, the original prediction of two quad displays (8 channels) per system is inadequate, and the more common request is for four quad displays (16 channels). In fact, it appears that the number of requested display channels is relatively constant regardless of the number of scaler channels. In one particular experiment the number of display channels equalled the number of scaler channels (20). The resemblance here to the TSI scaler philosophy is unmistakable.

Overall reliability and counting accuracy have been very good. The only difficulties from a reliability standpoint have been the quad display units. These have had a number of failures including Nixie drivers, intermittent connections, and power supplies. However, these failures have been system independent; that is, at no time was the whole system inoperative. It is felt that some of the problems can be traced to excessive heating, and fans are currently being added to the units. In the future it is possible that new display units will be designed based on newer technology (multiplexing, LED's, etc.) with a larger number of incremental channels in order to reduce the cost/digit. (The present total cost of the quad display is now approximately $30/digit.)

Counting accuracy has been tested in very long runs with perfect results. However, in one particular special scaler model, periodic interference of the asynchronous CAMAC Dataway scanning was detected. The trouble was traced to the scaler front end, and minor modifications corrected the problem. The importance of long term accuracy tests cannot be overestimated.

Computer interfacing has been achieved with a minimum of effort due to the flexibility and simplicity of the CAMAC bus. The system has been interfaced to a PDP-8, XDS9300, XDS Sigma 5, and in the near future, a PDP-11. All are operated on a program control basis.

The X-Y scope presentation of all data has been popular, and has aided in the transition from the TSI scalers. Additionally, in one case the user found that a photograph of the X-Y scope was more convenient than the printer tape. Should the scope display remain popular it may prove worthwhile to integrate the interface and character generator into one new unit for simplicity.

Acknowledgements

Obviously a task of this magnitude involved the efforts of many people. Wayne Knapp performed the difficult packaging for the quad display. Paul Arechiga constructed and helped de-bug several of the units, including the master controller. John Kieffer developed production documentation so that the equipment could be efficiently constructed by the SLAC Electronics Shops under the direction of Frank Generali.

The author would like to thank Mike Brown, who made several useful suggestions in the design of the crate controller.

Special thanks go to Bob Hettel, who detailed and coordinated much of the construction and who designed several portions of the system, including the printer interface.

References

1. Such as the E.G.&G. S424, the LeCroy 2550B or the Jorway 84.
2. Transistor Specialties, Inc. Model 1535/M-71 and other such units have been used at SLAC for many years. These feature a 7-digit, 0.6"-high Nixie display for each channel.
3. V. Thomas Rhyne, "Serial Binary-to-Decimal and Decimal-to-Binary Conversion," IEEE Trans. on Computers, September 1970, p. 808.
4. There is a 5 μsec guard band between the end of BCD strobe and the changing of data lines.

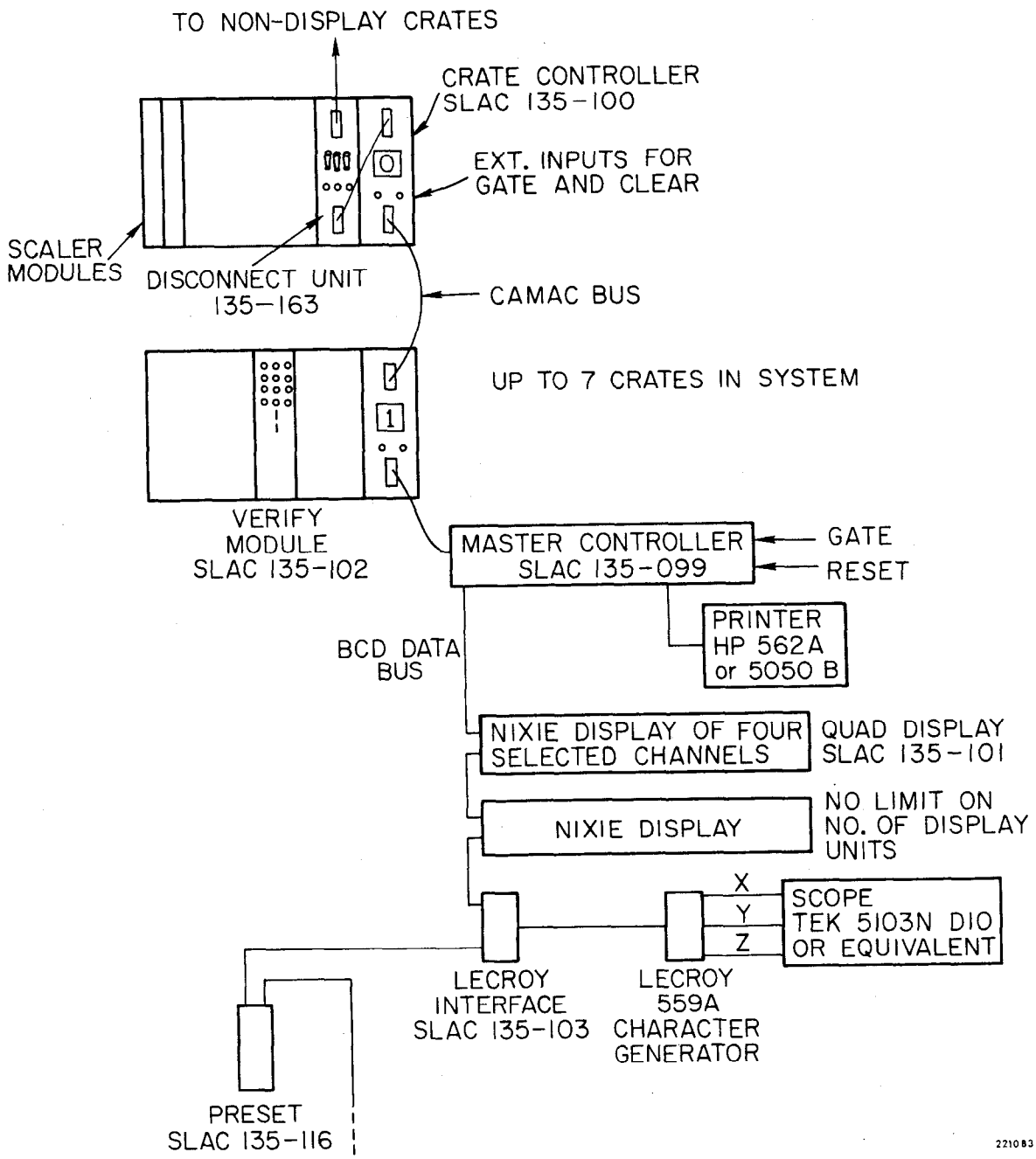

FIG. 1--Overall block diagram.

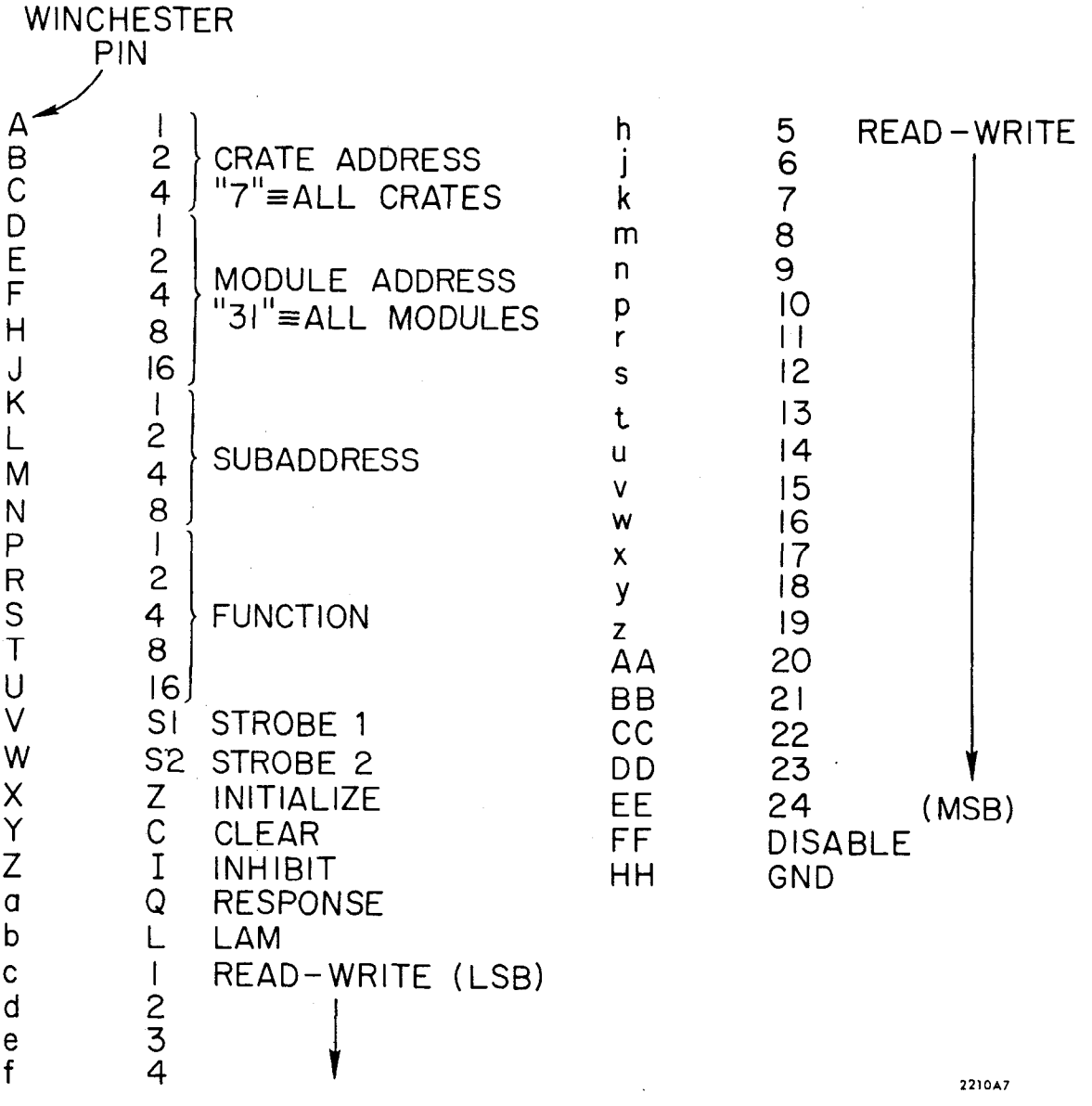

FIG. 2--CAMAC bus details (all signals negative true).

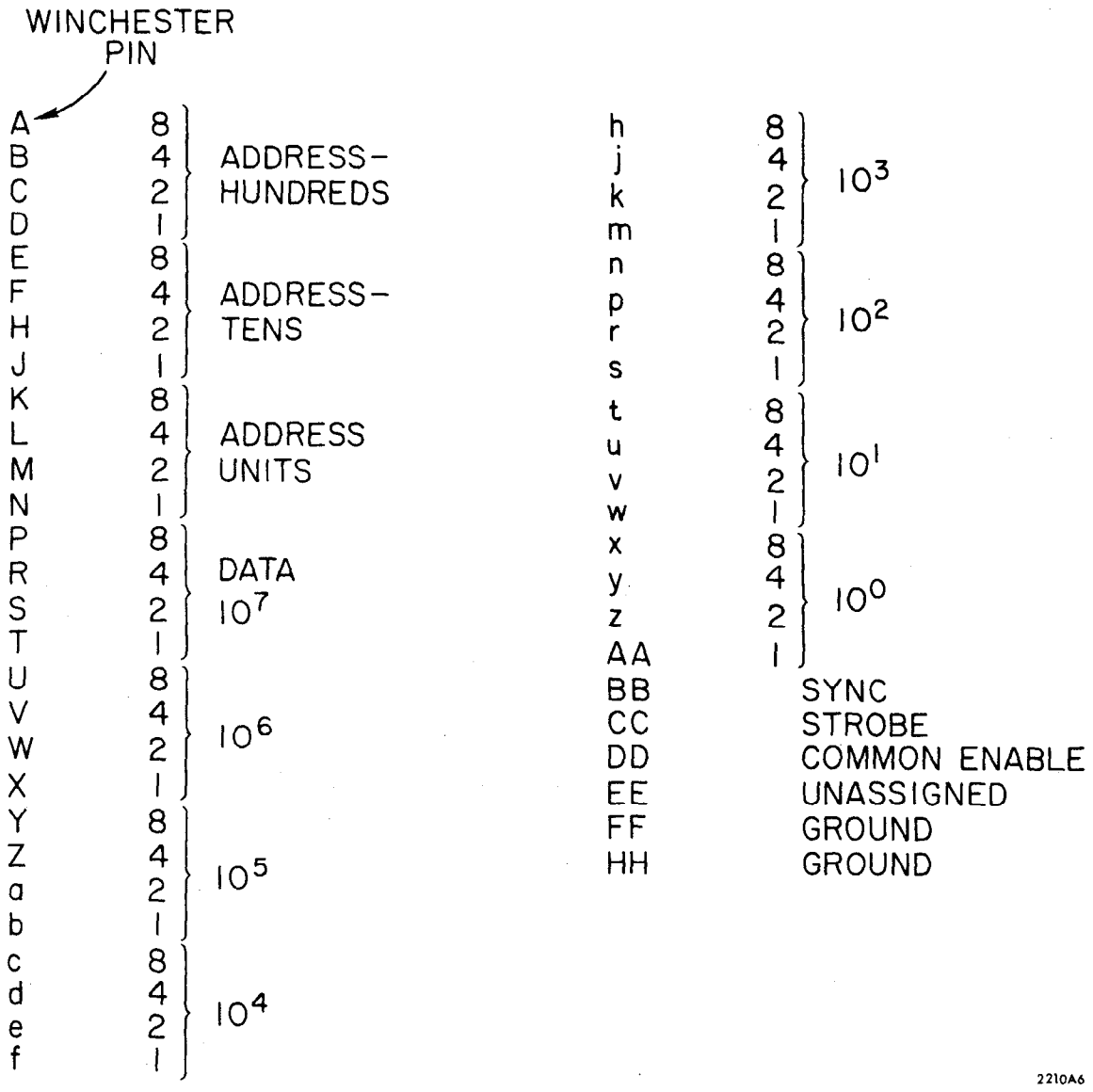

FIG. 3--BCD bus details (all signals negative true).

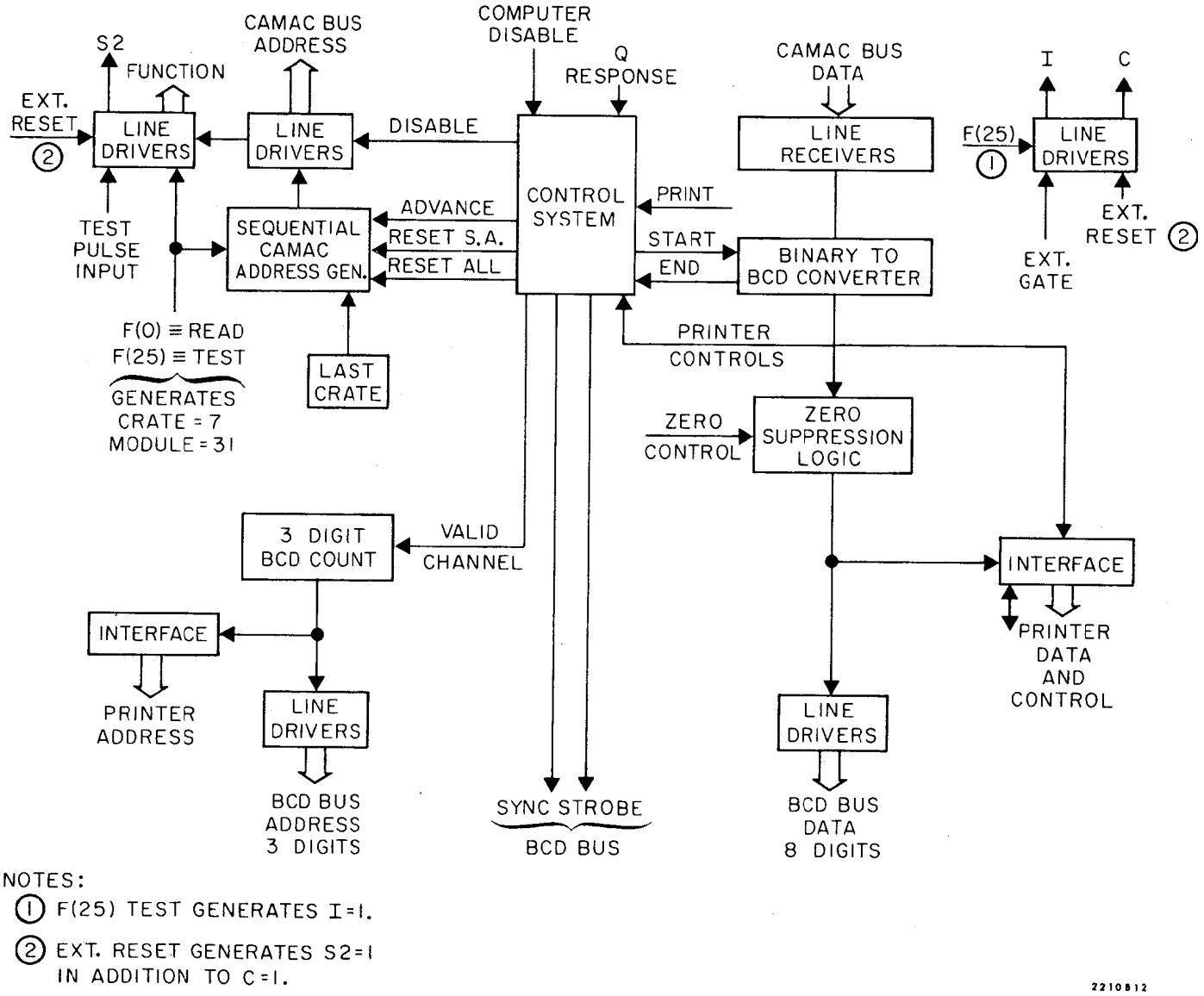

FIG. 4--Master controller block diagram.

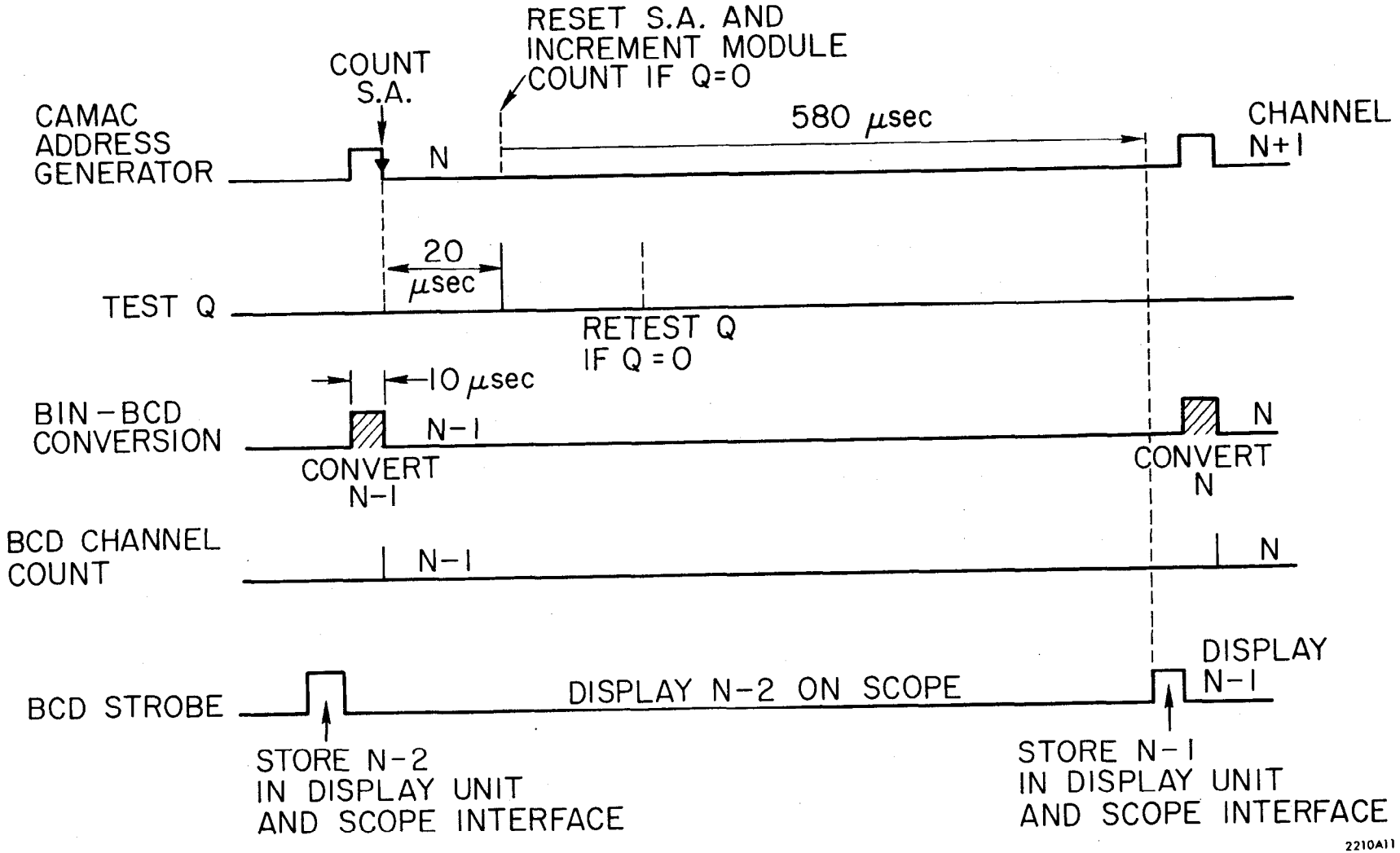

FIG. 5--Overall timing diagram.

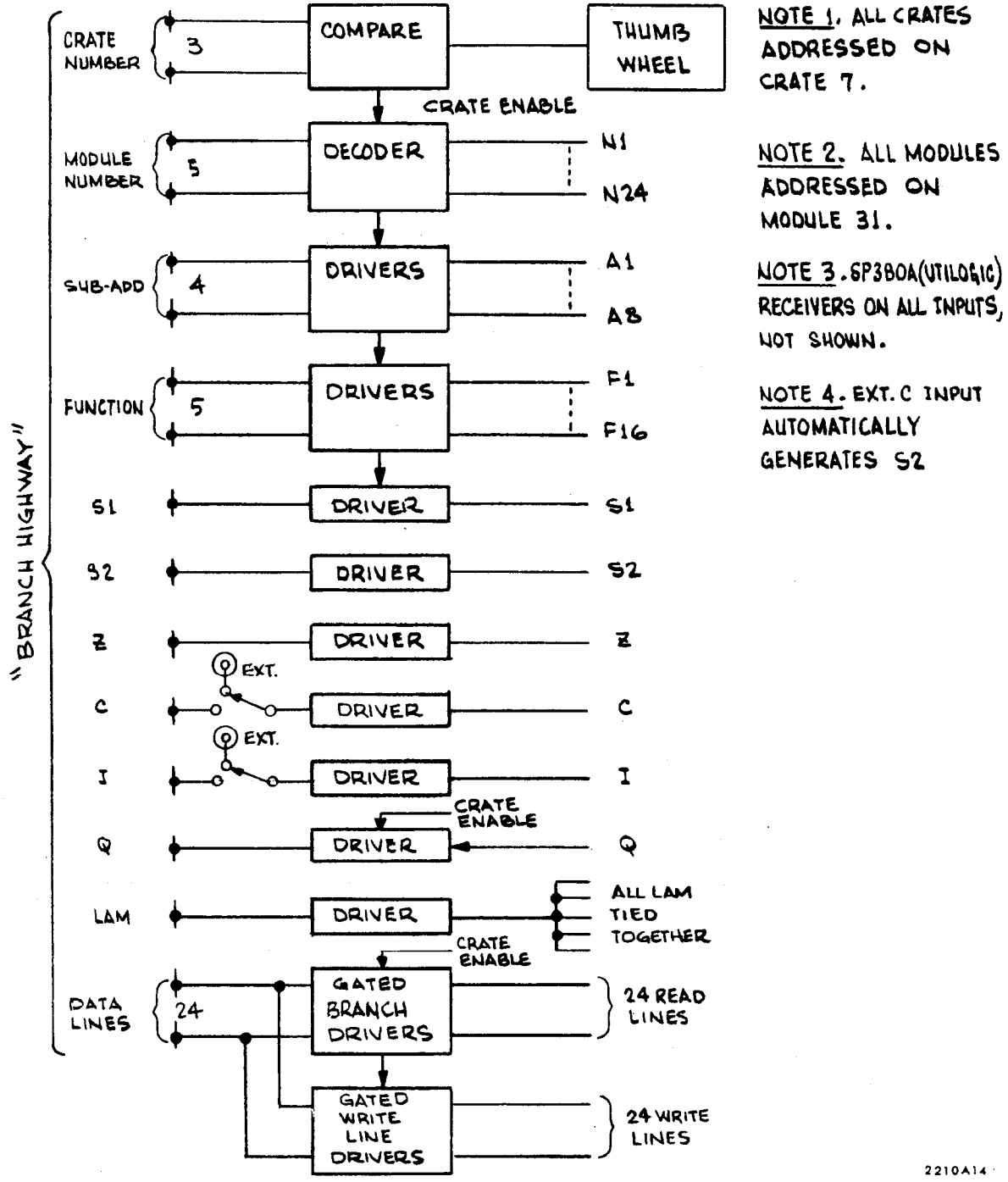

FIG. 6--Crate controller block diagram.

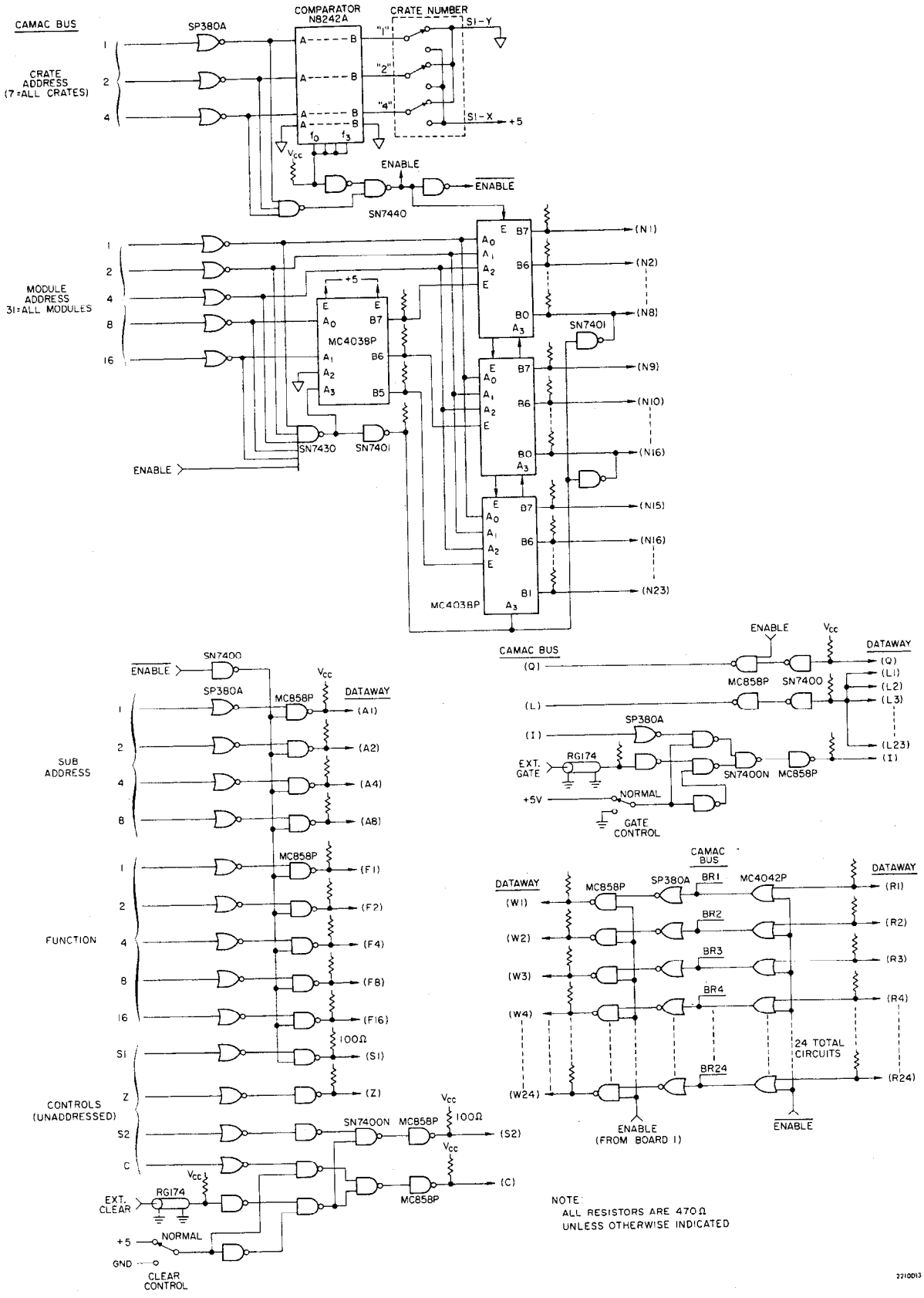

FIG. 7--Crate controller schematic.

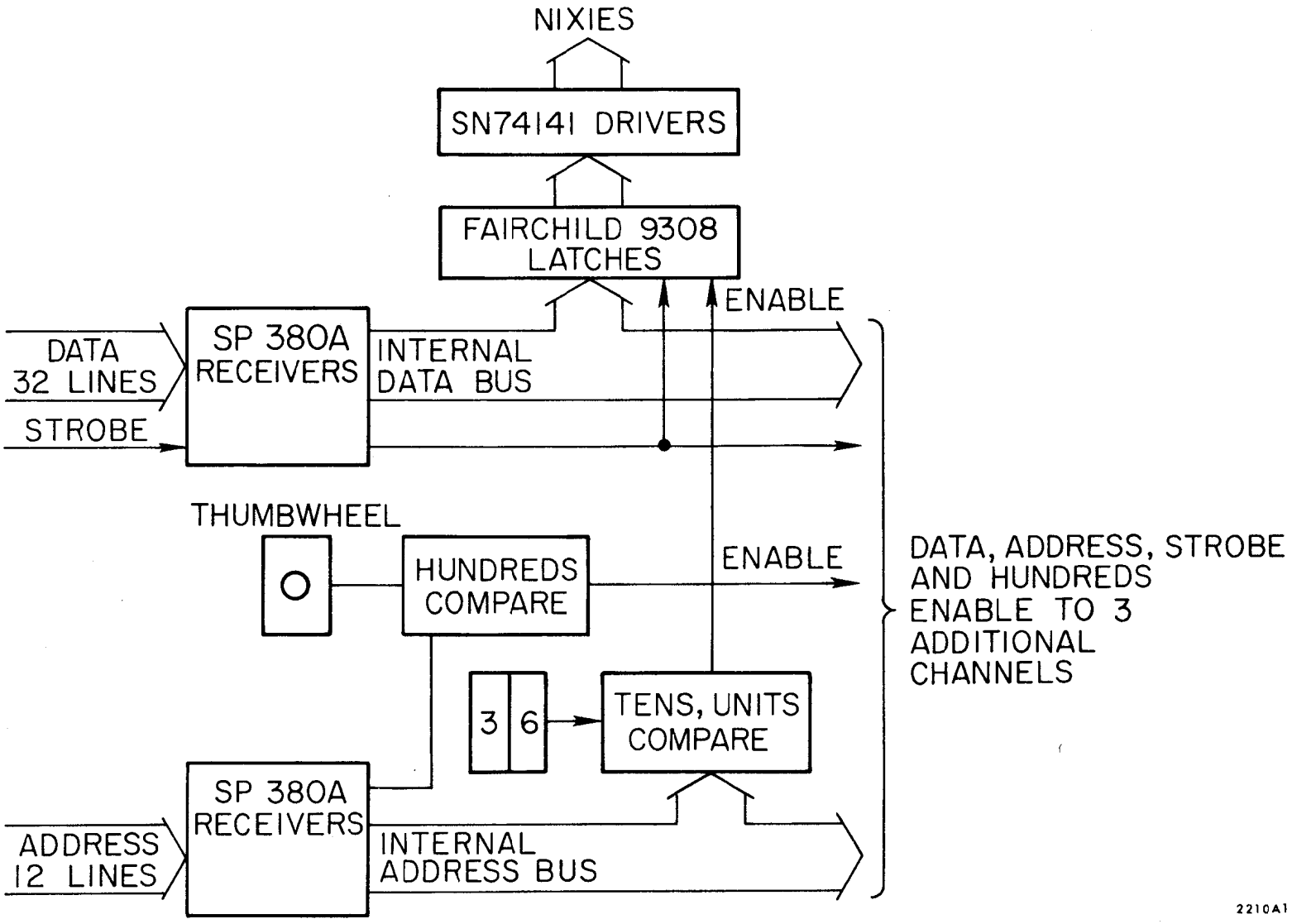

FIG. 8--Quad display unit block diagram.

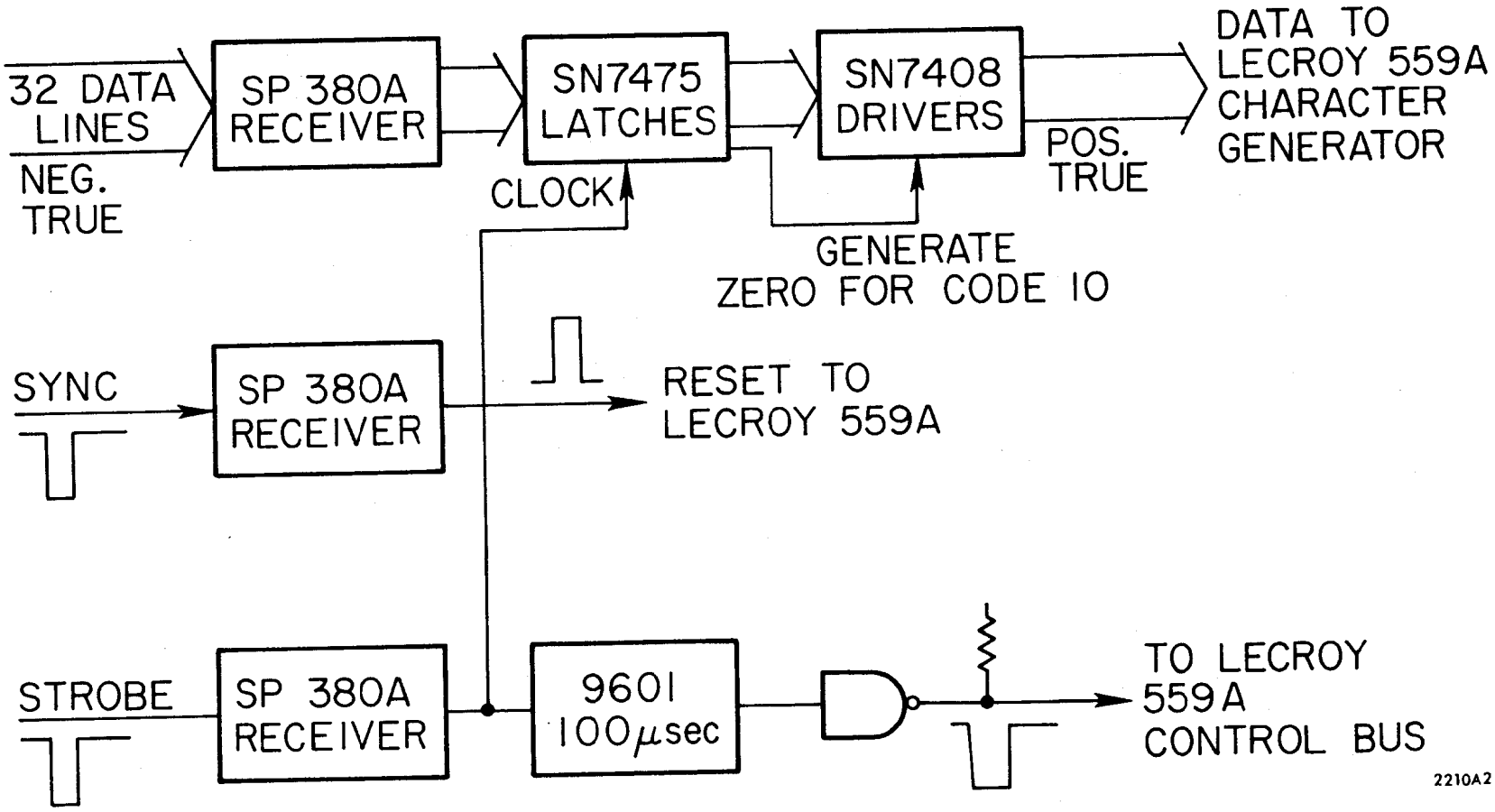

FIG. 9--LeCroy 559A interface schematic.

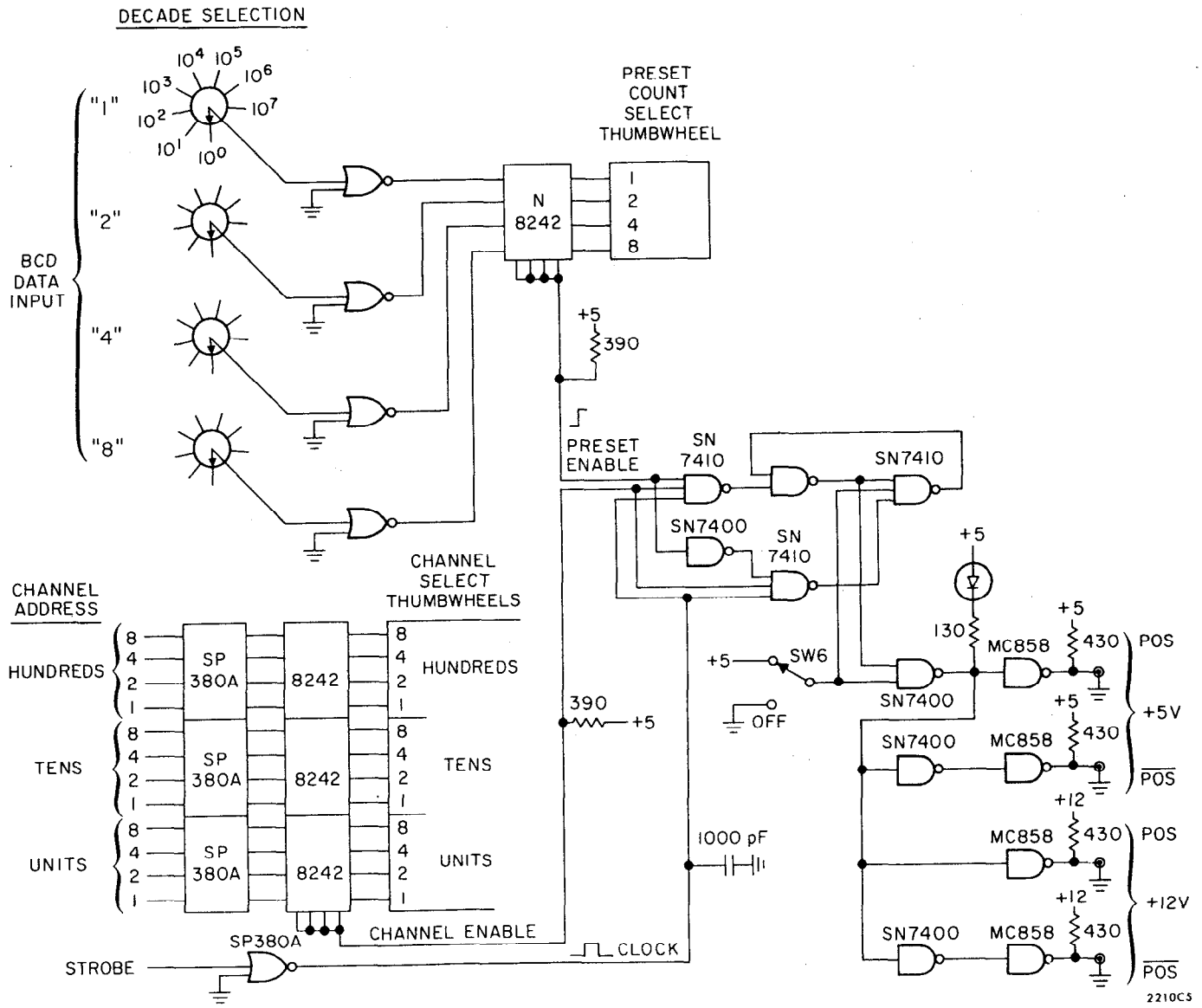

FIG. 10--Preset unit schematic.

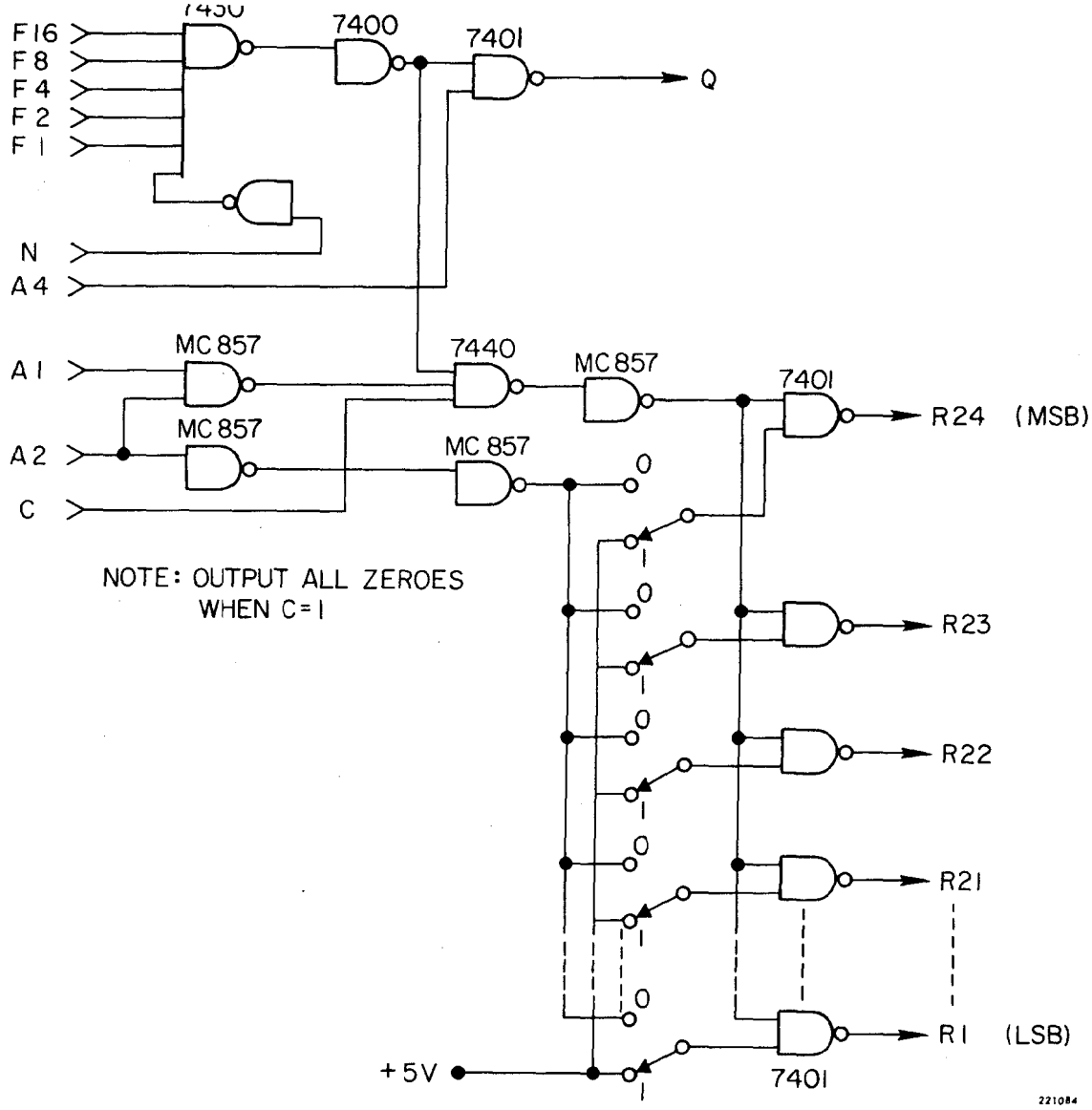

FIG. 11--Verification module schematic.

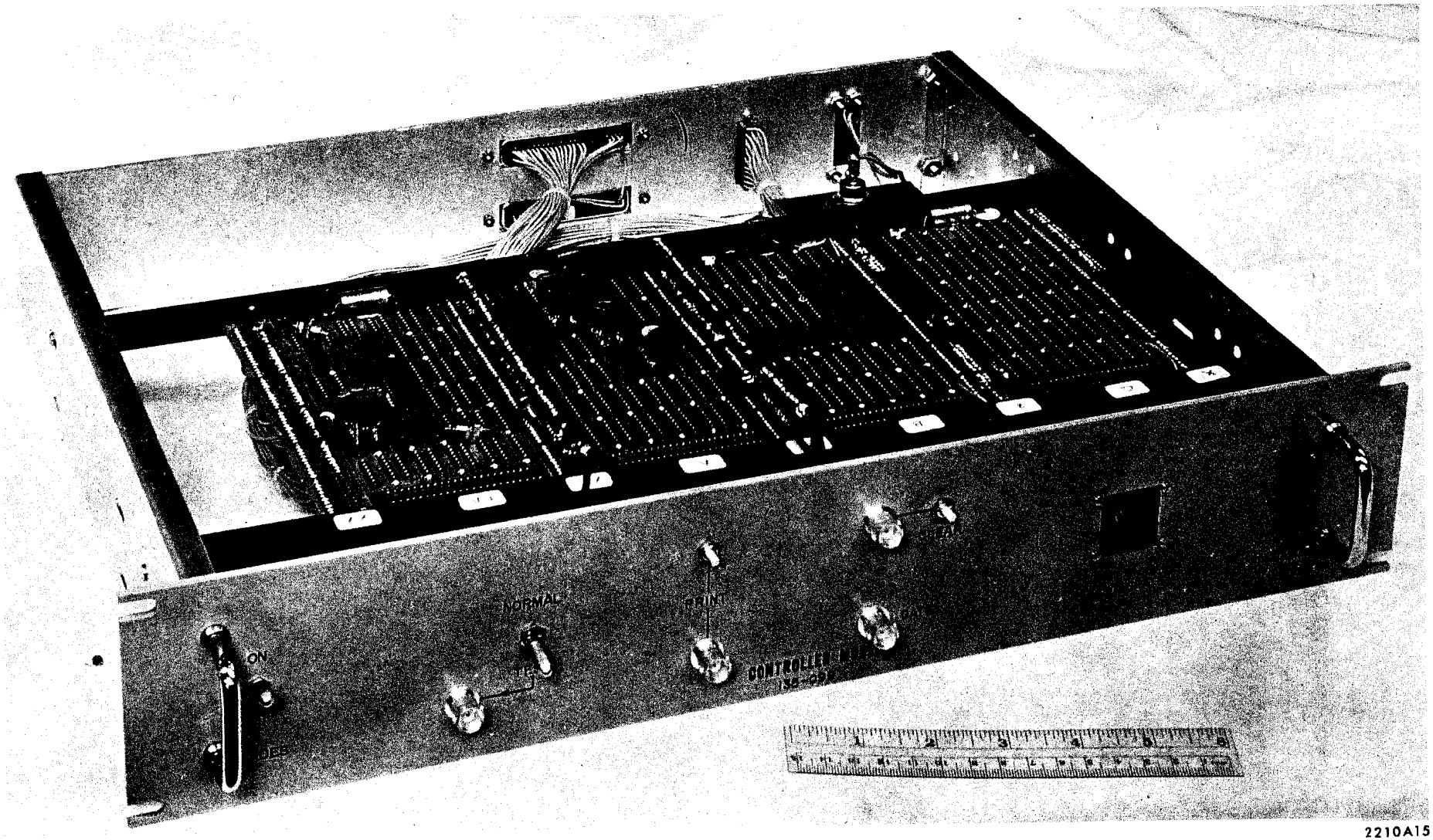

FIG. 12--Photograph of the master controller.

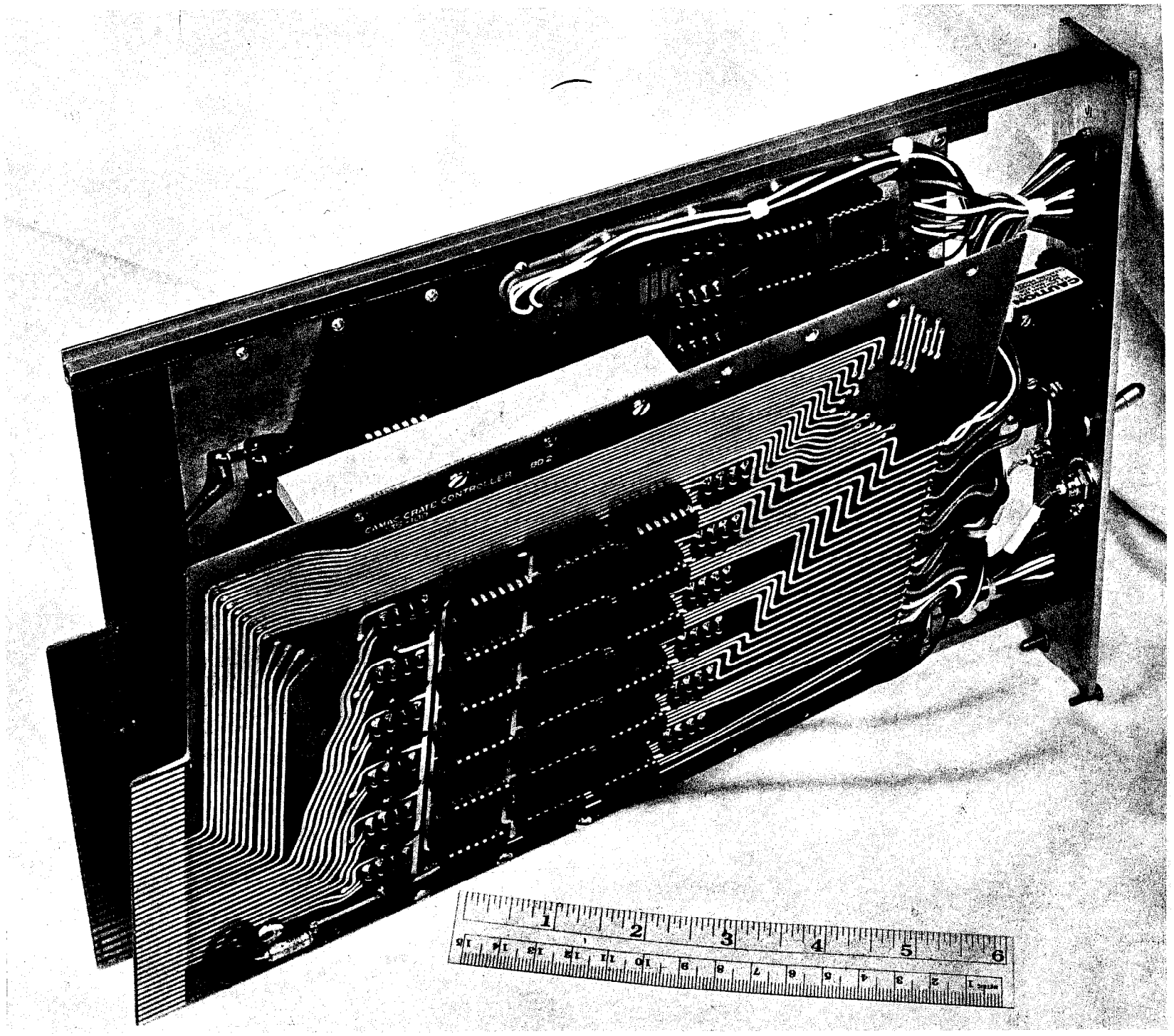

FIG. 13--Photograph of the crate controller.

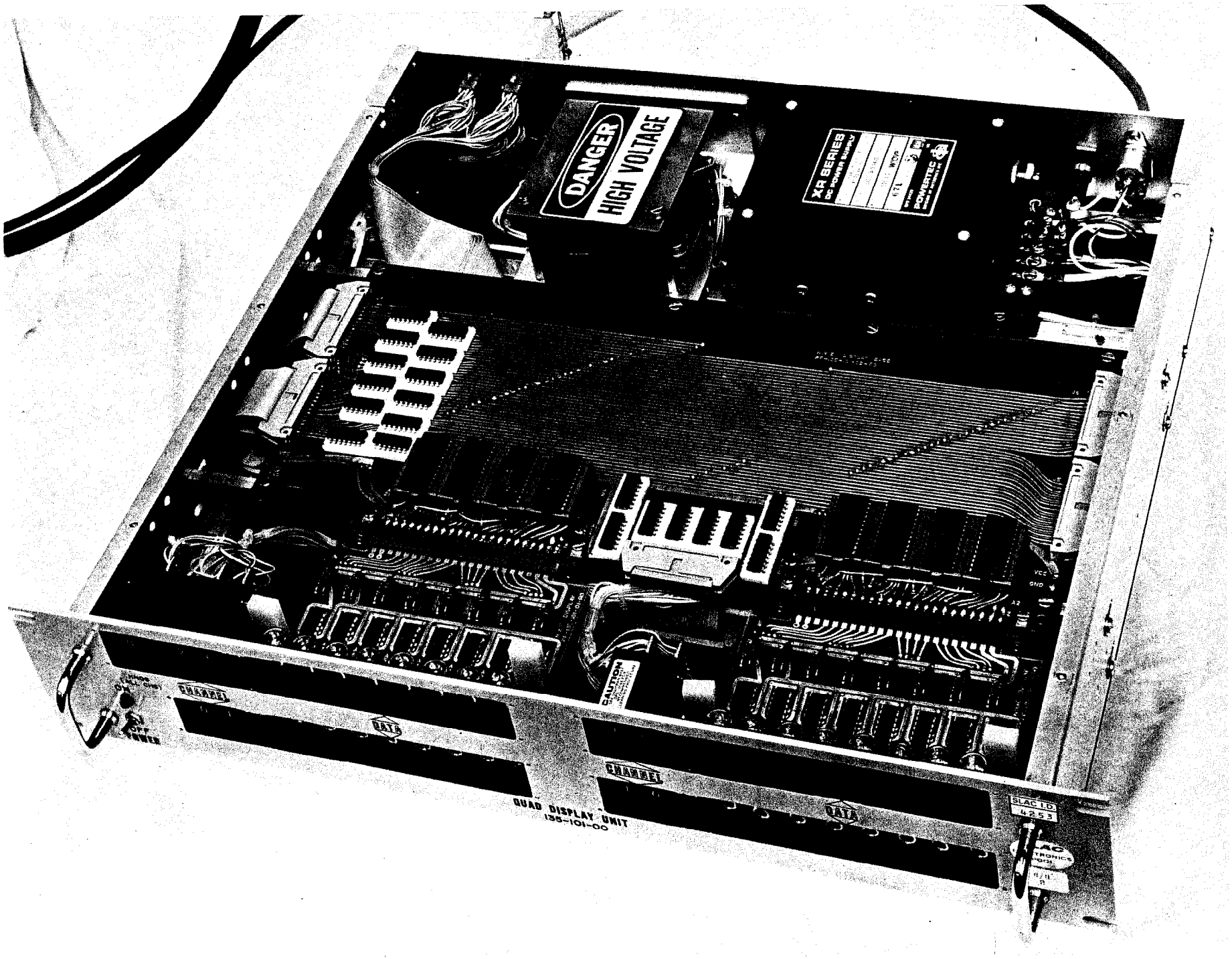

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FIG. 14--Photograph of the quad display unit.

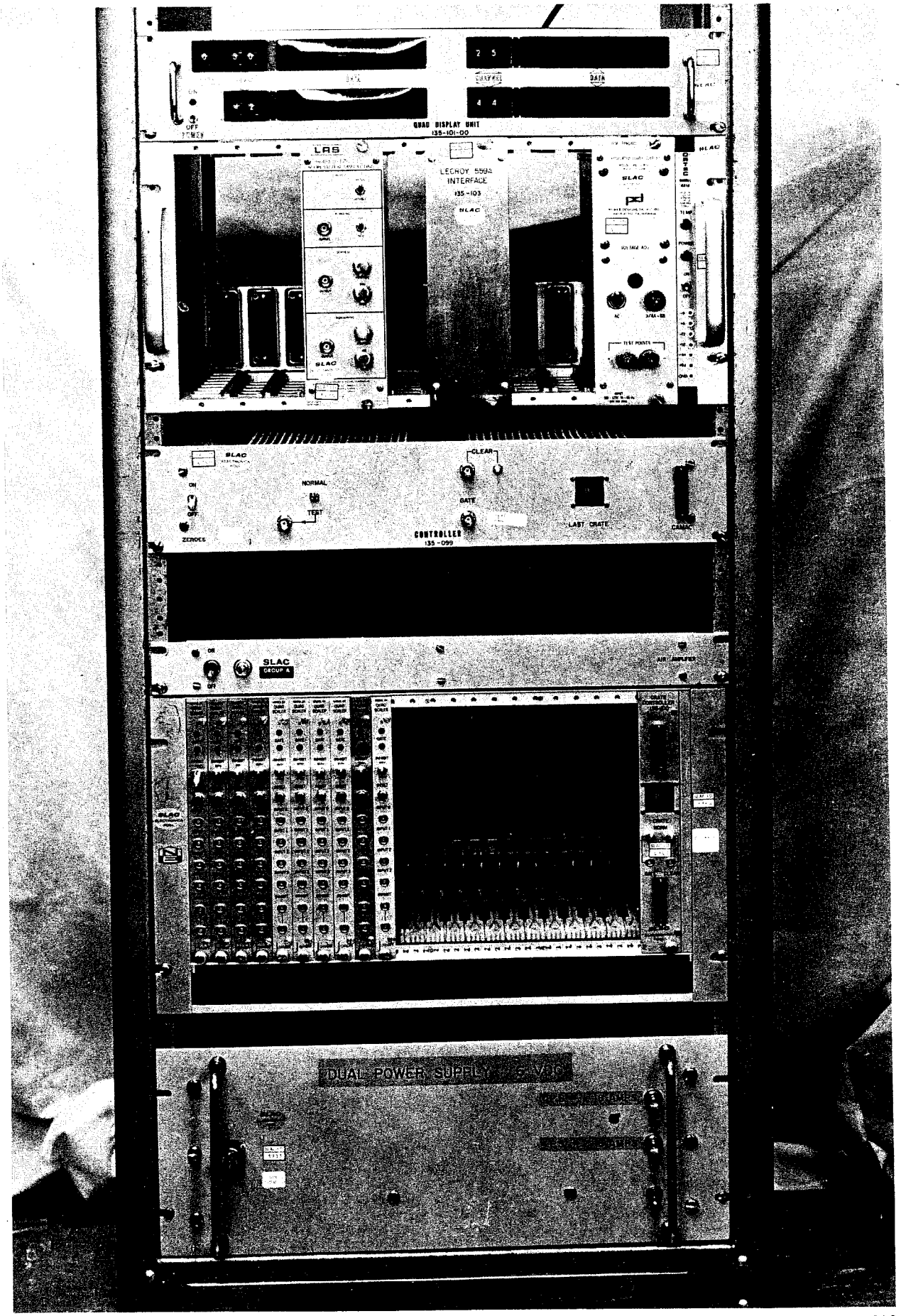

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FIG. 15--Photograph of the system.