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COMMENT ON "DECADE RATE MULTIPLIER"[1]

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ABSTRACT

The referenced letter suggests a method of achieving a decade rate multiplier with evenly spaced output pulses. This letter shows that the proposed technique can be implemented in a straight forward manner using integrated circuit divide by N counters.

(Letter to the Proceedings of the IEEE.)

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[1] V. C. V. Pratapa Reddy and M. P. Rajappan, "Decade Rate Multiplier", Proc. IEEE (Lett.) Vo. 60, N. 6, p. 759, June, 1972.

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The above named correspondence describes a technique for constructing a rate multiplier that produces equally spaced output pulses. Included in the correspondence is a block diagram implementing the technique with subcounters and various control gates. The purpose of this letter is to describe a more general implementation of the same technique using IC divide by N counters such as the Motorola MC4016 decade divider. The data sheet describes how these can be cascaded to produce a division by arbitrary N, where N is directly programmed by BCD inputs.

For example, to construct a rate multiplier for $x = 0 \rightarrow 9$, where the lowest common multiple is $5x7x8x9 = 2520$, it is necessary to use a 4 stage decade divide by N chain. For $x = 0 \rightarrow 9$, the necessary division ratios are given below:

x	N	x	N
0	0	5	504
1	2520	6	420
2	1260	7	360
3	840	8	315
4	630	9	280

For each x it is only necessary to program the inputs of the stages with the required BCD code using a ROM, a hardwired matrix, conventional gates, or manual switches as may be appropriate.

The advantage of this method of implementation is that it is completely general for any x, and requires no custom logic design for each case. Furthermore the number of IC's, and number of interconnections is reduced from the previous method.