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A COMPUTER SYSTEM FOR MULTIPARAMETER PULSE HEIGHT ANALYSIS AND CONTROL*

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Summary

A multiparameter pulse height analyzer and computer control system is described. Features include individual peak hold detectors with a time-shared ADC front end driving a PDP-9 computer to measure time-of-flight and light intensity from 12 scintillation counters around the 40-inch hydrogen bubble chamber.

Introduction

A data acquisition system consisting of time-of-flight scintillation counters, associated electronics, and a PDP-9 computer, has been developed for use with the SLAC 40-inch hydrogen bubble chamber (HBC).[1] The system is designed to give optimum timing resolution subject to the geometrical limitations of the current HBC design. During the experiment the HBC is expanded at a constant rate but the camera is triggered so that picture taking occurs only when an event of interest is detected. Since the camera is capable of taking over 1 mile of 70 mm film per hour, the cost saving potential is considerable.

The idea is to send data from the scintillation counter array (Fig. 1) into the PDP-9 computer while bubbles from the charged interaction tracks grow in the HBC. The PDP-9 scans this data, deciding whether an event of interest has taken place. If the computer decides an interesting event may have occurred, it triggers the camera lights.

High energy physics experiments in the past several years have become more complex requiring precise measurement of pulse height information from a large number of sources. The wide acceptance of digital computers with magnetic tape transports has provided a means to record this data. Conventional systems[2] use one ADC per source with the outputs multiplexed into the computer. The system described here significantly reduces the cost by time sharing these inputs with one ADC having a channel resolution of 4096.

Overall System

The system was intended to be used initially to measure momentum for a beam of neutral K_2^0 mesons and neutrons and is shown schematically in Fig. 2. The K_2^0 beam has a momentum spectrum that runs from 1 to 10 GeV/c with the majority between 2 and 6 GeV/c.[3] The primary electron beam from the Stanford Linear Accelerator hits a beryllium target 55 meters upstream from the 40-inch HBC producing K_2^0's and neutrons. The accelerator is operated so that 10 picosecond long bunches of electrons hit the target every 50 nanoseconds.[4] The arrival time of the electron beam on target is sensed by a beam pick off cable mounted just after the target. The arrival time of those neutral beam particles which send charged interaction products out through the HBC walls is sensed by the scintillation counters. The scintillators overlap one another so that each charged interaction product that goes through the counters causes two independent pulses to be sent to the electronics.

For the first pulse from each PMT the electronics measures the time differences between the beam pick off signal and the PMT pulse and the integrated charge of the PMT pulse. A firing pattern representing scintillator hits versus a particular beam bunch is also measured. This time difference (of 0 to 50 ns) is measured by starting and stopping a capacitor charging from a constant current source.† The integrated charge of the PMT pulse is measured by a linear gate. These analog signals are then held in a peak hold circuit and multiplexed into a 12-bit 200 MHz linear ramp analog to digital converter (ADC).†† The firing pattern consists of a bank of flip-flops, correlating which counters fired for each event. The time resolution of the electronics into the computer is better than 70 ps full width at one-tenth maximum.

The above information for each picture is read into a PDP-9 computer and recorded on magnetic tape. Histograms of the counter information are prepared and updated by the computer for continuous monitoring of the experiment. The histograms can be displayed on a display scope or teletype upon request by the experimenter. The PMT voltages, roll and frame numbers of the HBC photographs and beam conditions (parameters) are also automatically recorded by the computer. The data read-in takes 1.6 ms; this leaves time to execute a few hundred instructions before the final decision must be made. The normal light delay for the 40-inch HBC is about 2.75 ms.

Pulse Height Analysis

The peak hold (Figs. 3 and 4) has two modes of operation — sensing the top of an essentially flat pulse, representing time-of-flight from an EG&G TH200 and sensing the peak of a 1.5 μs linear gate output pulse. The technique is to charge a holding capacitor through a high gain differential amplifier using a buffer amplifier to sense the output voltage. F1 is an FET differential input stage driving the differential comparator A1 which switches Q_1 off and Q_2 on until the holding capacitor voltage is equal to the input voltage. The charging current is switched fast through the gold doped diode D2 and low drift is assured by the high impedance of D3. The output is driven by the buffer amplifier A2.

A greater charging current is provided in the amplitude mode which allows for many comparisons along the leading edge. The time pulse, however, is a flat pulse and requires only one interception. A +14 volt gate generator signal is sufficient to reset the peak holds prior to the input signal. The peak hold drifts at a rate of +25 millivolts/second. The computer reads the ADC on a high priority such that the voltages are always read at the same delay time to minimize the affects of drift.

The 40-point multiplexer, using REDCOR 770-730 multiplexers, ADC, and the controller are shown in Fig. 5. The multiplexer is reset prior to read in and then the computer ready pulse signals the ADC to digitize the selected analog signal. The ADC finished pulse to the computer advances the multiplexer providing a maximum settling time. The ADC is stabilized, internally, by periodically making a digital measurement against a built in reference and then correcting the gain. This condition is sensed and the computer read in is inhibited during this time.

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†EG&G TH200

††HP 6416A

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Computer Interface and Hardware

Our group purchased the PDP-9 in the spring of 1969 prior to the first PDP-15. We decided to use DEC cards for all data channel and device selector controls. These control signals and the data bus were shifted to TTL levels providing a flip-flop register for each output device word and a set of open collector gates for each input device word, thereby providing an interface similar to an SEL 810/B or an XDS sigma 3. Each device plugs into the interface panel and may be located any place in the control room. A typical controller for reading scalers is shown in Fig. 6. The controllers basically send data only to the computer and we have not found a need for a two-way data bus. In fact, it appears much cheaper and more reliable for this type of data acquisition system to build large systems such as the ADC, scalers, and buffer registers which have only computer data input capability. The interface proved quite flexible allowing blind scalers to be interfaced in a couple of hours during a run when the beam was off. The main disadvantage being that the interface panel must be worked on in place.

With a limited computer budget of $50,000 the PDP-9 offered 8 K of memory and the two required mass storage devices using DEC tapes. One tape is used for program storage and the other for data. Later we purchased a DEC mag tape controller and interfaced an existing IBM 2401 75 IPS mag tape. IBM provides essentially the raw read signal and we built the buffer amplifiers, precision rectifiers and peak zero crossing detectors to perform the deskewing in conjunction with our control circuit. The system is compatible with the DEC software and performs all the data reliability tests. These tapes may be taken directly to the IBM 360/91 where the data is analyzed and correlated with data from the HBC pictures.

Test Results

The pulse height resolution of the electronics is shown in Fig. 7 by 2 histograms displaced by approximately 350 picosecond. The accelerator RF was used to start a TAC and a cable in the beam used to stop it. After the first peak was obtained the accelerator operation was changed such that the electrons came in the next earlier RF cycle or approximately 350 ps earlier and the second peak obtained. Figure 8 shows a typical channel deviation from a straight line when the system was calibrated with a mechanical delay line.

Acknowledgements

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References

1. W. E. Smart et al., "Description of a Scintillation Counter Data Acquisition System for use with the SLAC 40-Inch Hydrogen Bubble Chamber," Dubna Instrumentation Conference, 1970 (to be published).

2. D. Porat and K. Hense, Nucl. Instr. and Methods 67, 229-239 (1969).

3. A. D. Brody et al., Phys. Rev. Letters 22, 966 (1969).

4. R. F. Koontz and R. Miller, Stanford Two Mile Accelerator, edited by R. B. Neal (W. A. Benjamin, New York, 1968), pp. 256-259.

Figure Captions

FIG. 1--Scintillation counter array.

FIG. 2--System block diagram.

FIG. 3--Peak hold circuit.

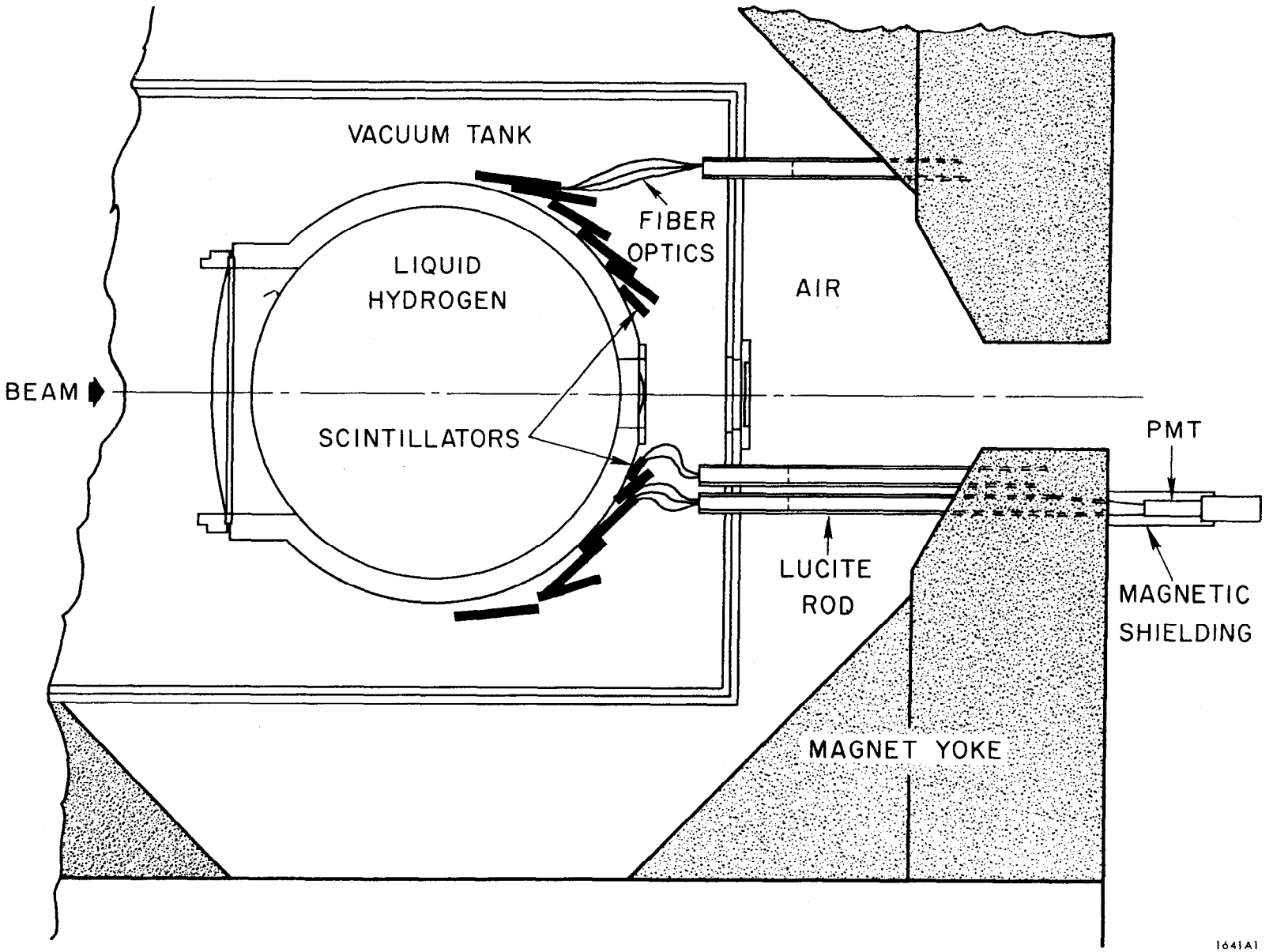
FIG. 4--Peak hold photograph.

FIG. 5--ADC and controller photograph.

FIG. 6--TSI controller photograph.

FIG. 7--Time resolution histogram.

FIG. 8--Straight line deviation.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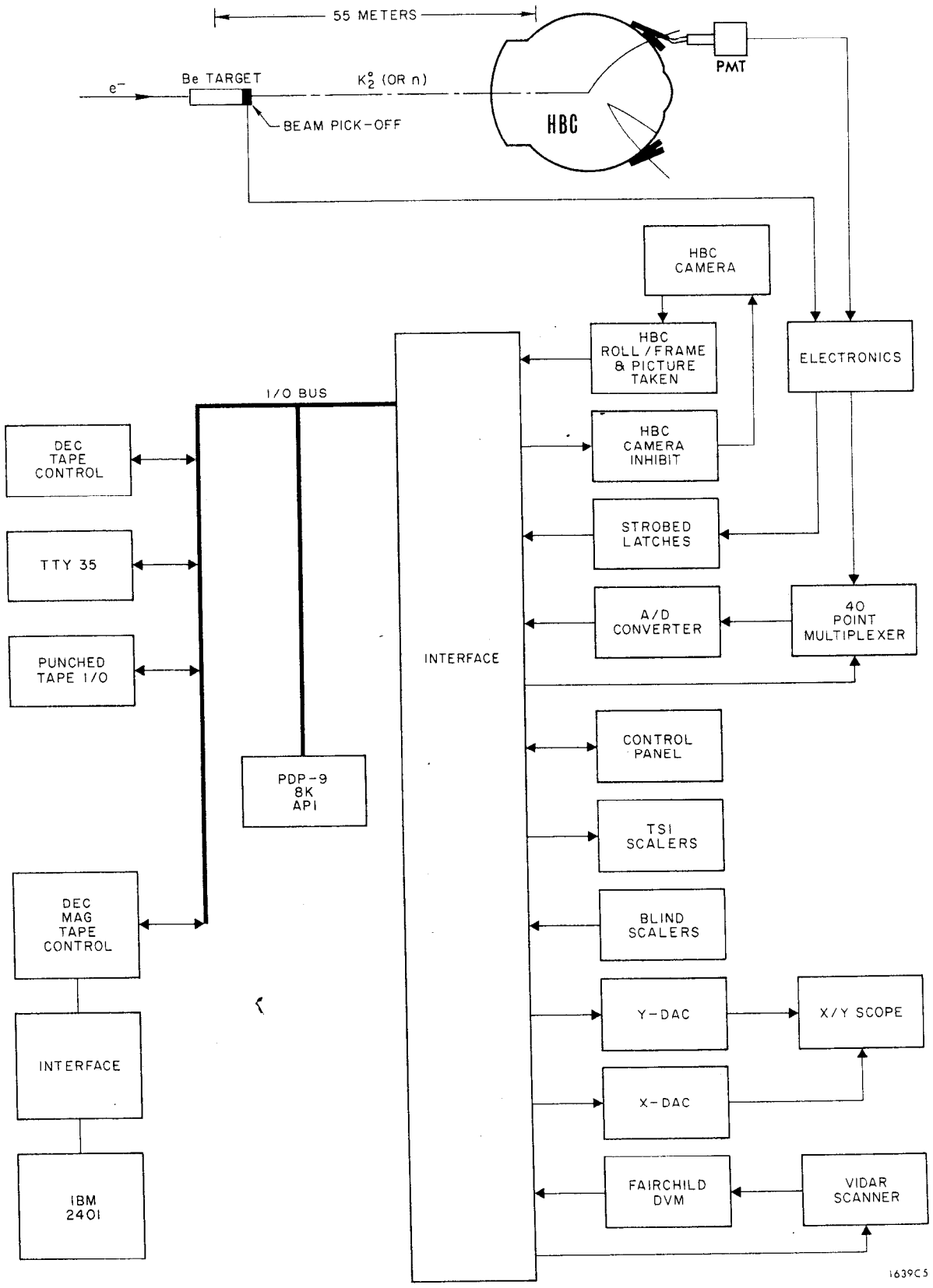
SHIELDING
MAGNET YOKE
1641A1

Fig. 1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HBC CAMERA
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HBC CAMERA INHIBIT
STROBED LATCHES
A/D CONVERTER
40 POINT MULTIPLEXER
ELECTRONICS
I/O BUS
INTERFACE
DEC TAPE CONTROL
TTY 35
PUNCHED TAPE I/O
PDP-9 8K API
CONTROL PANEL
TSI SCALERS
BLIND SCALERS
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X/Y SCOPE
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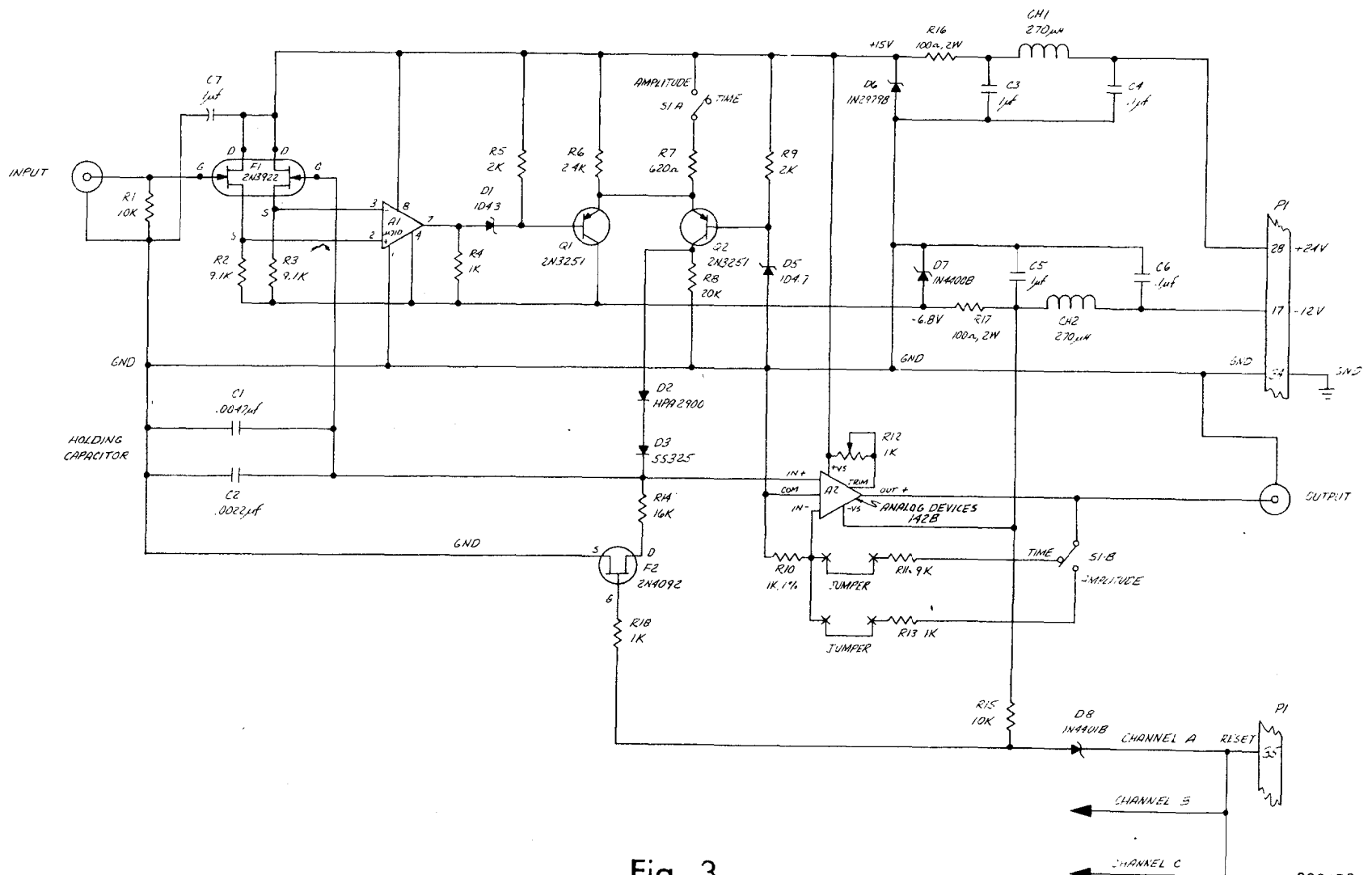
DEC MAG TAPE CONTROL
INTERFACE
IBM 2401
1639C5

Fig. 2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C7 1μf
F1 2N3922
R2 9.1K
R3 9.1K
A1 μ710
R5 2K
D1 1D43
R4 1K
R6 2.4K
Q1 2N3251
R7 620Ω
AMPLITUDE
S1A
TIME
Q2 2N3251
R8 20K
R9 2K
D5 1D47
+15V
R16 100Ω, 2W
CH1 270μH
D6 IN2979B
C3 1μf
C4 .1μf
D7 IN4008
C5 1μf
C6 .1μf
-6.8V
R17 100Ω, 2W
CH2 270μH
P1
28 +24V
17 -12V
24 GND
GND
GND
GND
GND
C1 .0047μf
C2 .0022μf
HOLDING CAPACITOR
D2 HPA2900
D3 5S325
R14 16K
F2 2N4092
R18 1K
R12 1K
A2 1428
IN+
COM
IN-
+VS
TRIM
OUT+
-VS
ANALOG DEVICES
OUTPUT
R10 1K, 1%
JUMPER
R11 9K
R13 1K
JUMPER
TIME
S1B
AMPLITUDE
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D8 IN4001B
CHANNEL A
RESET
P1
35
CHANNEL B
CHANNEL C

Fig. 3

2004D2

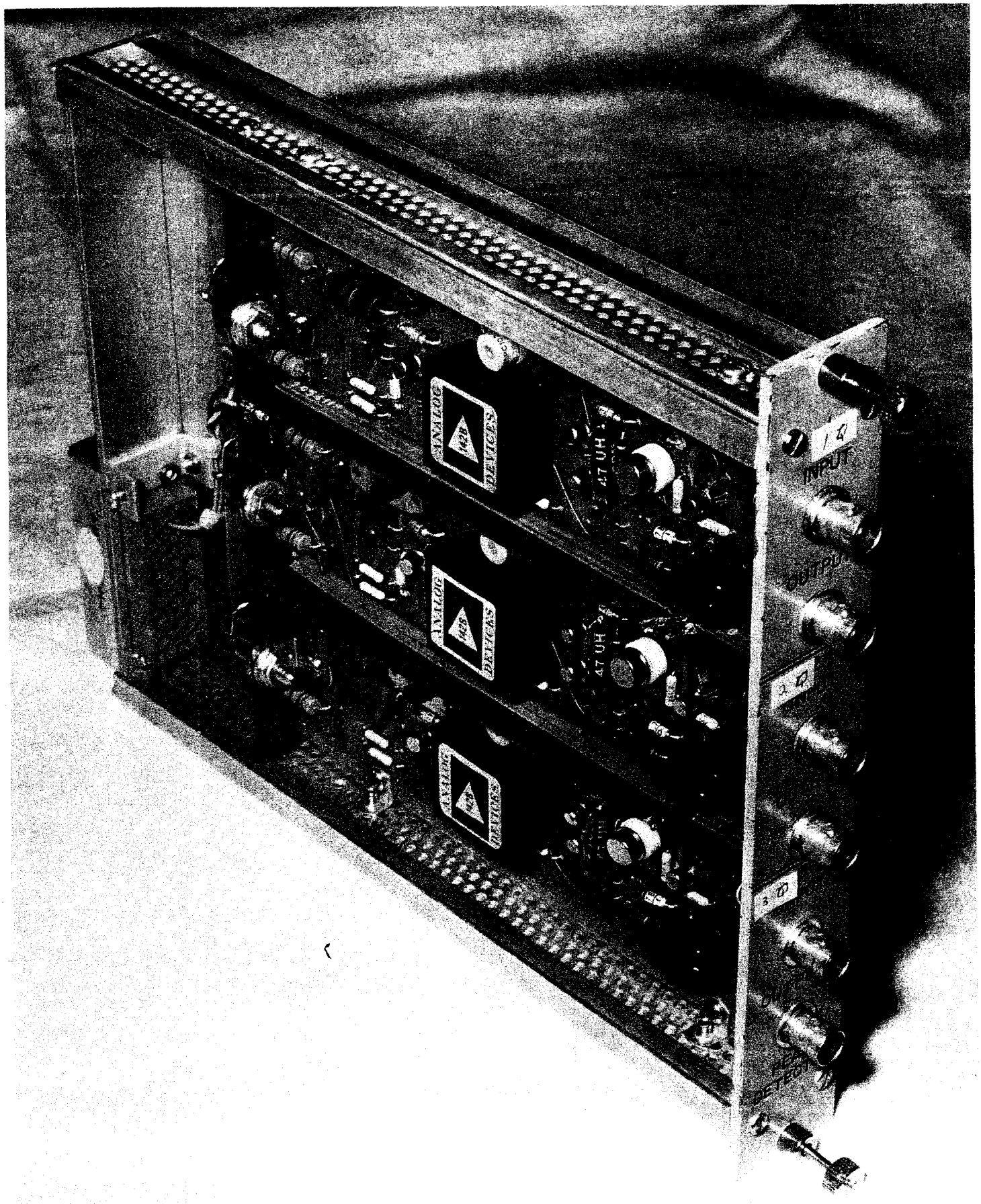

Fig 4

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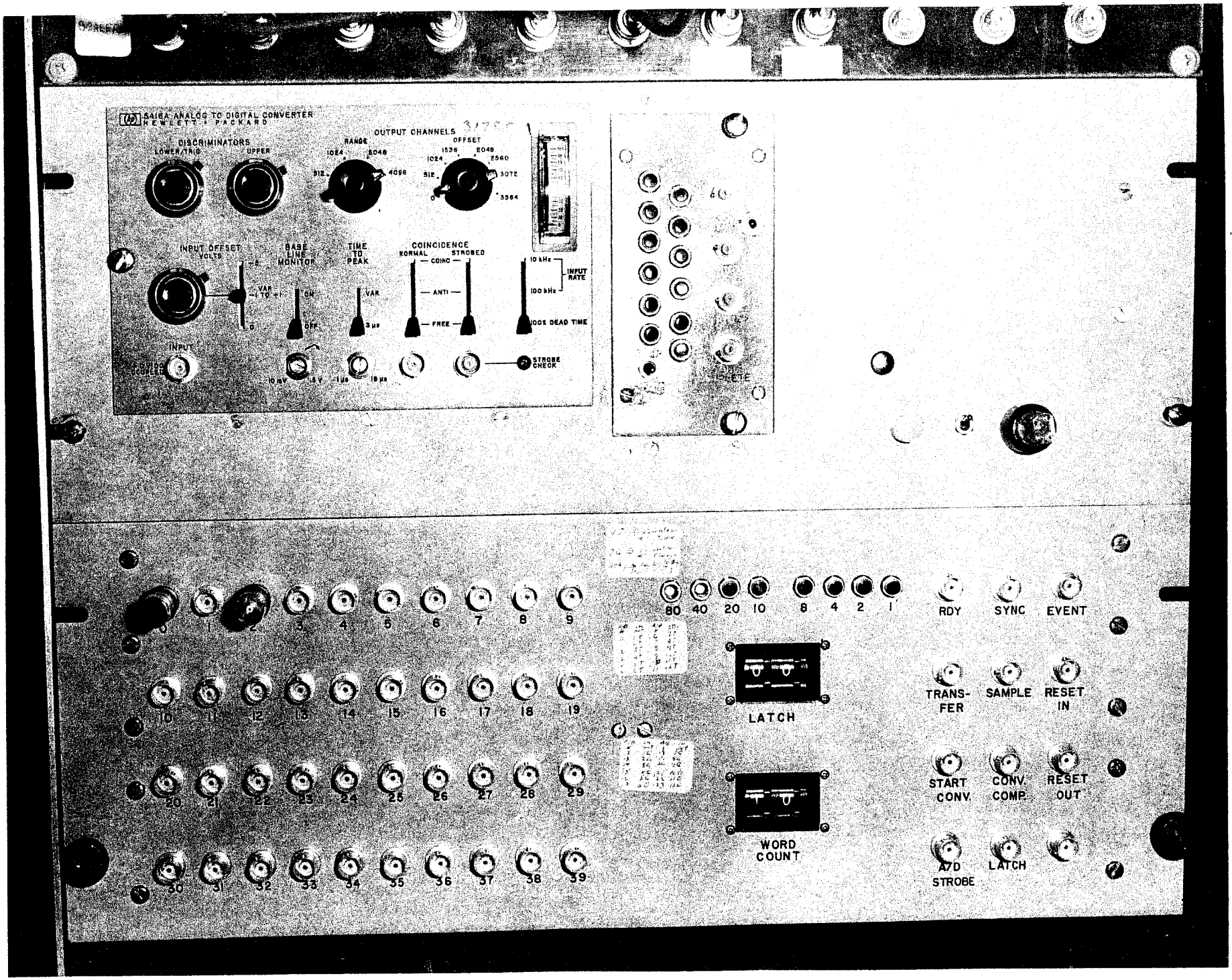

Fig. 5

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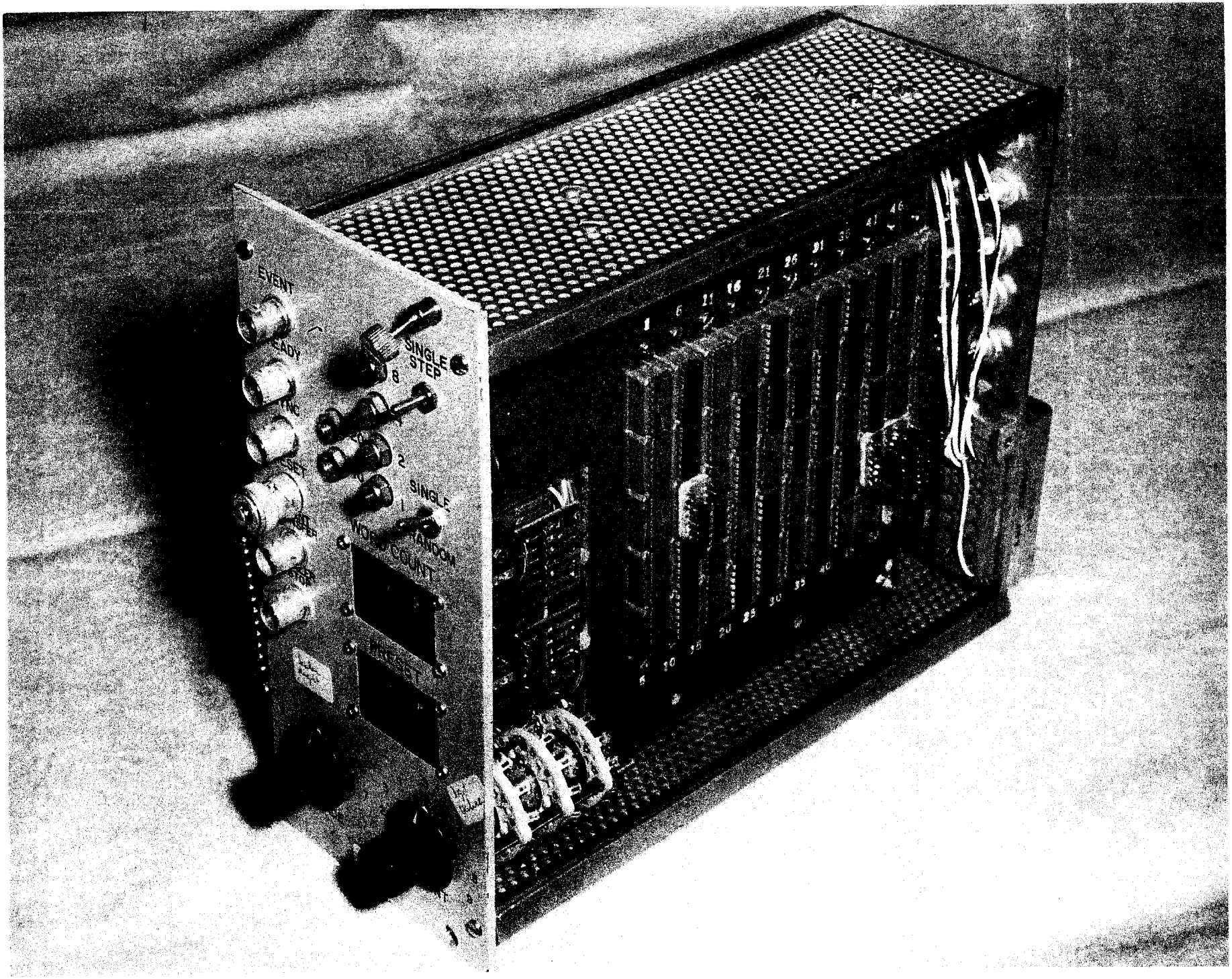

Fig. 6

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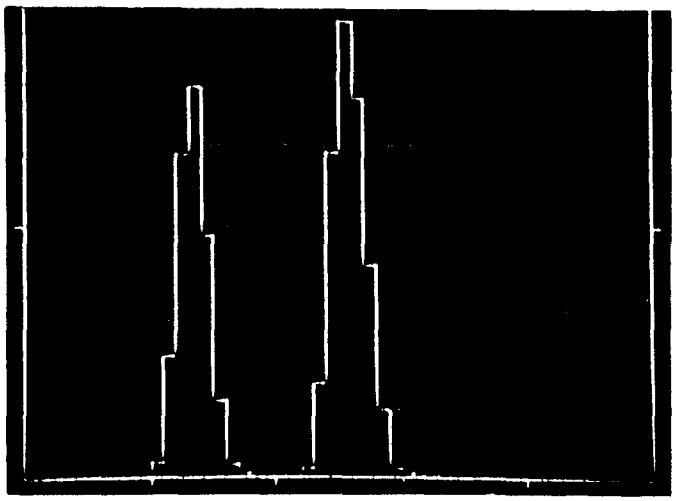
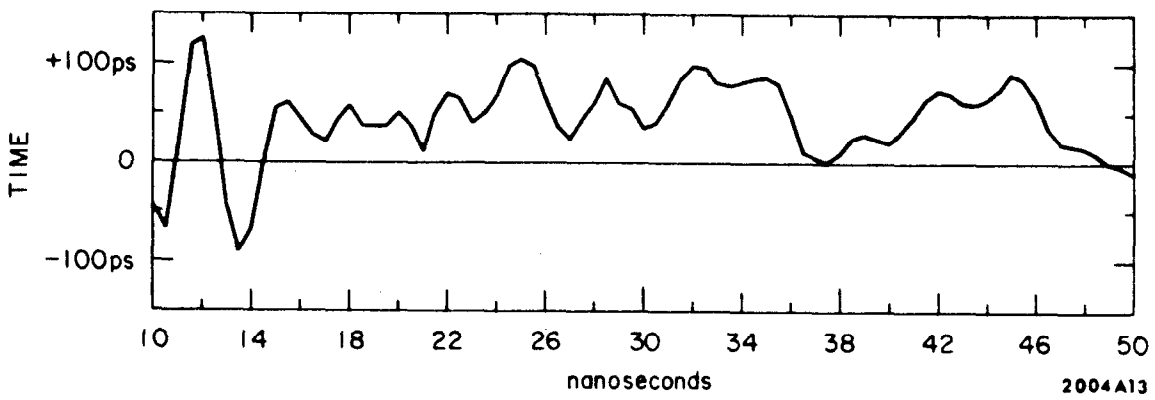


Fig. 7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nanoseconds
2004A13

Fig. 8