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INTERLABORATORY DEVELOPMENT OF AN INTEGRATED CIRCUIT FOR MULTIWIRE PROPORTIONAL CHAMBERS*

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1. Introduction

In October, 1970, a small group met at the Lawrence Radiation Laboratory in Berkeley to discuss the possibility of collaborating on the development of a special integrated circuit for proportional wire chambers. Attendees of this initial meeting were H. Steiner and F. Kirsten of LBL, M. Atac of NAL, R. Lanza of MIT, A. Minten of CERN, and J.-L. Pellegrin and the writer of SLAC. It was decided to organize a more general followup meeting in conjunction with the Nuclear Science Symposium in New York in November, 1970. H. Steiner mailed invitations to all known interested laboratories, and also to two semiconductor manufacturers, Fairchild Semiconductor in Mountain View, California and Motorola Semiconductor in Phoenix, Arizona.

The two day meeting, held on November 2-3, 1970, was attended by about 60 people from essentially every major laboratory, including CERN. The first day was devoted to formal presentations, and the second to a roundtable discussion involving manufacturers' representatives together with several laboratory representatives.

The final consensus of the New York meeting was that a subgroup should be formed to produce a specification with which to solicit manufacturers' proposals. Thus, immediately after the New York meeting, a subcommittee met at LBL to consolidate a specification. Participants in this effort were: M. Atac, NAL; H. Steiner and F. Kirsten, LBL; I. Pizer and F. Sauli, CERN; R. Lanza, MIT; T. Nunamaker, University of Chicago; and J.-L. Pellegrin and the writer, SLAC. A preliminary specification[1] was subsequently issued from LBL on November 20, 1970.

Following the subcommittee meeting at LBL, the writer was delegated the responsibility of submitting the specification to manufacturers, and of coordinating all proposals. This effort has essentially been continuous since the early part of December, 1970. The major developments to date and the general status of the project are summarized in the remainder of this paper.

2. Summary of the Specification

The general features of the preliminary specification are presented in the circuit of Fig. 1, the timing diagram of Fig. 2, and the specifications summary of Table I.

Figure 1 is the functional block diagram of a typical channel based on a horizontal partitioning of the circuit. The negative-going wire signal enters an amplifier or comparator having an adjustable gain or threshold. The amplified output, which is now a logic level, is shaped to a constant width before triggering a monostable. The shaper output is also passed through an open collector buffer to provide the FAST output.

The monostable output enters another shaper ahead of a WRITE gate, the output of which sets a bistable. The bistable output is passed through an open collector READ gate to form the final data output. The bistable output is also made available directly through an open collector buffer. The schematic also shows the monostable output to be available. The monostable timing elements are shown to be external to the integrated circuit.

*Work supported by the U. S. Atomic Energy Commission.

The corresponding waveforms are shown in Fig. 2. The main points are that the propagation delay to the FAST output is shown as ≤ 40 ns; the shaped outputs are shown as 30 ± 10 ns; the monostable delay is shown as 100 ns to 10 μs, adjustable by external RC; and the monostable recovery time is shown as $\leq$ the output pulse length. These various specifications are included in the summary of Table I.

3. Interpretation of the Specification

Several aspects of the specification should be noted. First, it was not explicitly required to use TTL as opposed to ECL logic; nor to use horizontal rather than vertical partitioning of functions. It was recognized that either of these options might have distinct advantages when the detailed design is considered. Also, although the original idea was to develop a monolithic circuit, the option of a hybrid circuit was left open.

The one major technical decision inherent in the specification is that a monostable shall be used for the delay element. If horizontal, rather than vertical, partitioning is used, then the monostable becomes an inseparable part of the circuit, and no other form of delay (such as a passive transmission or delay line) can be used. This was a basic decision made at the original New York meeting.

A second technical point is that the original specification called for a minimum input threshold of 5 ± 2 mV. This reflects the feeling at the time that the so-called "magic" gas mixtures would be generally used in future, and that the 0.5 to 1 mV thresholds required for other gases such as Ar-CO_2 would not be necessary. At a proposal review meeting at SLAC on April 13, 1971, this part of the specification was changed to read "1 mV typical, 2 mV maximum", reflecting the later consensus that a circuit with a lower threshold would be more generally applicable.

The functional block diagram of the specification is intended as a guide for manufacturers, and not to dictate the exact method of implementation. For example, the amplifier gate after the first shaper, and the monostable direct output gate, are clearly not fundamental to the operation of the circuit. Since extra pins on an integrated circuit are costly, these may not be included. Also, the monostable timing elements are shown to be external in order to provide a wide range of output width control. Experience with setting of individual circuit delays has shown, however, that to require setting of delays externally is intolerably costly and time-consuming for the user. A much more desirable situation is to have the manufacturer trim the delays internally at 300 ns $\pm$ 2%, and to have a group delay control through a single pin out of each package.

A further important consideration which may affect the final design is power consumption. In general, additional speed and complexity increase the power required, and in a system of tens of thousands of wires, the power distribution and circuit cooling problems can be serious. This point will be discussed later in more detail.

4. Proposal Review

In December, 1970, the specification was sent to 5 manufacturers: Motorola, Fairchild and Texas Instruments in the U.S.; Valvo-Phylips in Germany; and SESCOSEM in France. All companies responded except Valvo-Phylips.

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Motorola expressed interest, but stated that their facilities were loaded and they could not consider the job until April. Fairchild indicated that a formal proposal for a monolithic would be forthcoming. Texas Instruments indicated a similar intention. SESCOSEM also eventually submitted a proposal for a monolithic.

There ensued a lengthy period of negotiation in order to secure formal proposals. Fairchild's original plan to submit a proposal for a monolithic collapsed because of lack of support from various internal departments involved. The Texas Instruments effort was delayed first because of a management change, and second when CERN independently requested a proposal for a hybrid.

Finally, on February 25, 1971, a proposal for a monolithic development was received from Texas Instruments, and on March 10, a followup proposal for a 2-channel hybrid was received. On March 29, Fairchild also submitted a hybrid proposal. In view of these developments, the existing MECL circuit developed by Pellegrin at SLAC was submitted to Motorola in order to obtain a quotation on a hybrid; the verbal quotation was received April 12, just prior to a review meeting held at SLAC on April 13. (The formal quotation was received on April 19, 1971.) Also, just prior to this meeting, SESCOSEM submitted their proposal for a 3-chip vertically integrated monolithic.

A proposal review meeting was held at SLAC on April 13, 1971. Attendees were: M. Atac and Ron Martin, NAL; T. Nunamaker, University of Chicago; Ray Martin, LASL; R. Lanza, MIT; B. Jackson, F. Kirsten, H. Steiner, J. O'Keefe, S. Parker, LBL; and J.-L. Pellegrin and the writer, SLAC. The various circuit options which were considered are shown in Table II. The main points of interest are as follows:

1. Development of a monolithic will cost about $40,000. Production cost is projected at $2 - $3/channel.

2. Cost of a TTL hybrid from Fairchild or Texas Instruments is projected at $4 - $5 in 100,000 quantities.

3. The Motorola quotation on TEDDY of $10.37/channel is not competitive.

4. The SESCOSEM proposal contained no indication of method of implementation.

5. Information on CERN quotations was included for interest only. No formal proposals were received from Phylips or GE-Marconi.

The major decision of the meeting was to concentrate further efforts on developing a TTL hybrid version of the circuit, to be followed by a monolithic at a later time. This decision was made principally because of the shorter development time and lower development cost for a hybrid, plus the lack of encouragement from any manufacturer for an ECL hybrid or monolithic. The projected production cost of the TTL hybrid of the order of $5/channel in large quantities was considered sufficiently attractive to solve the short-term requirements. It should be emphasized, however, that the ultimate goal is to attempt to develop a monolithic, in order to achieve lowest possible costs as well as optimum reliability. The hybrid of course may point out problems which make further development of a monolithic impractical or economically unattractive; however, this possibility will be investigated thoroughly.

As noted previously, the threshold requirement was changed to 1 mV typical, 2 mV maximum. The meeting concluded with the decision to pursue further development of a TTL hybrid with both Fairchild and Texas Instruments, with the added requirement of a lower threshold voltage.

At that time it was estimated that the most optimistic date for delivery of production hybrids would be about September 1, 1971. This assumed minimal delays in obtaining proposals and evaluating breadboards.

5. Specification Review

Several additional points concerning the specification were discussed at the April 13 meeting:

1. The preferred input circuit specification was changed to make $1\ K\Omega \leq Z_{in} \leq 2\ K\Omega$. Protection is required as originally specified.

2. Crosstalk — 100 times overdrive on one channel should not cause triggering of adjacent channels.

3. Delay time — Monostable delay must be accurate to ±2.5%, adjustable 100 ns to at least 500 ns. If internal trimming only is used, it should be performed at a setting of 300 ns.

4. Channels should not respond to positive pulses of 100 times over threshold.

These points were subsequently relayed to Fairchild and Texas Instruments by letter.

6. Prototype Testing

At the April 13 meeting the following standard tests were suggested for evaluating prototypes:

1. Threshold vs. pulse width
2. t_{pd} to FAST out vs. V_{in}
3. Monostable delay jitter vs. Vcc, ΔT, rep rate
4. Coincidence curve at minimum WRITE gate width
5. Crosstalk for 40 db overdrive
6. Response to positive inputs
7. Operation in a 20 kG field
8. Operation on chamber-time resolution using $Ar\text{-}CO_2$

It was further agreed that a number of laboratories would independently evaluate the prototype before any final conclusion is reached. At the present time, 8 different laboratories are supporting the development effort and will be evaluating prototypes.

7. Status of Fairchild Proposal

A. Original Proposal

The original Fairchild proposal specified two packages, one containing 4 amplifier channels, the other containing 4 one-shots plus logic. The circuits are shown in Figs. 3 and 4. The package outline is shown in Fig. 5.

In June two prototype circuits of each type were delivered to SLAC. These units were developed from a design submitted to CERN by Fairchild's Weisbaden group in Germany. Tests on the amplifiers immediately revealed that the input thresholds were much higher than specified. This was traced to the fact that in the configuration used, current offsets inherent in the μA733 amplifier limited reliable thresholds to considerably higher than 10 mV.

The logic portion was given a cursory test. The main problem here appeared to be that there was an excessive spread in monostable delay between channels (±25 ns at a setting of 300 ns). This was apparently due to the fact that the delays had never been properly trimmed in the fabrication process. Another problem was that the OR outputs were not open-collector gates as called for in the specification.

In summary, the results of this unit were very unsatisfactory. The two units were sent to LBL and MIT for further

testing. In the meantime, the problems were reviewed with Fairchild, and a new development cycle initiated.

B. Current Proposal

Amplifier circuit. Immediately after the measurements on the original circuits, Fairchild began designing a new amplifier circuit based on the μA760, rather than the μA733. A single-channel breadboard of the circuit shown in Fig. 6 was subsequently delivered to SLAC. The circuit performance is summarized in Table III, and in Figs. 7 - 11.

Figure 7 was made by setting the TRIM potentiometer for a given threshold, and varying the THRESHOLD potentiometer. In the final version of the circuit, a single setting of the TRIM will be made internally for the lowest stable threshold, and the THRESHOLD control (which adjusts the hysteresis of the circuit) will be used to set the input threshold. The only change required to accomplish this is to increase the amount of feedback in the present circuit. The important fact to note in Fig. 7, however, is that the unit appears to operate stably down to a threshold of about 0.1 mV.

Figures 8 and 9 show the propagation delay from the fast input signal leading edge to the output leading edge, for the case of a shaped pulse input. The leading edge of the shaped pulse has a falltime of about 15 ns. The difference between the two curves is attributable to this falltime. In general, the delay and the incremental delay over a 10:1 input range (2 v_T to 20 v_T) are satisfactory.

Figure 10 shows the variation of v_T with temperature, and Fig. 11 the relative variation of propagation delay with temperature. Both characteristics appear very stable.

The unit was also tested with a large positive overdrive. A 3 volt, 1 ns T_R signal applied to the input produced no trigger at the output, with v_T set to 1 mV.

In general, this circuit appears very satisfactory as a front end for the hybrid. A slight modification to the hysteresis (THRESHOLD) control will be made before the breadboard is approved.

Logic circuit. No further work has been done on the original breadboard. However, Fairchild is now preparing a new logic circuit, including the following:

1. Wire-OR gates for the FAST and DIRECT outputs
2. Revised shaper circuits consistent with wire-OR outputs
3. A new, low-power monostable

The latter is desirable since the majority of power consumed in the logic portion goes into the one-shot. Different approaches are being investigated for inclusion in a future breadboard.

Power considerations. Based on the power consumption of the breadboard, a 4-channel amplifier package would consume about 1 watt. The original logic section consumed about 0.6 watts, for a total of 1.6 watts for 4 channels, or 0.4 watts per channel. For a 1000-wire chamber, the total power required would be 400 watts, or 80 amperes at 5 volts. Obviously, such high currents pose difficulties in distribution and in effective cooling of the circuits, and it is desirable to reduce power as much as possible without sacrificing performance significantly.

Two possibilities for reducing power consumption in the Fairchild circuit are being examined. First, the front end (μA760) may be operated at a lower voltage, with some sacrifice in gain, in order to reduce the power by about 40%. Second, it is hoped to use a lower-power monostable to reduce the logic section power requirements by a similar factor.

C. Contractual Agreement

The original Fairchild circuit, designed for the Weisbaden group, was furnished at no cost to the U. S. laboratories. For the second round of development, a purchase order has been placed through SLAC for 8 prototype hybrids, at a development cost of $8000. No hybrids will be constructed until after evaluation of at least a single-channel breadboard. The group of laboratories contributing to development costs are ANL, BNL, NAL, LBL, MIT, University of Chicago, University of Illinois, and SLAC. Delivery of hybrid prototypes has been quoted as 8-10 weeks after approval of a final breadboard.

8. Status of Texas Instruments Proposal

A. Original Proposal

The circuit originally proposed is shown in Fig. 12. The front end is an SN75107 comparator driving a conventional monostable and latch. The packaging proposed is 2 complete channels in a 24-pin dual in-line package.

This circuit was produced in response to the original specification requesting a 5 mV ± 2 mV threshold. Since this requirement was later changed, a new front end design was necessary. The circuit of Fig. 12 was therefore never breadboarded.

B. Current Proposal

The latest proposed circuit is shown in Fig. 13; a complete 2-channel breadboard was recently received and is presently undergoing evaluation.

This circuit is essentially identical to a unit which has been proposed for CERN, who have independently contracted with Texas Instruments for a unit to be used in the ISR detector. The circuit has several noteworthy features. First, the original SN75107 was found to be unsatisfactory even for the CERN requirement of a 5 mV threshold; therefore the circuit was re-designed around the SN72733. An attempt has been made to stabilize this amplifier for thresholds approaching 1 mV.

Second, a low-power one-shot has been employed, in order to minimize power requirements; this apparently introduces only a very small degradation in the timing performance.

Third, a special gate, consisting of two open-collector and two standard outputs, has been designed for the FAST and MEMORY-OR outputs. The standard outputs are used because in the former configuration using NAND gates with inverted logic inputs as NOR gates, the following problem arises: since the outputs must be normally low, each unit requires a pullup current through a resistor to Vcc. The OR signal shuts off this current, so that the risetime of the output is limited by the pullup resistor and the total circuit capacitance. This turns out to be a very slow response time, necessitating a lower pullup resistor, in turn resulting in higher power dissipation within the unit. Therefore the new circuit, as adopted by CERN, uses a standard totem-pole output to improve the speed, at the same time minimizing power consumption. The FAST output shaper has not been included, and the outputs are not directly wire OR-able.

This part of the circuit needs further study. For the U. S. version, it is hoped to retain the shaper, as well as a FAST output which requires no external buffering in order to form a group OR.

The results of some preliminary measurements are shown in Figs. 14 and 15. In Fig. 14, the incremental time delay as a function of input amplitude is seen to be in the order of 30 ns for a range of amplitudes of 2X to 20X over threshold, whereas the time delay for large amplitude is 45 ns for channel 1 and 30 ns for channel 2. In Fig. 15, relative delay curves are shown for the two channels at a nominal setting of 300 ns, using a 30 ns FWHM strobe width. The curves were made for an input amplitude of 6 mV. Note that on the breadboard unit, a common control for the two delays was not available; thus only relative delay measurements were possible. Note also that in the region of the skirts of the delay curve, the output amplitude oscillates between the zero and one states, due to the jitter of the monostable delay.

No temperature or stability tests have yet been made on this breadboard. It seems clear, however, that the amplitude dependence of the propagation delay, and the minimum achievable stable threshold, are somewhat inferior to the μA760 circuit.

C. Contractual Agreement

A purchase order has been placed through SLAC for 5 hybrid prototypes at a cost of $4500. The 5 laboratories supporting this effort are NAL, LBL, LASL, University of Chicago, and SLAC. The original Texas Instruments proposal quoted a delivery of 8 weeks ARO for the hybrids; this however is clearly contingent on delays in the evaluation of prototypes.

9. Production of Hybrid Units

The original plan of negotiating with at least two manufacturers was to maintain a competitive bidding situation for production units. The probable approach, at the conclusion of the hybrid prototype tests, will be to request proposals from each manufacturer for production quantities of his particular device. At the April 13 review meeting at SLAC, an attempt was made to totalize approximate yearly requirements from the major laboratories, based on known or planned experiments. The number appeared to be somewhere between 50K and 100K channels in the first year. Therefore it would appear reasonable to negotiate a blanket AEC contract based on a quantity of about 50K channels per year.

Once a contract is negotiated, either company will require about 8 weeks to reach a production volume of 2-3K units per week. The production rate of course will depend heavily on the total quantity of orders received. Prices will not be in the $5 range until quantities approaching 50K channels are reached.

Before a blanket order is placed, it will of course be necessary to obtain some reasonably accurate estimates, or preferably commitments, from the various laboratory users.

10. Summary and Conclusion

Progress has been made toward developing a special TTL hybrid integrated circuit for proportional wire chambers. Two manufacturers, Fairchild and Texas Instruments, both appear close to completing a satisfactory circuit. Deliveries of hybrid prototypes will require probably 6 to 8 weeks after final approval of the breadboards.

After successful conclusion of the hybrid project, the question of the possible development of a monolithic will be re-opened.

11. Acknowledgements

Many people from different laboratories have contributed to this project. It is hoped that the most important contributors have been mentioned at the beginning of this report. Particular credit should go to H. Steiner of LBL who initiated the first organization meeting; F. Kirsten of LBL who authored the original specification, and E. Cisneros of SLAC who performed the measurements reported herein.

12. References

1. "Multiwire Proportional Chambers. Preliminary Specifications for a Monolithic Integration of the Wire Electronics," Lawrence Radiation Laboratory, Berkeley, California, November 20, 1970.

TABLE I

SPECIFICATION SUMMARY

I.	Amplifier	
	Input	-5 mV to -500 mV, negative; T_F ~20 ns, T_R ~ 200 ns
	V_T	-5 mV to -100 mV ± 2 mV or ± 10%; T.C. 1%/°C 0° to 70°C
	Positive signals	Insensitive to +500 mV signals
	Protection	No damage for 100 pF at ±5 kV through 2,000 Ω
	Gain	4 mV change gives full output
	Fast out	Width 30 ± 10 ns, < 10 ns T_R, T_F delay ≤ 40 ns ± 20%
II.	Monostable Delay	
	Output pulse	Adjustable 100 ns to 10 μs; T_R, T_F ≤ 10 ns
	Propagation delay	T_{PD} ≤ 40 ns ± 20% from FAST out
	Temp. coeff. of width	< ± .05%/°C
	External R C trim	Required
	Power supply coeff. of width	≤ ± 1% for ± 10% change
	Duty Cycle	≤ 50%
III.	Gated Latch	
	Minimum write gate width	≤ 20 ns
	Minimum coincidence curve	≤ 40 ns
IV.	General	
	Outputs must be wire OR-able	
	No unusual cooling requirements	
	Direct out and gated out must be TTL compatible	
	Operating range 0° to 70° C	

TABLE II

PROPOSAL SUMMARY

	Manufacturer	Hybrid	Fixed Cost	Production Cost	Monolithic Fixed Cost	Cost/Ch	Package	Comments
1.	Texas	TTL	$4.6K	$4.3/ch 5 mV	$40K	$2.5-3.25 (100K)	Mono- 16 pin DIP 1 or 2 ch Hybrid- 24 pin DIP 2 ch	Hybrid t_{pd} to fast out =55 ± 10 ns > 20 ns write gate required
2.	SESCOSEM				$38.7K	$2.34 (100K)	3 - 16 pin DIP's per 4 ch	
3.	Fairchild	TTL	0	$5.4/ch (100K) 1 mV			2 - 1.4" × 0.9" ceramic + plastic lid/4 ch	
4.	Motorola	MECL	$7K	$10.37/ch (50K) 1 mV			1" × 1" ceramic per 2 ch	Not including MECL-TTL converter and output gates
5.	CERN (Phylips)	MECL		2.8 mV $5.8/ch (large Qty)			Not specified	Data from Pizer/ Verweij
6.	CERN (GE Marconi)	TTL	$1.8K	$8/ch 50K			Not specified	Data from Sauli via Kirsten

TABLE III

FAIRCHILD μA760 BREADBOARD MEASUREMENTS

Parameter	Value
Input Impedance (Z_{in})	2KΩ (Approx.)
Power Dissipation	16 mA at -8 V → 128 mW 24 mA at +5 V → 120 mW Total/Ch → 248 mW
Minimum Input Sensitivity (v_T)	0.1 mV
Output Risetime (T_R)	10 ns 10-90%
Power Supply Sensitivity ($\Delta v_T/\Delta Vcc$)	0.5 mV/V at v_T = 2 mV

Figure Captions

FIG. 1--Functional block diagram.

FIG. 2--Timing diagram.

FIG. 3--Fairchild proposal - linear section Mod 1.

FIG. 4--Fairchild proposal - logic section Mod 2.

FIG. 5--Fairchild package.

FIG. 6--Fairchild proposal — linear section Mod 2.

FIG. 7--Threshold vs. bias.

FIG. 8--Delay vs. input - no shaper.

FIG. 9--Delay vs. input - with shaper.

FIG. 10--Threshold temperature sensitivity.

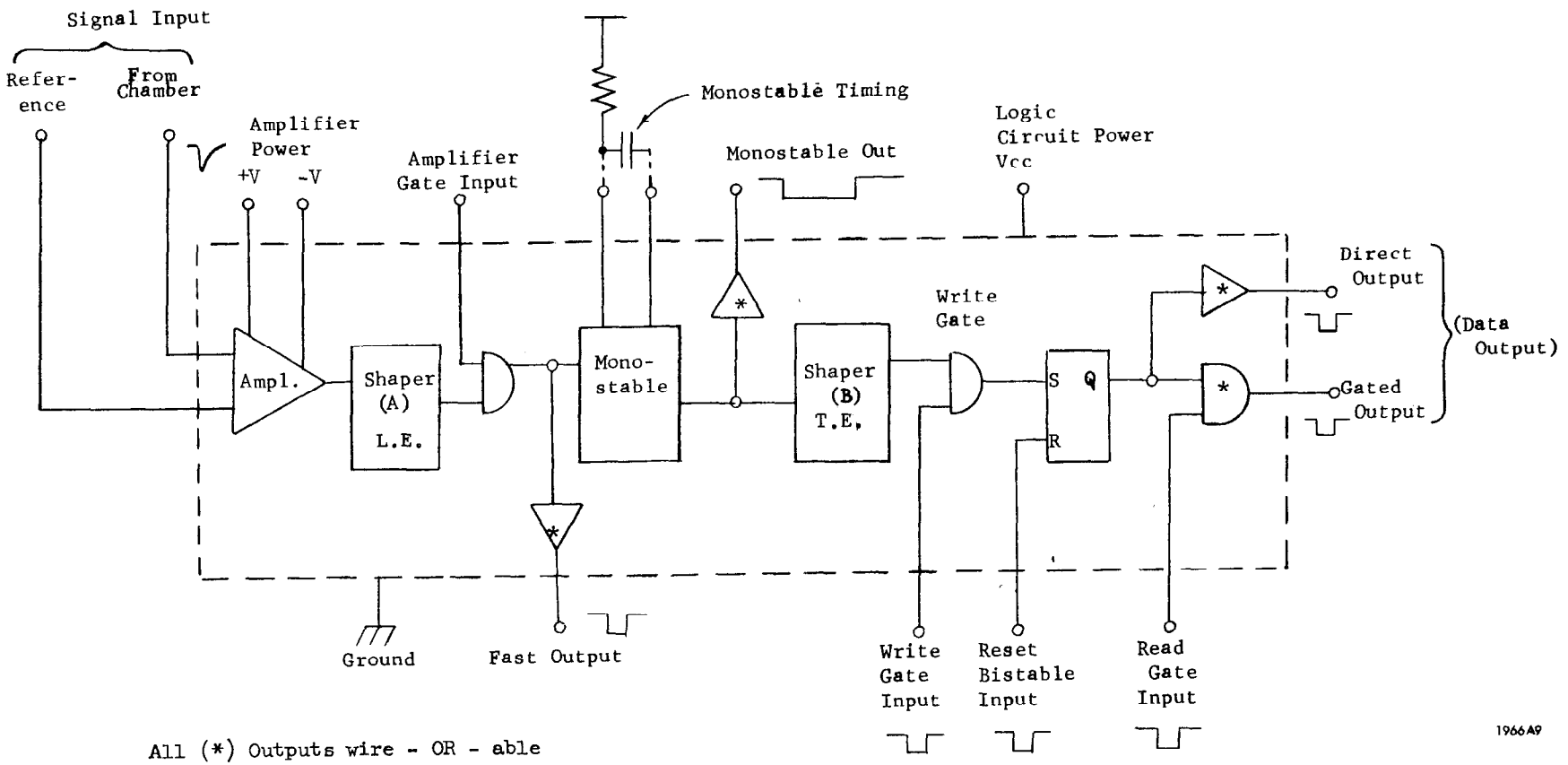
FIG. 11--Delay temperature sensitivity.

FIG. 12--Texas proposal Mod 1.

FIG. 13--Texas proposal Mod 2.

FIG. 14--Delay vs. input - with shaper.

FIG. 15--Output coincidence curve.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Refer-ence
From Chamber
Amplifier Power
+V
-V
Amplifier Gate Input
Monostable Timing
Monostable Out
Logic Circuit Power Vcc
Ampl.
Shaper (A) L.E.
Mono-stable
Shaper (B) T.E.
Write Gate
S
Q
R
Direct Output
Gated Output
(Data Output)
Ground
Fast Output
Write Gate Input
Reset Bistable Input
Read Gate Input
All (*) Outputs wire - OR - able
1966A9

Fig. 1

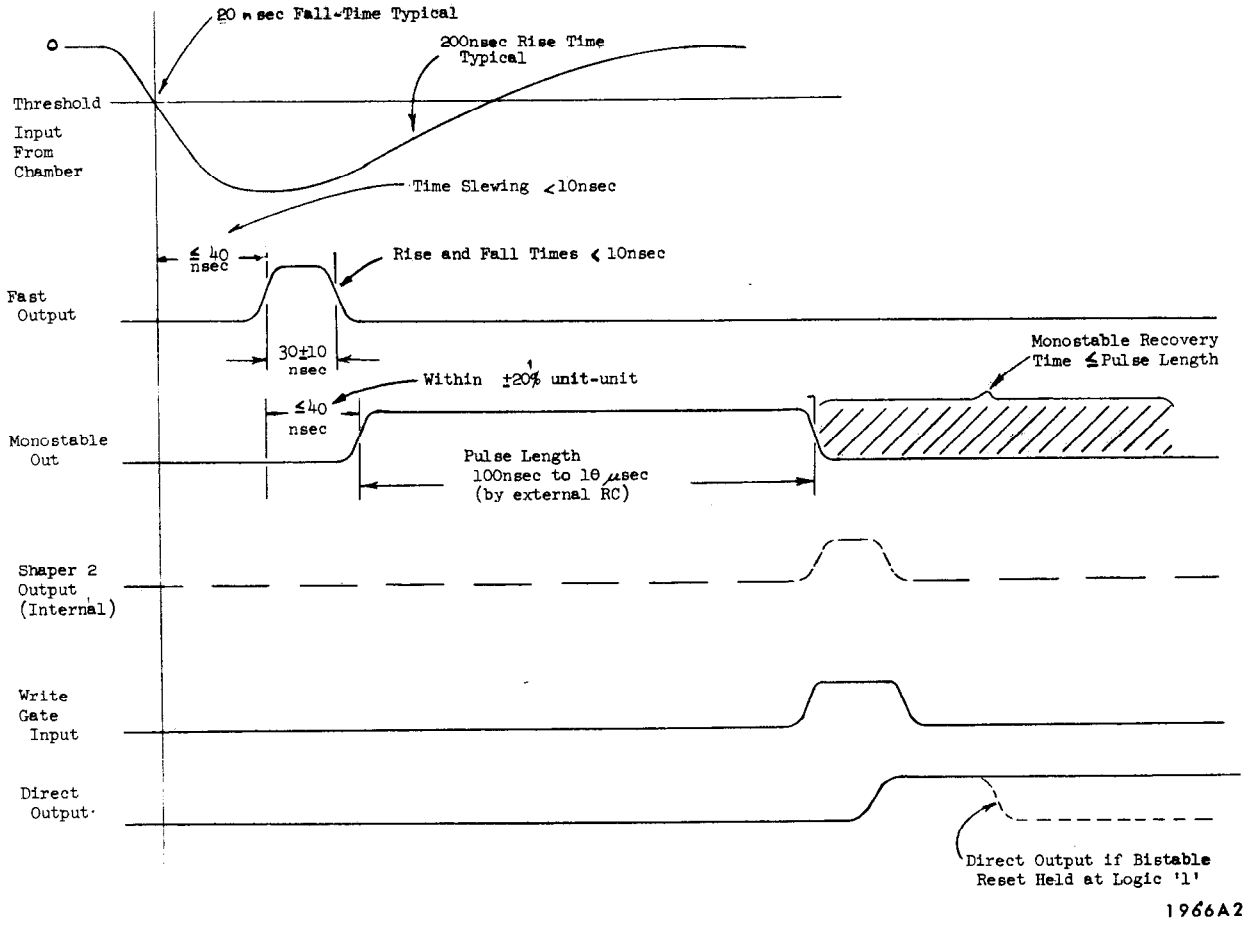
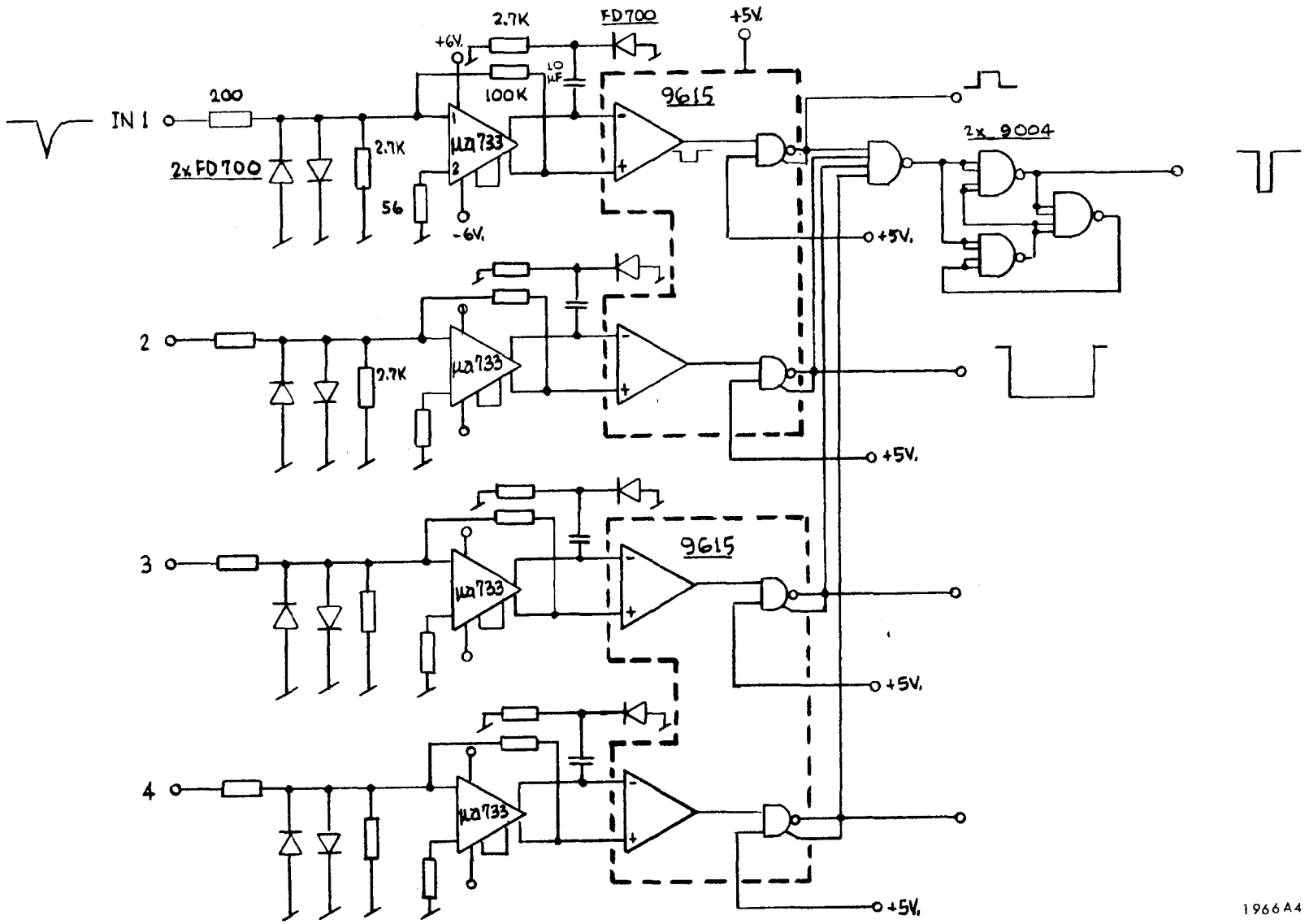

20 n sec Fall-Time Typical
200nsec Rise Time Typical
0
Threshold
Input From Chamber
Time Slewing <10nsec
≤ 40 nsec
Rise and Fall Times < 10nsec
Fast Output
30±10 nsec
Monostable Recovery Time ≤Pulse Length
Within ±20% unit-unit
≤40 nsec
Monostable Out
Pulse Length 100nsec to 10 μsec (by external RC)
Shaper 2 Output (Internal)
Write Gate Input
Direct Output
Direct Output if Bistable Reset Held at Logic '1'
1966A2

Fig. 2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FD700
+5V.
+6V.
LO
μF
100K
9615
200
IN 1
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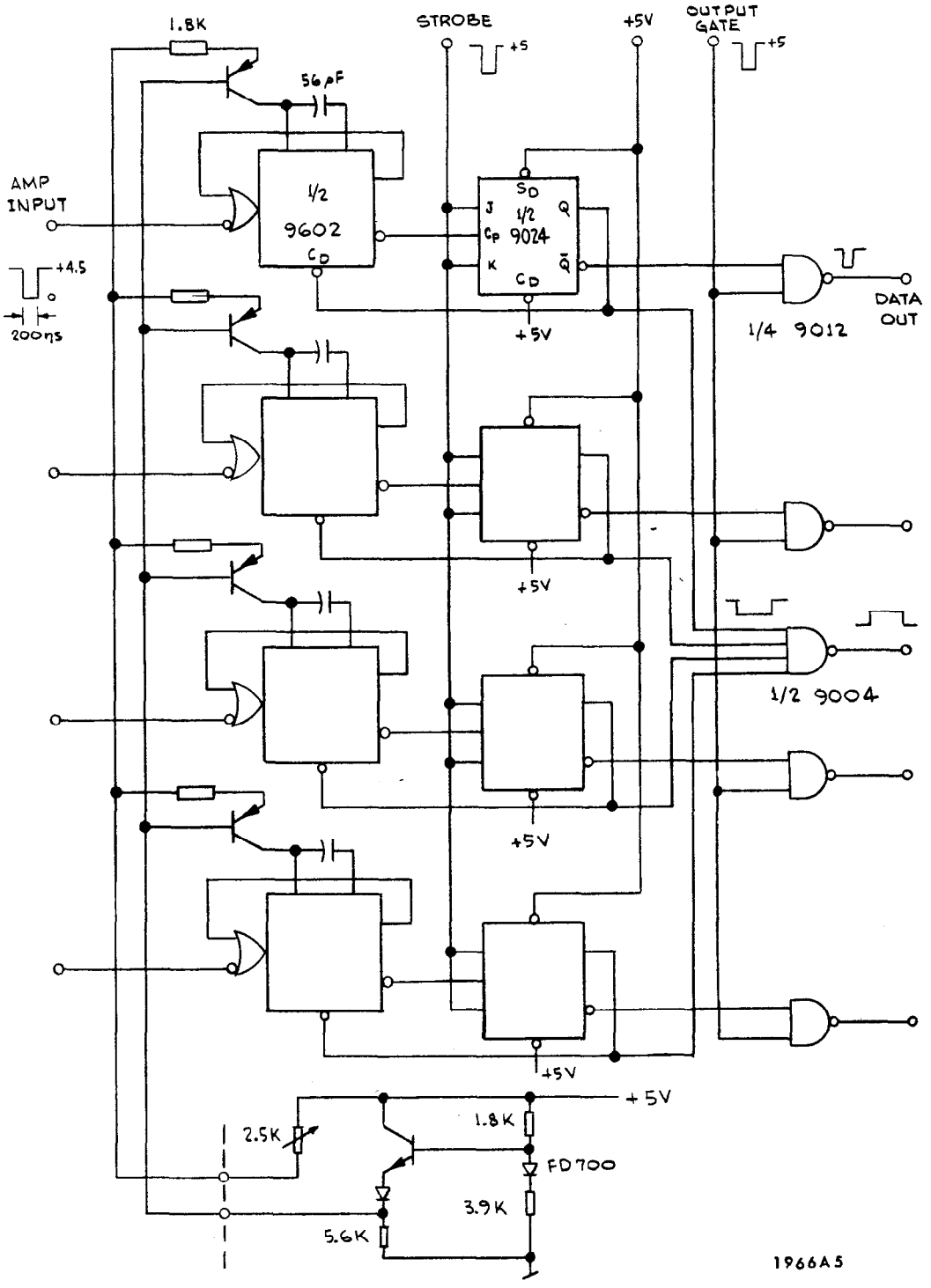
-6V.
+5V.
2x 9004
2
3
4
1966A4

Fig. 3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+4.5
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1/2 9602
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S_D
J
1/2 9024
C_P
K
Q
$\bar{Q}$
C_D
+5V
1/4 9012
DATA OUT
1/2 9004
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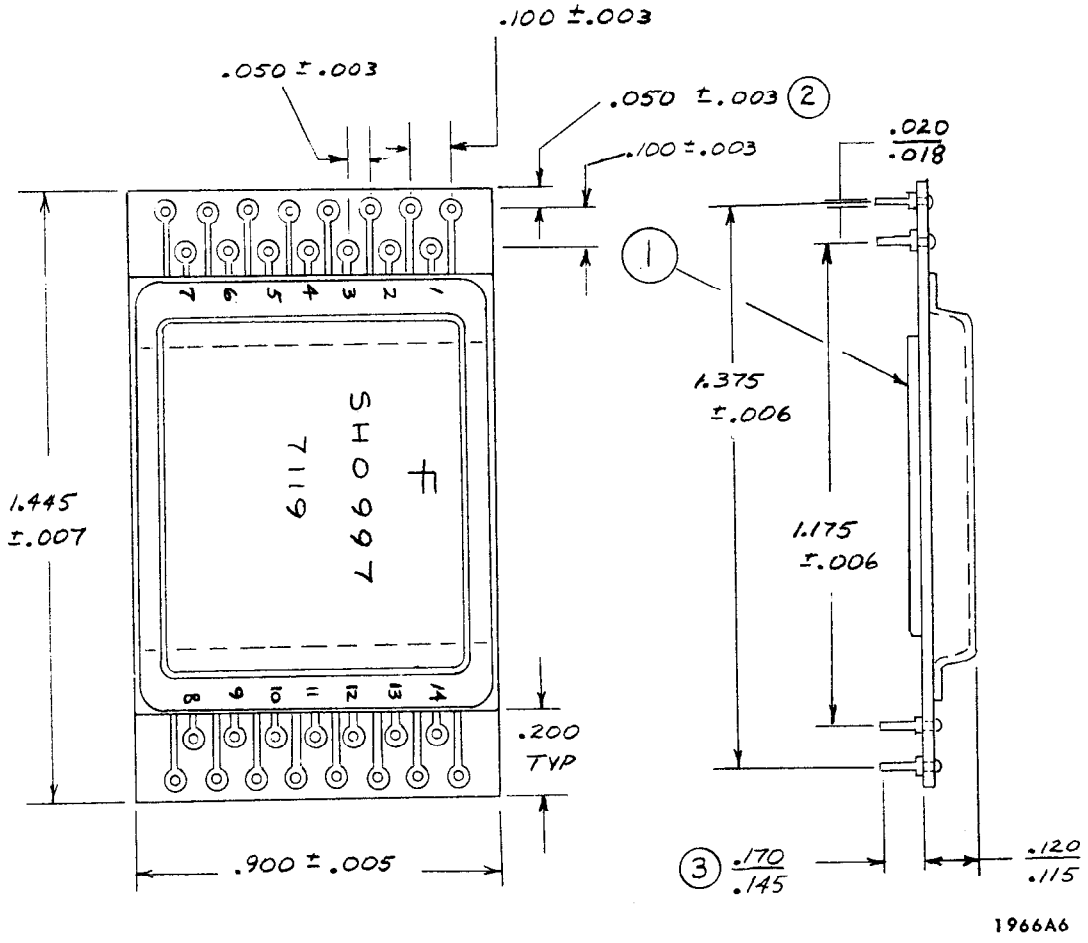
1.8K
FD700
3.9K
5.6K
1966A5

Fig. 4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TYP
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3
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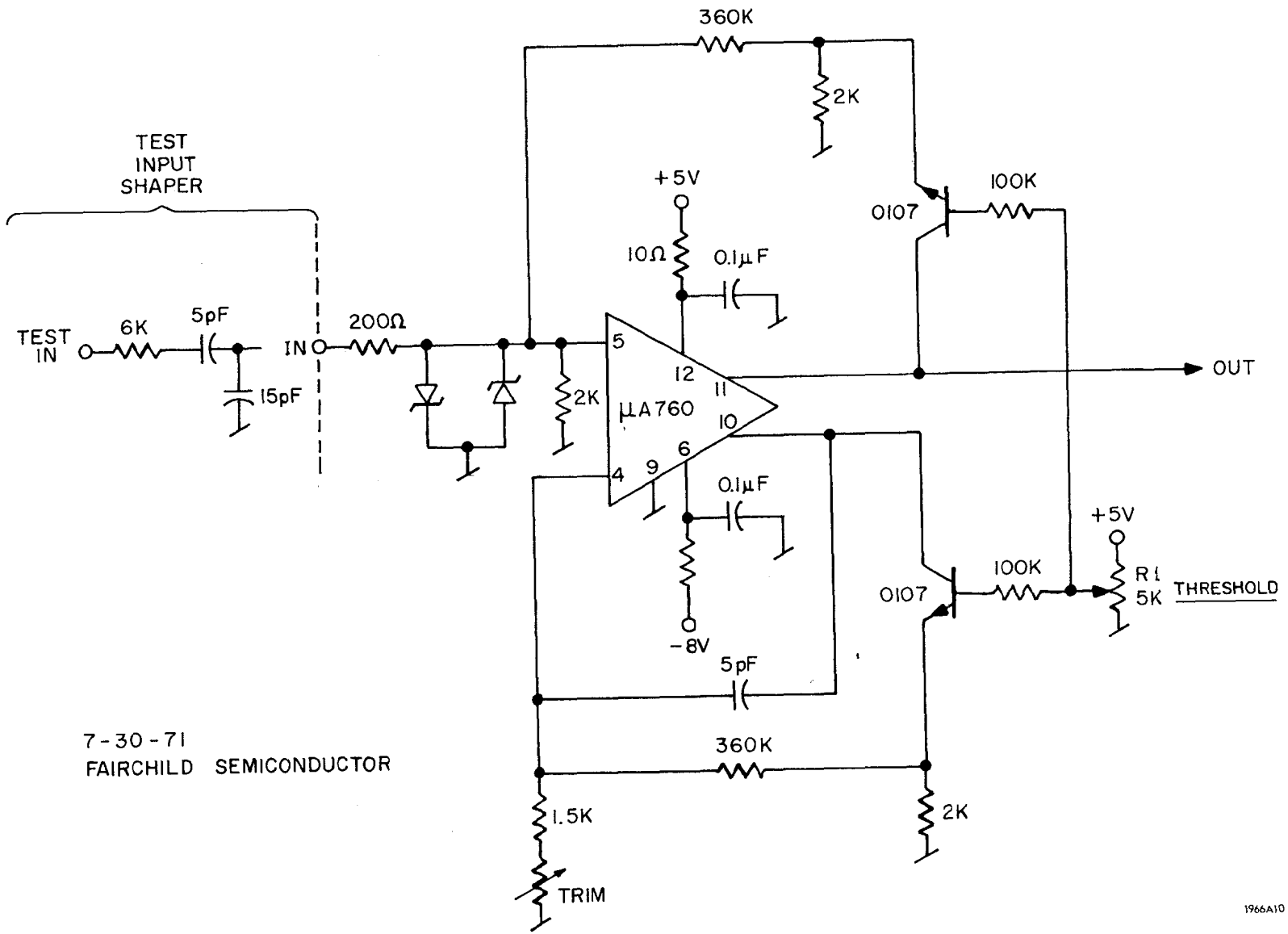
.115
1966A6

Fig. 5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2K
TEST
INPUT
SHAPER
+5V
100K
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10Ω
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TEST
IN
6K
5pF
IN
200Ω
5
12
11
OUT
15pF
2K
μA760
10
6
4
9
0.1μF
+5V
100K
Q107
R1
5K
THRESHOLD
-8V
5pF
7-30-71
FAIRCHILD SEMICONDUCTOR
360K
1.5K
2K
TRIM
1966A10

Fig. 6

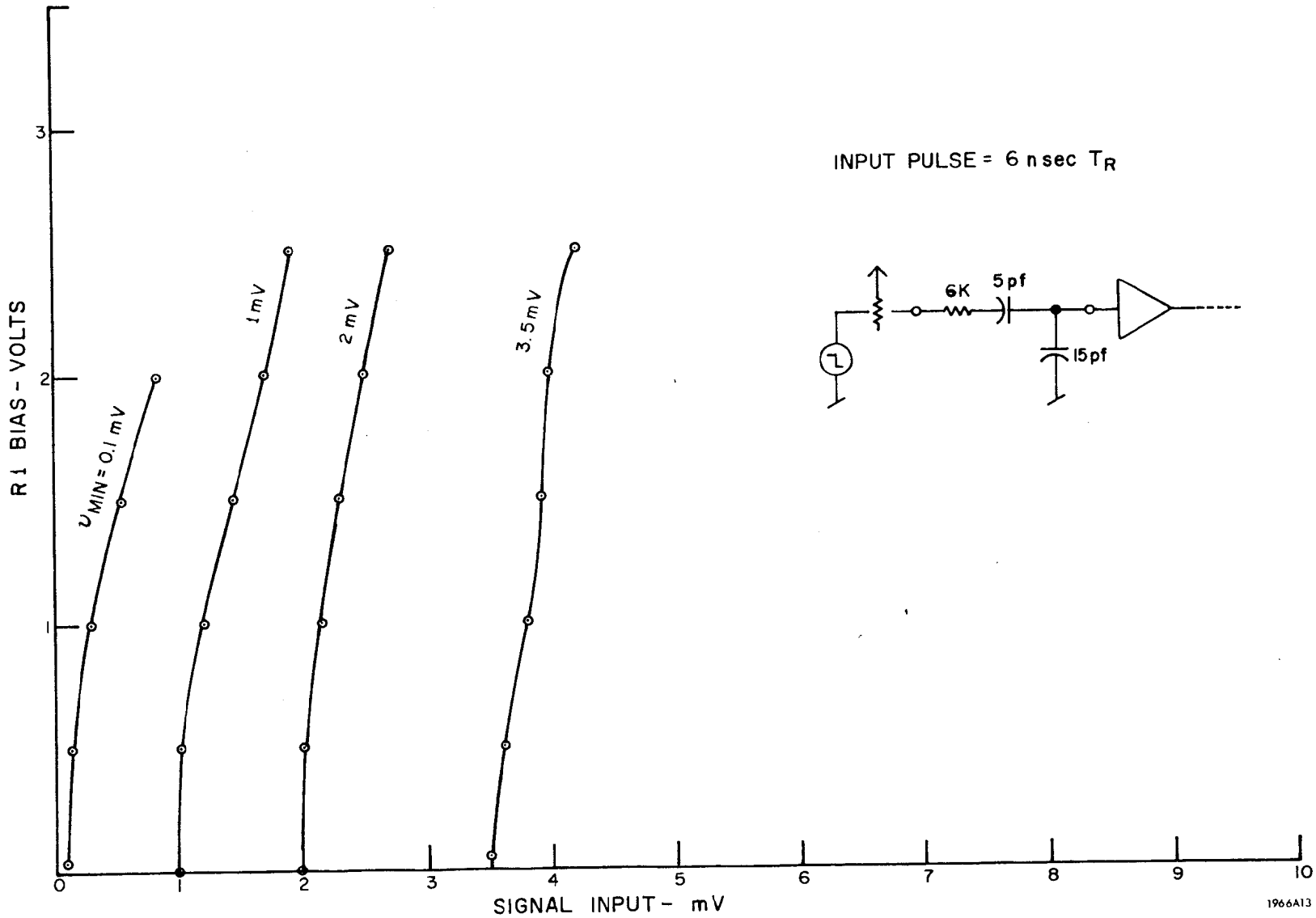

INPUT PULSE = 6 n sec T_R
6K
5pf
15pf
R1 BIAS - VOLTS
v_{MIN} = 0.1 mV
1 mV
2 mV
3.5 mV
SIGNAL INPUT - mV
0
1
2
3
4
5
6
7
8
9
10
1966A13

Fig. 7

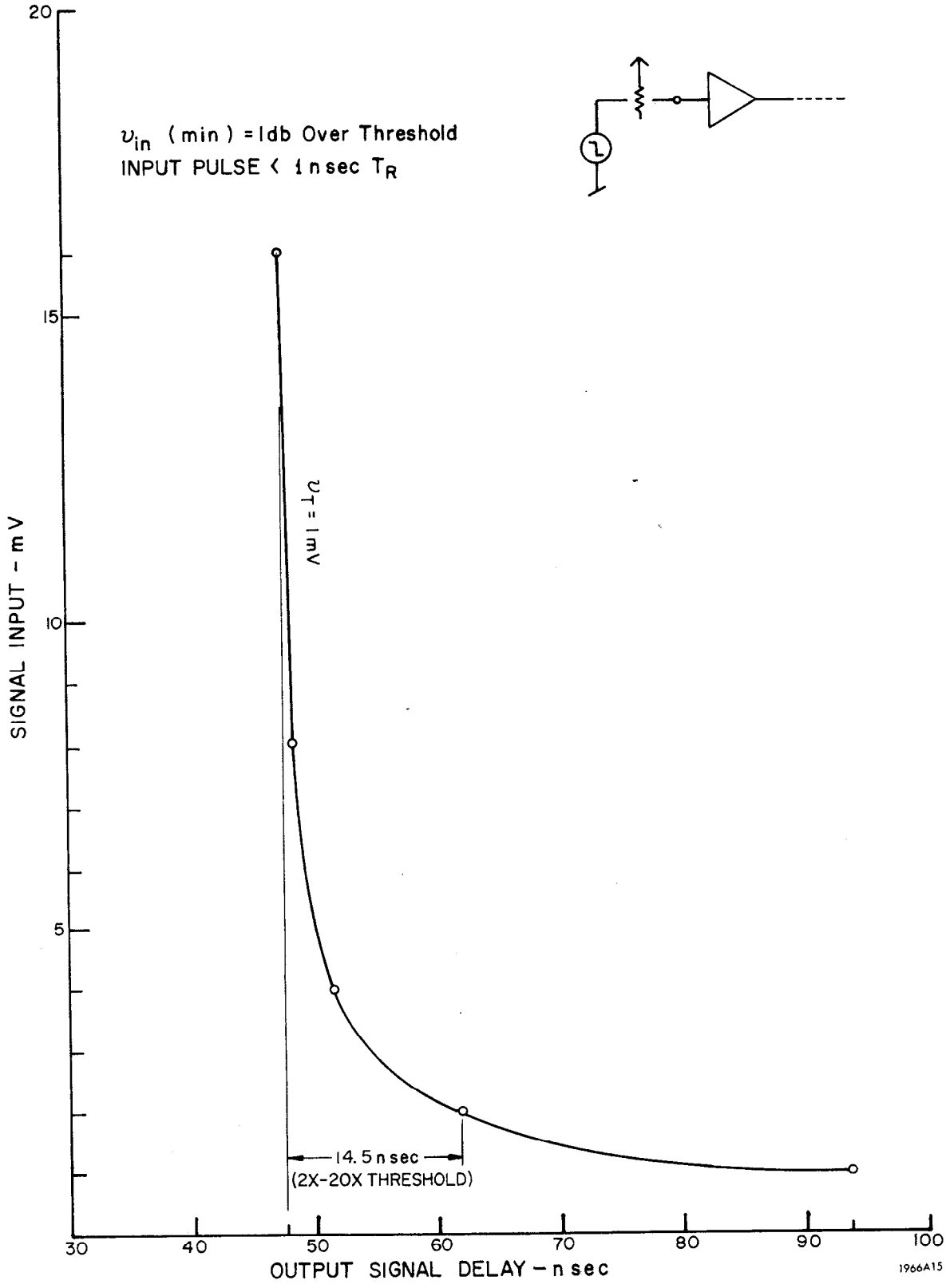

v_{in} (min) = 1db Over Threshold
INPUT PULSE < 1 n sec T_R
20
15
10
5
SIGNAL INPUT - m V
v_T = 1 mV
14.5 n sec
(2X-20X THRESHOLD)
30
40
50
60
70
80
90
100
OUTPUT SIGNAL DELAY - n sec
1966A15

Fig. 8

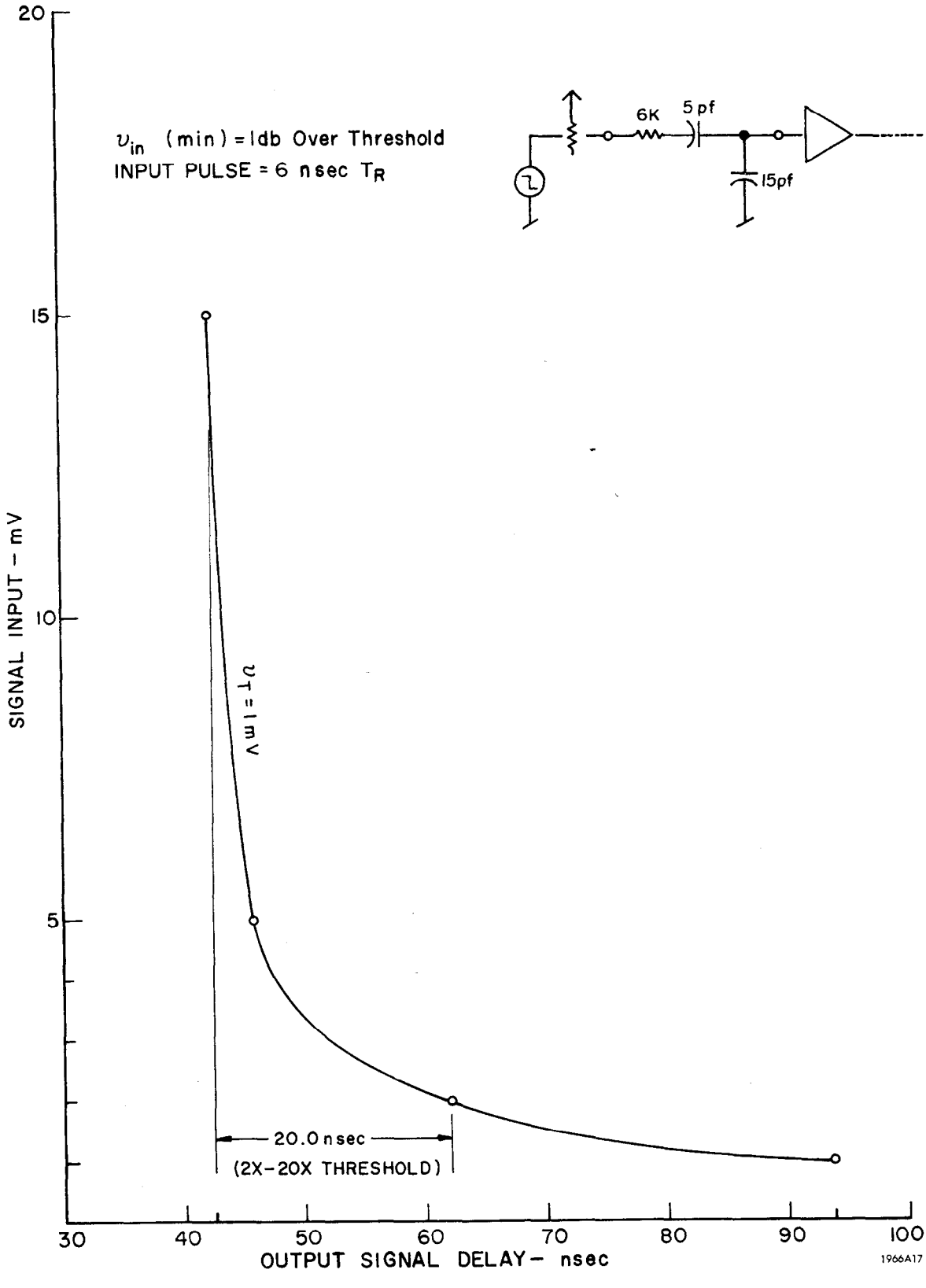

20
15
10
5
SIGNAL INPUT - mV
v_{in} (min) = 1db Over Threshold
INPUT PULSE = 6 nsec T_R
6K
5pf
15pf
v_T = 1mV
20.0 nsec
(2X-20X THRESHOLD)
30
40
50
60
70
80
90
100
OUTPUT SIGNAL DELAY- nsec
1966A17

Fig. 9

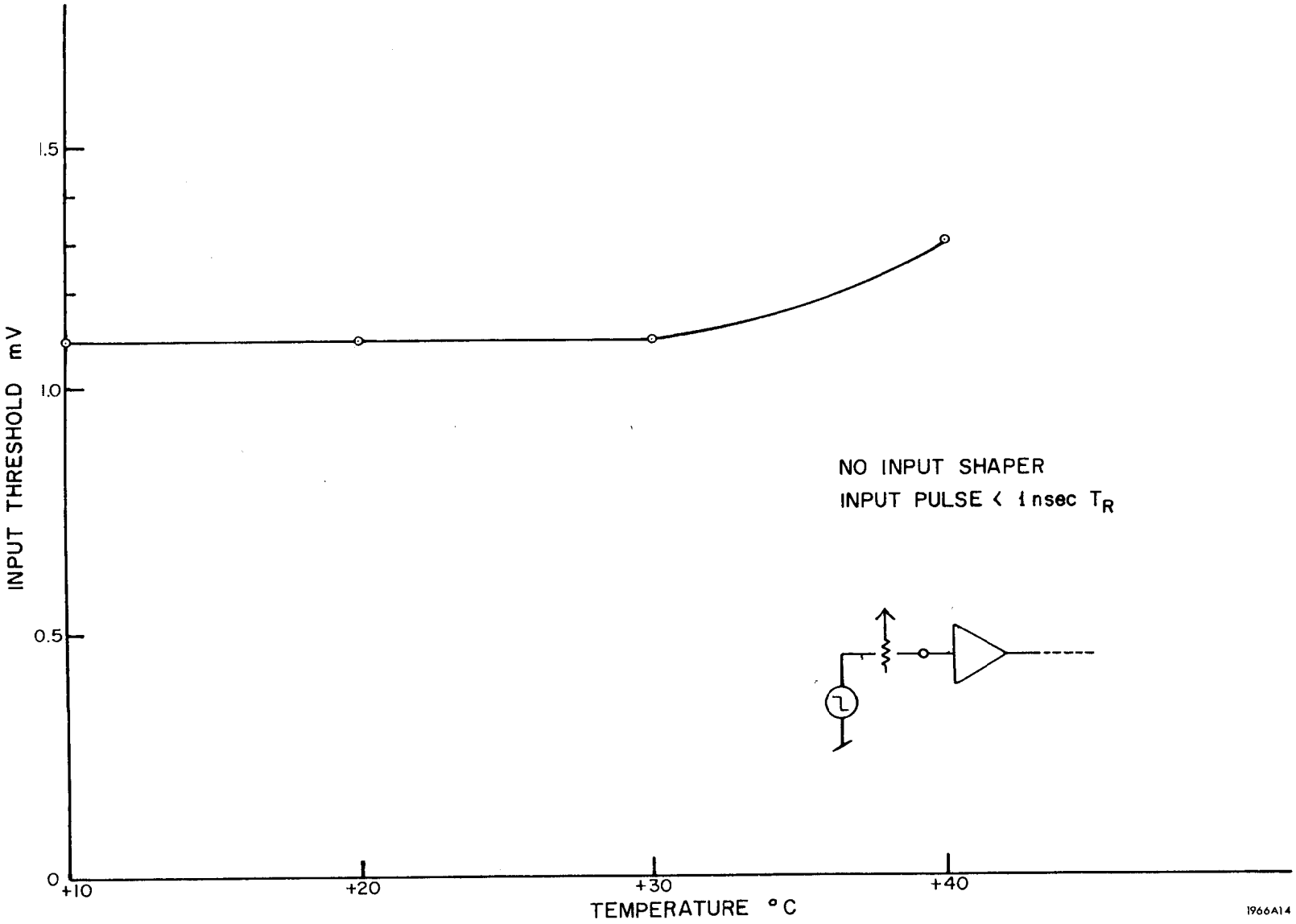

INPUT THRESHOLD mV
1.5
1.0
0.5
0
+10
+20
+30
+40
TEMPERATURE °C
NO INPUT SHAPER
INPUT PULSE < 1 nsec T_R
1966A14

Fig. 10

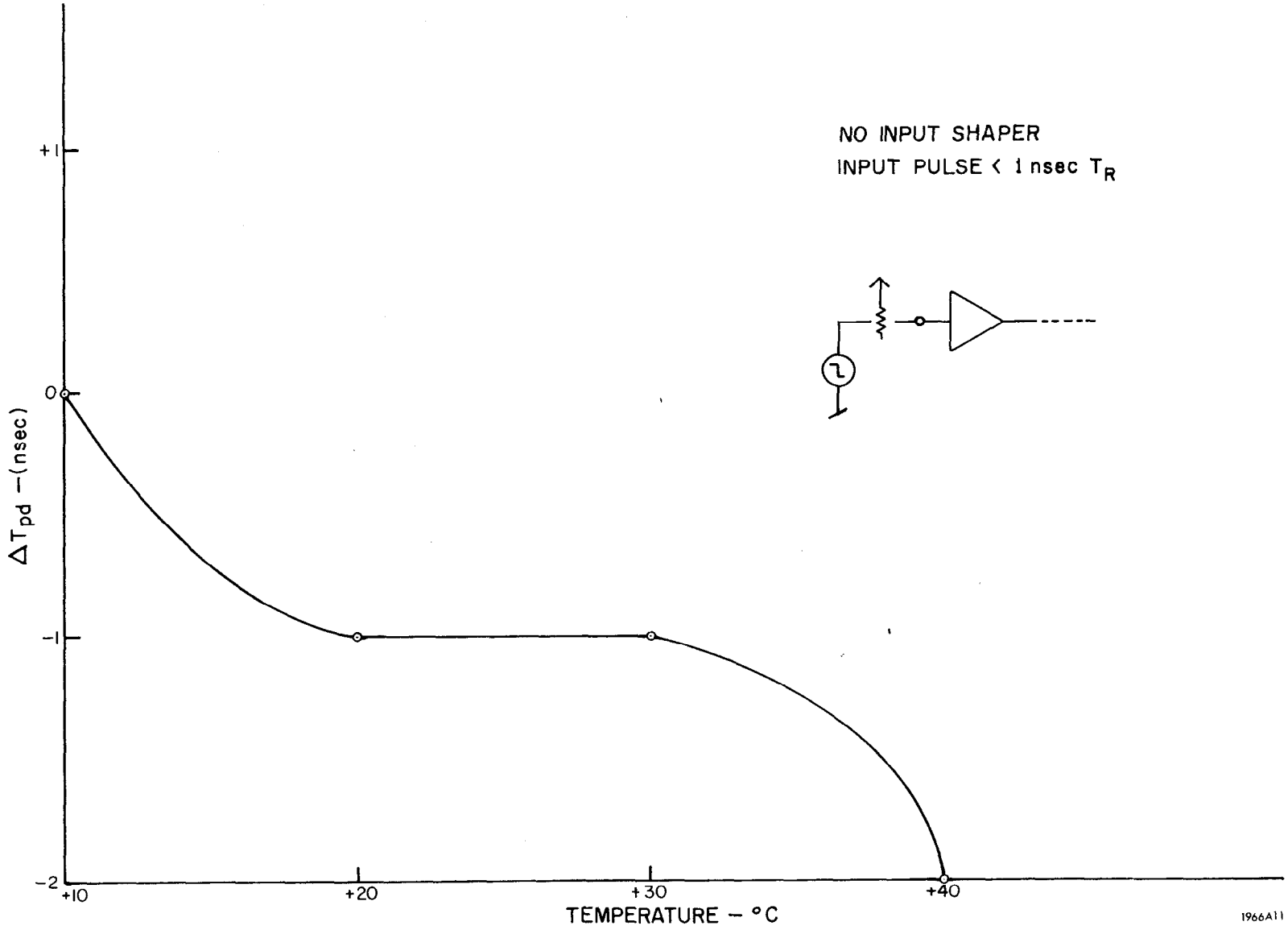

NO INPUT SHAPER
INPUT PULSE < 1 nsec T_R
+1
0
-1
-2
ΔT_{pd} — (nsec)
+10
+20
+30
+40
TEMPERATURE — °C
1966A11

Fig. 11

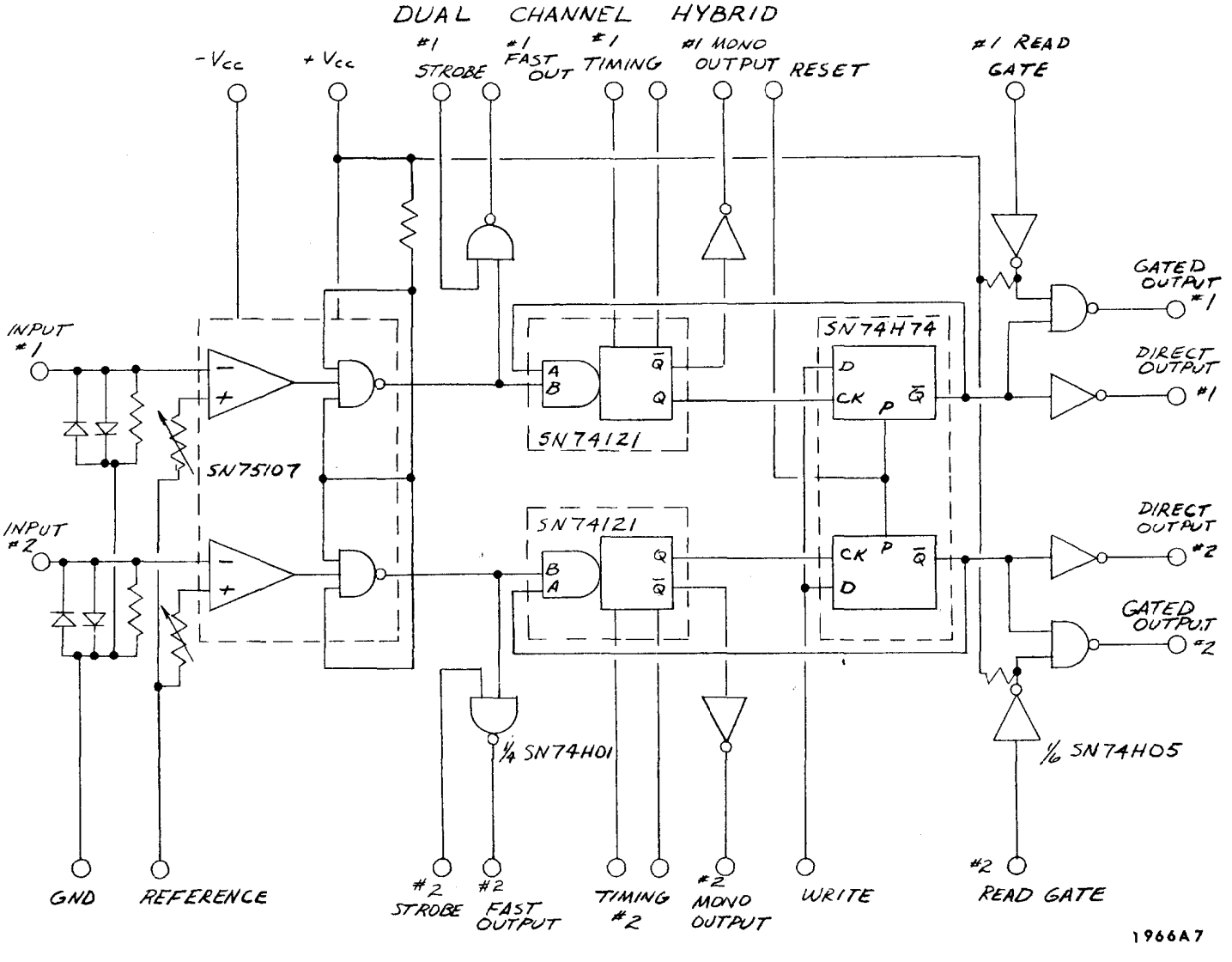
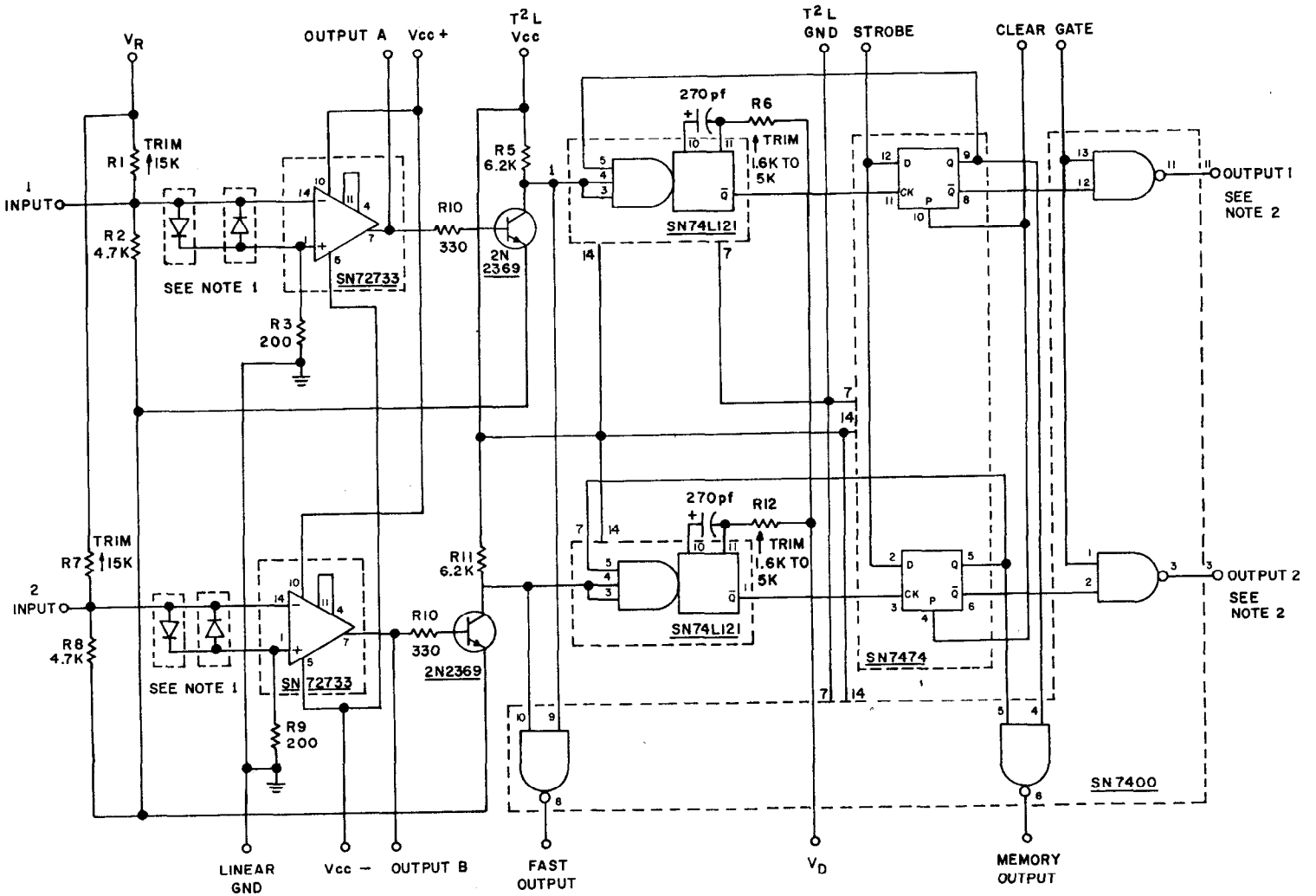

DUAL CHANNEL HYBRID
-Vcc
+Vcc
#1 STROBE
#1 FAST OUT
#1 TIMING
#1 MONO OUTPUT
RESET
#1 READ GATE
INPUT #1
INPUT #2
SN75107
SN74121
SN74121
SN74H74
GATED OUTPUT #1
DIRECT OUTPUT #1
DIRECT OUTPUT #2
GATED OUTPUT #2
1/4 SN74H01
1/6 SN74H05
GND
REFERENCE
#2 STROBE
#2 FAST OUTPUT
TIMING #2
#2 MONO OUTPUT
WRITE
#2 READ GATE
1966A7

Fig. 12



NOTES:

1. INPUT PROTECTION DIODES ARE BASE EMITTER JUNCTIONS OF 2N2369 WITH COLLECTORS OPEN.
2. OUTPUT 1 AND OUTPUT 2 ARE FLOATING COLLECTORS OUTPUTS.

TEXAS INSTRUMENTS

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1966A18

Fig. 13

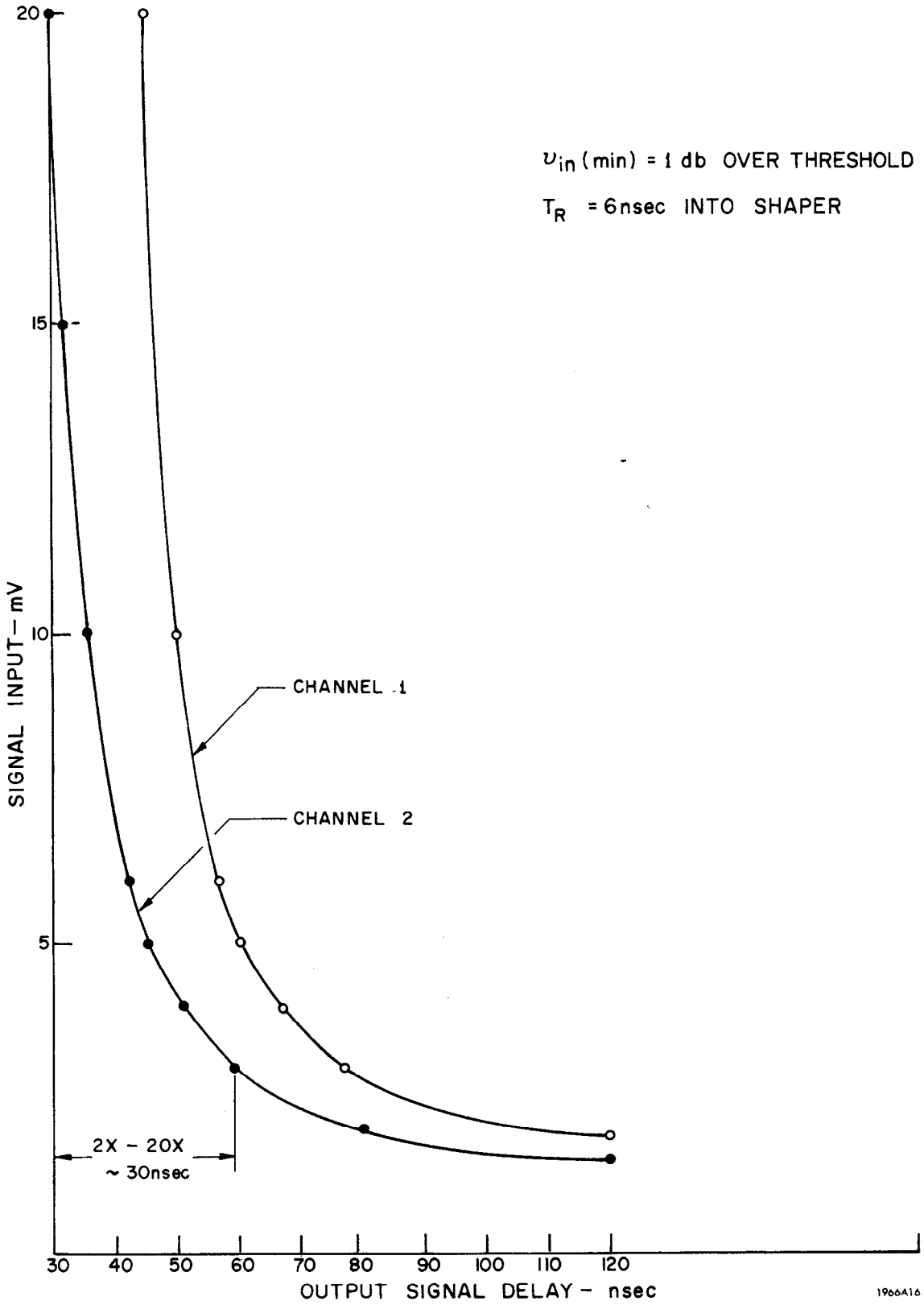
v_{in} (min) = 1 db OVER THRESHOLD
T_R = 6nsec INTO SHAPER
SIGNAL INPUT – mV
20
15
10
5
CHANNEL 1
CHANNEL 2
2X – 20X
~ 30nsec
30
40
50
60
70
80
90
100
110
120
OUTPUT SIGNAL DELAY – nsec
1966A16

Fig. 14

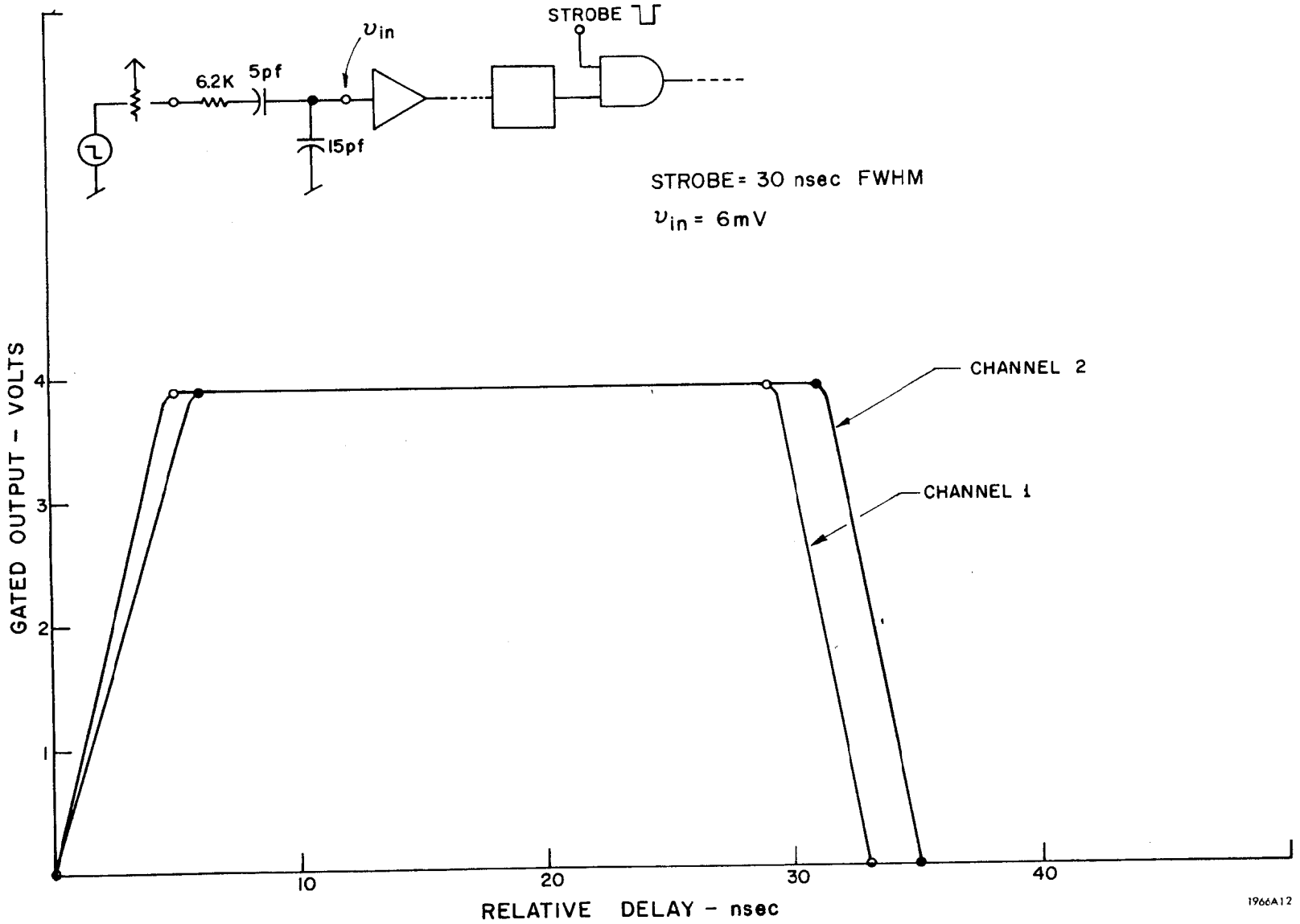
STROBE
v_{in}
6.2K
5pf
15pf
STROBE = 30 nsec FWHM
v_{in} = 6mV
CHANNEL 2
CHANNEL 1
GATED OUTPUT - VOLTS
1
2
3
4
10
20
30
40
RELATIVE DELAY - nsec
1966A12

Fig. 15