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"PEPPO" — A DUAL DIGITAL DELAY AND GATE GENERATOR*

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Summary

A new high performance two-channel gate generator in a triple NIM module using integrated circuits is described. Its main characteristics are the digital design and the generation of both delay and width of a signal, relative to a trigger pulse, in each channel.

Introduction

This paper describes a new dual gate generator whose functions are similar to those of a conventional analog gate generator but the use of a digital design eliminates the dead time and combines adjustable delay and width in each channel.

The output width and delay varies from 100 ns to 9.99 s, in six different ranges, with a resolution of 1 part per 1000. Outputs include logic L and $\overline{L}$ (-700 mV on 50 Ω) and gate G and $\overline{G}$ (+12 volts on high impedance or +10 V on 50 Ω).

The input sensitivity for the NIM start pulse is less than 3 ns. An LED light indicates "on" time for each channel. Thumbwheel switches are used for presetting delay and width. A six position switch selects the operating frequency of the clock (TIME BASE).

The module described occupies a triple† NIM width and includes two channels which are independent except for the common time base. MECL integrated circuits and discrete transistors are used for IN/OUT signal interfacing; TTL integrated circuits are used for the internal logic. This results in simplicity and increased reliability over the conventional analog circuits.

Principle of Operation

Suppose a gated clock oscillates at some selected frequency ν. The nth pulse, after the clock gate has been opened by a start pulse at $t_0=0$, occurs at the time $t=nT$ ($T=1/\nu$). If the start pulse ($t_0=0$) sets a flip-flop and the nth clock pulse resets it, we will have an output pulse whose width is $W=nT$, and which starts at $t_0=0$.

If we, instead, set the flip-flop with the mth pulse and reset it with the nth (where m and n are arbitrary numbers with $n > m$) we have a very versatile gate generator having an output starting at $t_1=mT$ and ending at $t_2=nT$ with a width $W=t_2-t_1=(n-m)\,T$ and a delay from the start pulse $D=t_1-t_0=mT$.

The thumbwheel switches in the circuit described here select the delay (m) and the width (n-m); the six position selects the time base T.

A start pulse (block diagram, Fig. 1) at $t_0=0$ enables a clock to oscillate at 10 MHz. The time base T is generated by using the clock directly or divided in steps of factors of ten to 100 Hz in five ranges. Note that a single time base generator is shared by the two channels. For each channel, these clock pulses are counted in sequence in two presettable scalers, one of which determines the gate delay m and the other the gate width (n-m).

A D-type clocked flip-flop, operating in conjunction with the two scalers, produces the signal which is converted to logic (L, $\overline{L}$) at NIM standard levels and to gate (G, $\overline{G}$) pulses, at 0 and +12 volt levels.

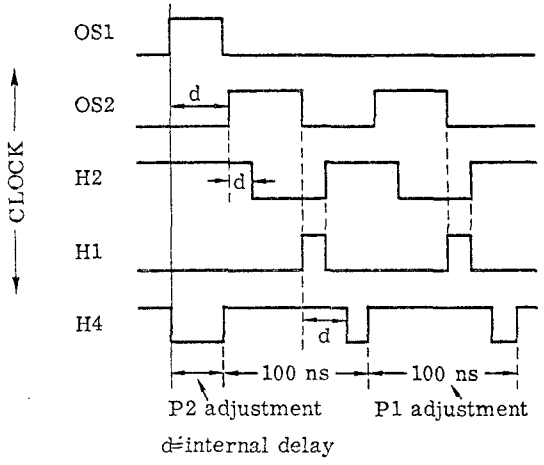
An automatic Reset/Strobe is internally performed at the end of the cycle, which resets the frequency divider scaler and presets the delay and width scalers so the unit is prepared for the next start pulse.

Circuit Description

The MECL integrated circuits A1, A2 and B1 (Fig. 2) convert the NIM start pulse to a TTL pulse whose negative-going edge triggers the "one shot" OS1, generating a pulse that sets the flip-flop C1-C2 which enables the clock (OS2, H1, H2, H3) to oscillate at 10 MHz.

A five decade scaler J1-J5 divides the clock frequency from 10 MHz to 100 Hz in factors of ten. The switch S1 (TIME BASE) in conjunction with the multiplexer (MPX) selects the appropriate clock frequency ($\nu=1/T$) for the gate generator logic. In order to shorten the IN/OUT delay the start pulse is ORed with the selected clock pulses and becomes the first clock pulse to be counted.

The variable resistor P1 adjusts the clock frequency to 10 MHz and P2 adjusts the time interval between the start pulse and the first of the clock pulses to achieve uniform clock spacing, as illustrated in the diagram below.



The selected clock pulses are counted in a double three decade scaler (Fig. 3) whose outputs allow a D-type flip-flop to be set and reset by the appropriate clock pulses. This situation is illustrated in Fig. 4 which describes the operation of channel 1 where the delay is preset to 3 units ($D_1=3T$) and the width to 5 units ($W_1=5T$).

The gate K1 is open while K2 is kept closed by the high state of the T1** output. While the D input of M1 is low, no transition occurs on the output. The delay (R1) and width (R2) scalers are preset by three digital thumbwheels of a

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†Due to the size of the thumbwheel switches.

**In Fig. 3b, n=1, 2, 3, 4 where 1 and 2 refer to channel 1 delay and width respectively; 3 and 4 to channel 2; so T1 refers to the Tn gate channel 1 delay counter; T2 channel 1 width counter. In the same spirit R1 of Fig. 3a refers to the combination of the 3 counters R11, R12, R13 of Fig. 3b, and so on.

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nine's complement type; e.g., in the example described here, the delay scaler is preset at 996 and the width at 994.

The first three clock pulses, through the open gate K1, brings the count on the scaler R1 to 999 so that the AND gate T1 changes its state to a low level enabling the D-type flip-flop to change to the set state with the next clock pulse (positive going edge). The gate K1 is then closed and K2 is opened to the width counter R2. The next five clock pulses through K2 bring the scaler R2 to 999. The gate T2 then changes the level at the D input of the flip-flop enabling this to change to the reset state with the next clock pulse. At the same time it closes the gate K2, keeps K1 closed and opens K3 allowing a reset pulse to pass through. The output pulse ℓ-1 (and the complement g-1) is then 5 units wide starting 3 units after the start pulse (Fig. 4: M1-Q). The reset pulse from the gate K3 passes through the OR gates L3 and E1 (Fig. 2) and resets the flip-flop C1-C2. This disables the clock and also keeps: (a) the multiplexer (MPX) inhibited, (b) the frequency divider (J counters) reset, and (c) the Rn scalers (Fig. 3) strobed and preset until the next cycle starts.

When both channels are operating the only change from the sequence described above (Fig. 4) is that the reset pulse occurs at the end of the longest operating cycle.

The positive (ℓ) output from the D-type flip-flop is converted (Fig. 5) from TTL to MECL (N1, U1) and, by the MC1025 emitter-coupled pair (V1, V2), to NIM standard levels L and $\bar{L}$ (-700 mV on 50 Ω, with rise and fall time $\simeq$ 2 ns). The negative (g) output is amplified (2N 2219) and converted to gate outputs G and $\bar{G}$ (+12 V on high impedance or +10 V on 50 Ω, with rise and fall time $\simeq$ 8 ns) by a complementary pair emitter follower.

An LED for each channel is lit for the duration of each pulse or for 300 μs (OS3), whichever is longer.

Conclusion

The module is triggered by a negative going edge (-700 mV) so that modules may be cascaded using the $\bar{L}$ output. In this spirit, PEPPO can be used as an oscillator if $\bar{L}$ output of the channel with the largest sum of delay and width is fed back into the input with an appropriate delay.

A stop input can be used to terminate the cycle at any time.

The circuit is completely dc coupled.

Bridging BNC's are available at the start input so the same start pulse can be used for other modules; if not used the second BNC must be terminated with 50 Ω.

Acknowledgements

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Figure Captions

FIG. 1--"Peppo"-block diagram.

FIG. 2--Time base generator.

FIG. 3--Gate generator logic (a) logic circuit, (b) detail of the scalers.

FIG. 4--Timing diagram.

FIG. 5--Output level converters.

FIG. 6--Power converter.

FIG. 7--"Peppo"

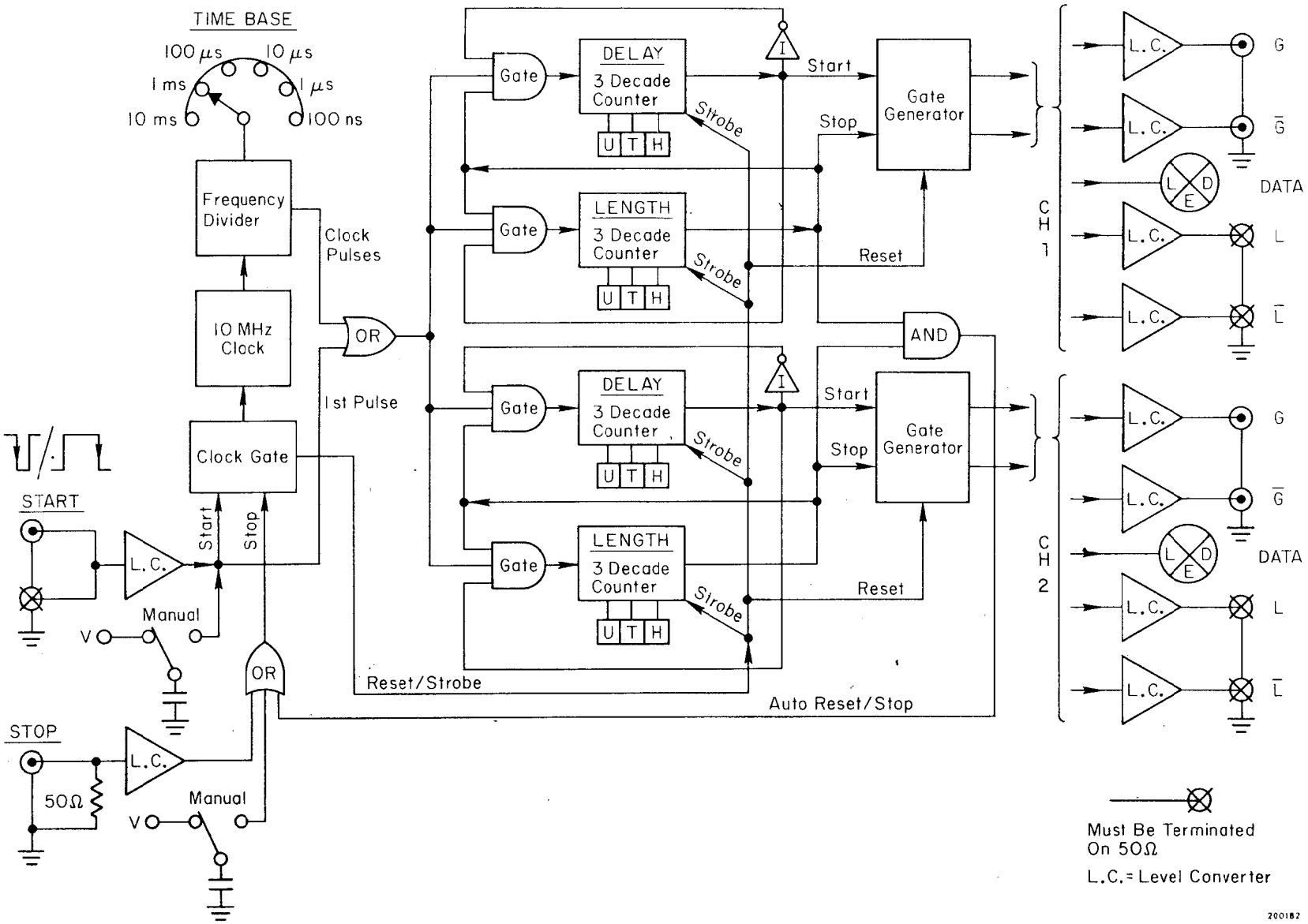

TIME BASE
100 μs
10 μs
1 ms
1 μs
10 ms
100 ns
Frequency Divider
10 MHz Clock
Clock Gate
Clock Pulses
1st Pulse
OR
START
STOP
L.C.
Manual
50Ω
Start
Stop
Reset/Strobe
Auto Reset/Stop
Gate
DELAY
3 Decade Counter
LENGTH
3 Decade Counter
U T H
Strobe
Start
Stop
Reset
AND
Gate Generator
CH 1
CH 2
G
Ḡ
DATA
L
L̄
Must Be Terminated On 50Ω
L.C. = Level Converter
200182

Fig. 1

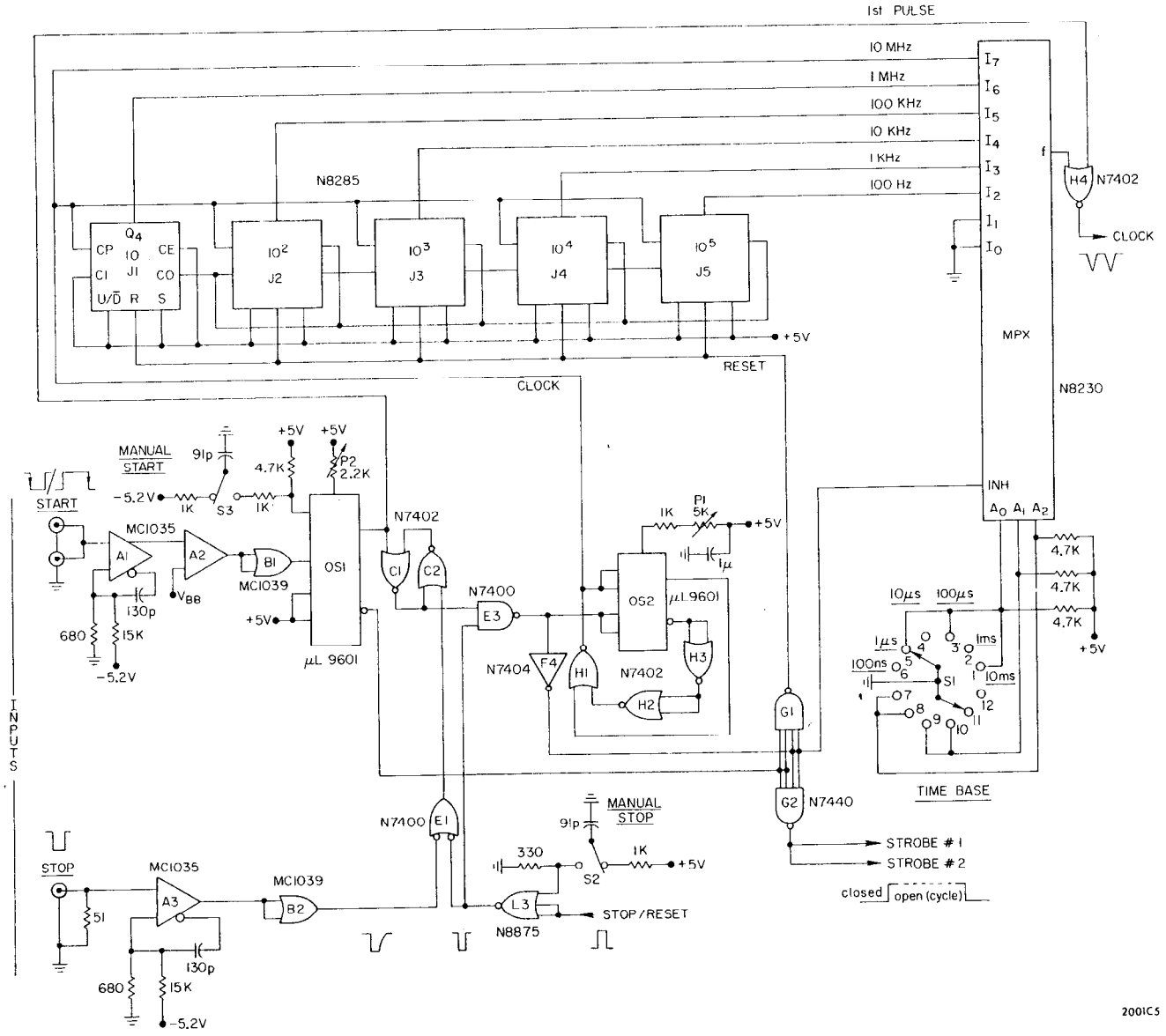

1st PULSE
10 MHz
1 MHz
100 KHz
10 KHz
1 KHz
100 Hz
N8285
MPX
N8230
CLOCK
RESET
+5V
INH
TIME BASE
STROBE #1
STROBE #2
closed
open (cycle)
MANUAL START
START
MC1035
MC1039
μL 9601
N7402
N7400
N7404
N7440
MANUAL STOP
STOP
STOP/RESET
N8875
INPUTS
2001C5

Fig. 2

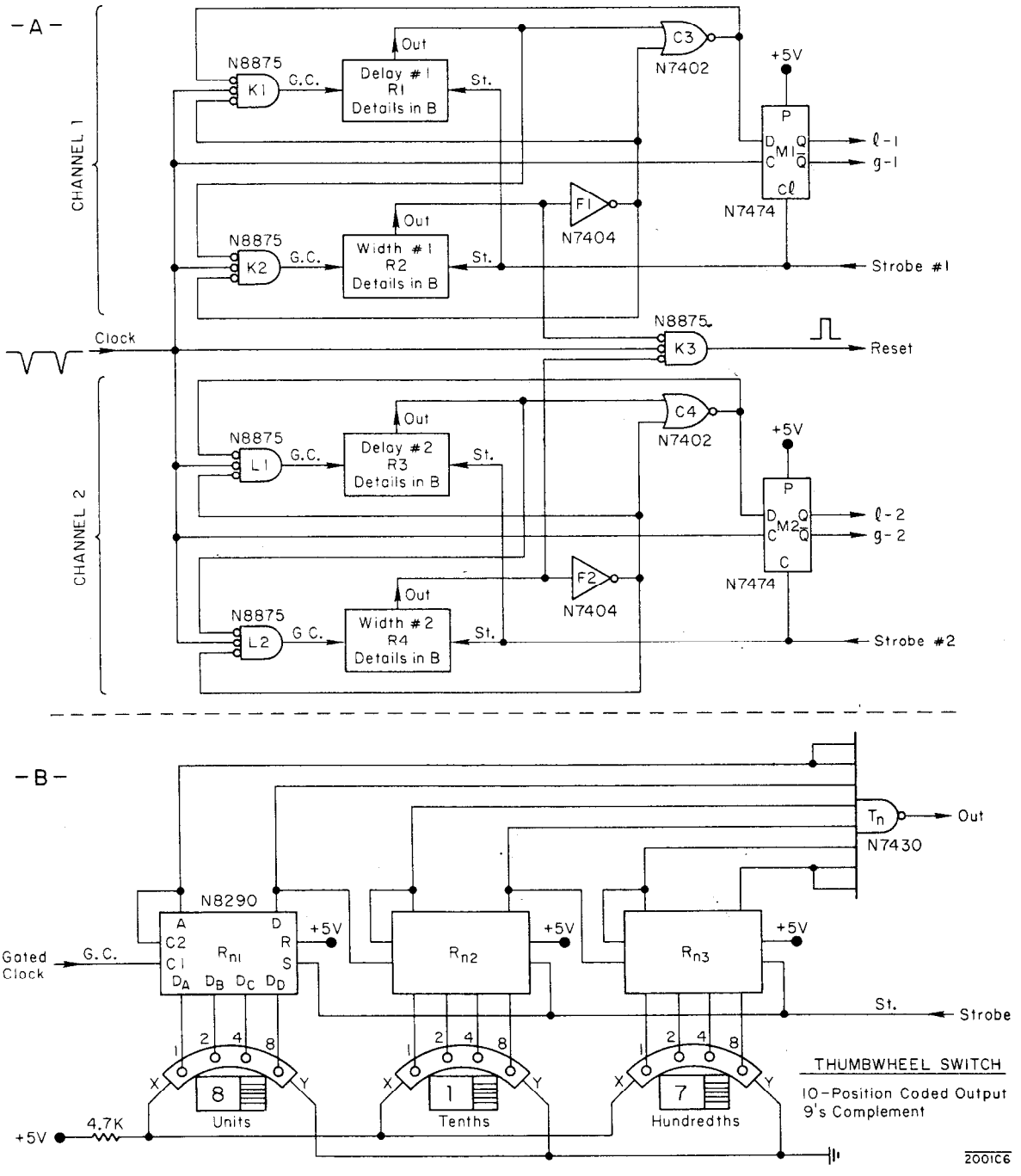

-A-
CHANNEL 1
CHANNEL 2
N8875
K1
G.C.
Delay #1
R1
Details in B
Out
St.
C3
N7402
+5V
P
D
C
M1
Q
Q̄
Cl
ℓ-1
g-1
N7474
F1
N7404
N8875
K2
Width #1
R2
Details in B
Strobe #1
Clock
N8875
K3
Reset
N8875
L1
Delay #2
R3
Details in B
C4
N7402
M2
ℓ-2
g-2
F2
N7404
N8875
L2
Width #2
R4
Details in B
Strobe #2
-B-
Tn
N7430
Out
N8290
A
C2
C1
DA DB DC DD
D
R
S
Rn1
Rn2
Rn3
Gated
Clock
1 2 4 8
X
Y
8
Units
1
Tenths
7
Hundredths
4.7K
THUMBWHEEL SWITCH
10-Position Coded Output
9's Complement
200IC6

Fig. 3

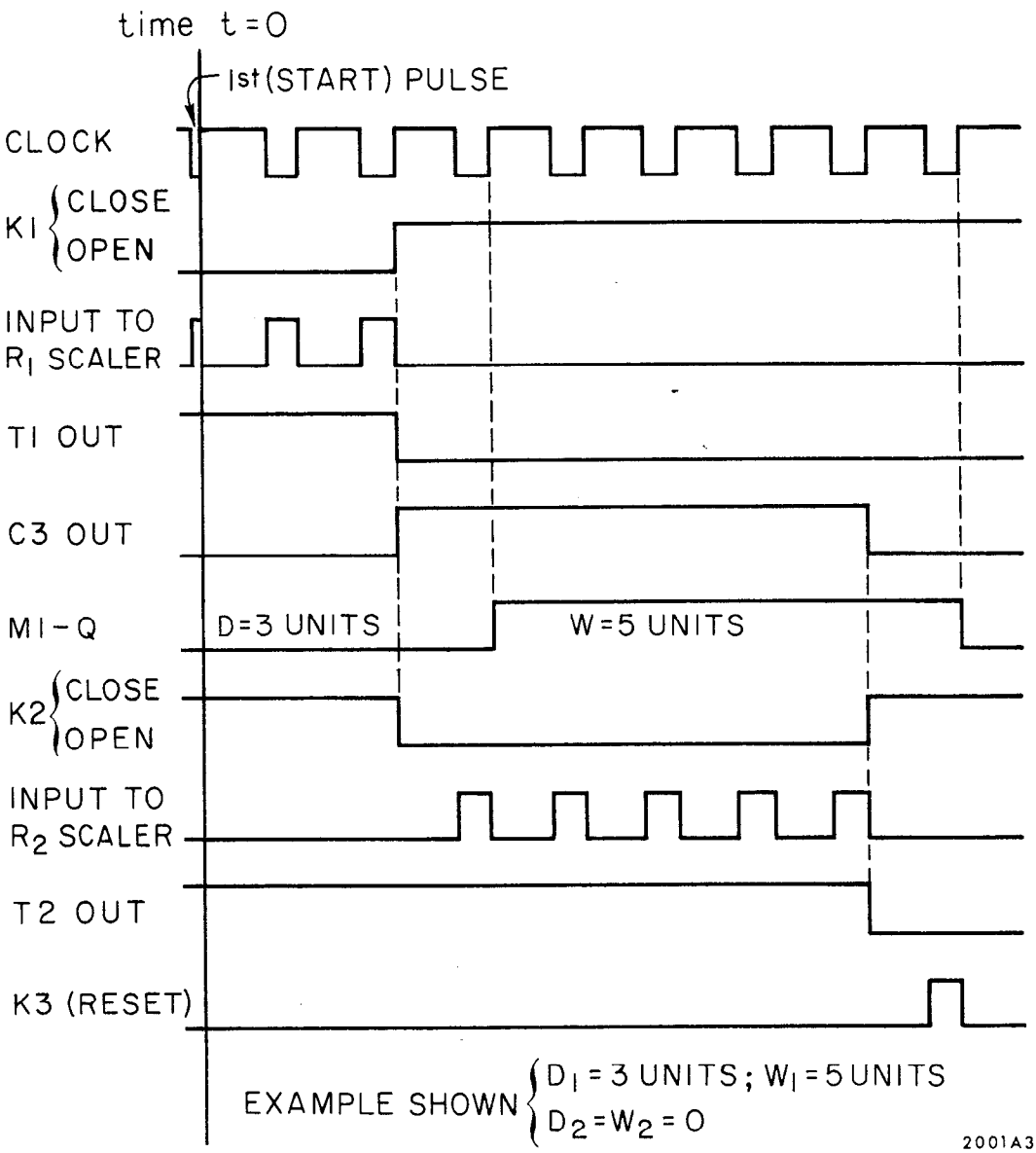

time t=0
1st (START) PULSE
CLOCK
K1 CLOSE
OPEN
INPUT TO
R1 SCALER
T1 OUT
C3 OUT
M1-Q
D=3 UNITS
W=5 UNITS
K2 CLOSE
OPEN
INPUT TO
R2 SCALER
T2 OUT
K3 (RESET)
EXAMPLE SHOWN
D1 = 3 UNITS; W1 = 5 UNITS
D2 = W2 = 0
2001A3

Fig. 4

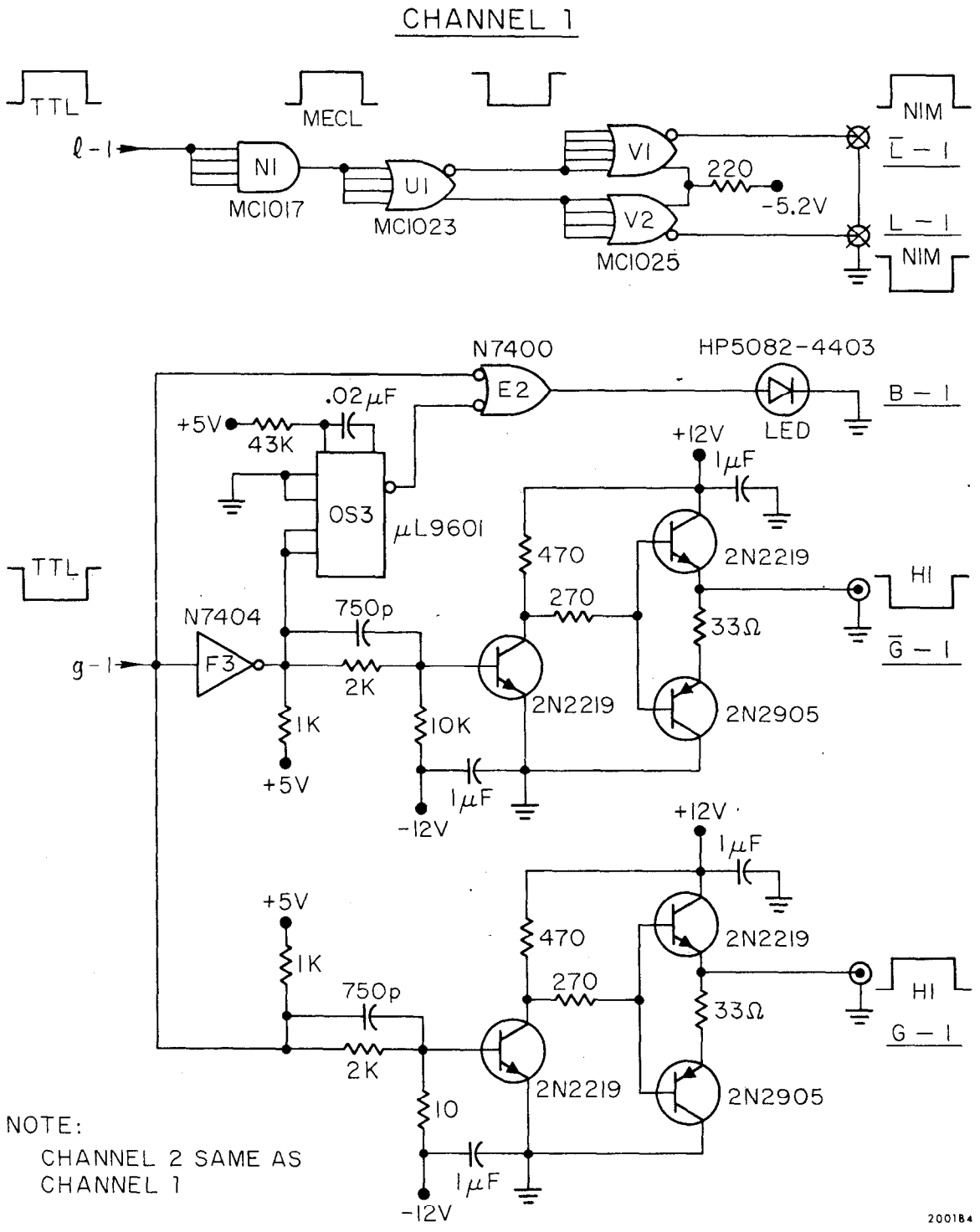

CHANNEL 1
TTL
MECL
NIM
ℓ-1
N1
MC1017
U1
MC1023
V1
V2
MC1025
220
-5.2V
L-1
NIM
N7400
E2
HP5082-4403
B-1
LED
+5V
43K
.02μF
OS3
μL9601
+12V
1μF
470
270
2N2219
HI
33Ω
G-1
TTL
N7404
F3
g-1
750p
2K
1K
10K
+5V
-12V
1μF
2N2219
2N2905
+12V
1μF
+5V
1K
470
270
750p
2K
10
2N2219
2N2905
HI
G-1
-12V
1μF
NOTE:
CHANNEL 2 SAME AS
CHANNEL 1
200184

Fig. 5

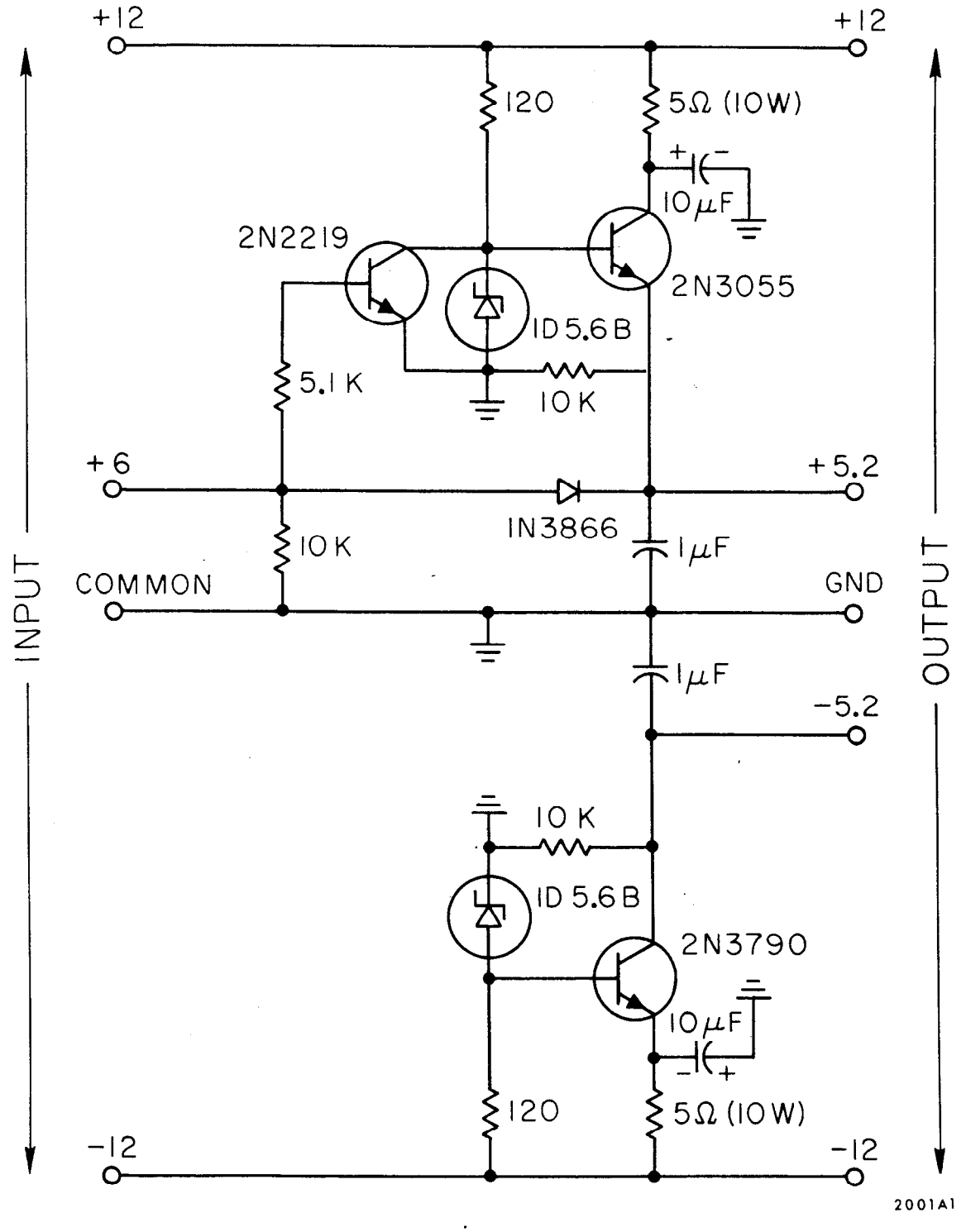
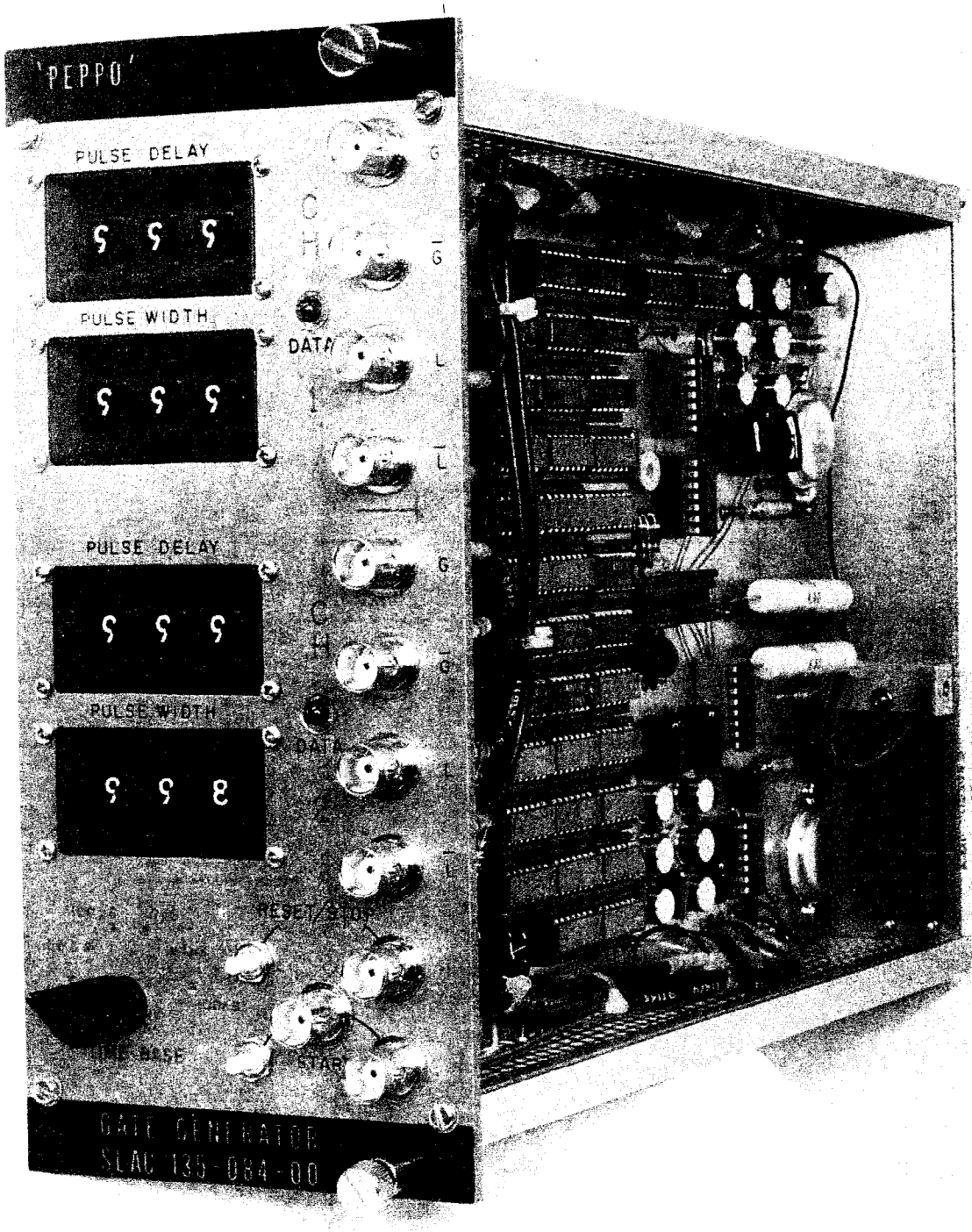

+12
+12
120
5Ω (10W)
10μF
2N2219
2N3055
1D5.6B
5.1K
10K
+6
+5.2
IN3866
10K
1μF
COMMON
GND
INPUT
OUTPUT
1μF
-5.2
10K
1D5.6B
2N3790
10μF
120
5Ω (10W)
-12
-12
2001A1

Fig. 6


'PEPPO'
PULSE DELAY
PULSE WIDTH
PULSE DELAY
PULSE WIDTH
RESET/STOP
TIME BASE
START
GATE GENERATOR
SLAC 135-084-00

2001A7

Fig. 7