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CAMAC DISCRIMINATOR-GATED LATCH WITH DIGITAL MULTIPLICITY LOGIC, "TITO" *

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Summary

A 16-channel discriminator-gated latch CAMAC module using MECL II has been designed and built for use in a phototube trigger hodoscope array. The module includes individual discriminator outputs, analog summing outputs, and high speed digital multiplicity outputs which are processed by an "analyzer" in order to decide if the particle multiplicity is suitable for streamer chamber firing. Latch data are transmitted to a PDP-9 for recording and further processing.

1. Introduction

A multiple channel discriminator-gated latch unit for a large phototube array has been designed and built to be used in an K^-p experiment at SLAC in February, 1972. For convenience, and standardization of data readout the CAMAC packaging and readout standards are used for the 16-channel module.

The phototube hodoscope is used to decide if the event is of sufficient interest to fire the primary detector, a large streamer chamber. This decision is based upon the number (multiplicity m) of phototube signals that were latched (number of particle tracks) in the event. In this experiment, if the number is sufficient ($m \geq N$, where N is the selected multiplicity) the chamber is fired, photographs are taken, and the latch data, along with other information, is read into the computer (PDP-9). If the event multiplicity is not acceptable ($m < N$), then the latches are reset, and the discriminators are ready to accept the next event for investigation. The overall delay in making a decision and resetting the latches is approximately 100 ns, which is satisfactory for this and other similar low rate experiments. Thus "slow" discriminators (< 20 MHz) are adequate.

A completely digital approach to the multiplicity requirement has been implemented for $0 < N \leq 8$. The basic addition logic is built into the latch module and the final decision is made in a special CAMAC "analyzer" module. All circuits are designed using MECL II logic. It is felt that this approach leads to a more accurate, and more stable decision network, although the production cost is greater than the more conventional analog summing methods.

For complete versatility, analog outputs are provided in each module to permit other decision criteria. Individual discriminator outputs, and an $m \geq 1$ output are provided on each latch module as well. LED indicators display the state of each latch to aid in timing, debugging, and maintenance.

2. Overall System

A block diagram of the hodoscope electronics is shown in Fig. 1. Most of the phototubes are inexpensive, low gain units, requiring high speed amplifiers. These amplifiers, with an adjustable gain of 4 to 90, are discrete circuits separately packaged in NIM and will not be discussed here. The K^- trigger is generated by other scintillation counters and standard high speed logic, and serves as the master trigger (strobe) and timing reference for the decision logic system.

The discriminator-coincidence-latch is packaged 16 channels in a triple width CAMAC module and is constructed entirely of IC's except for discretes in the input and analog sum circuits. A separate NIM output is provided for each channel so that (a) the module may be used as a 16-channel slow discriminator, or, (b) more complex decision logic may be performed. In each module the latch outputs are linearly added in two sets to generate two analog outputs, one for each 8-channel half.

MECL logic is included which digitally sums the latches in each module and adds this binary encoded sum to the accumulated sum from the previous module. Finally, the sum m emerges as 4 lines in binary code; 1, 2, 4, and overflow (the latter signifying 8 or more particles), and is sent to the analyzer. This addition logic is shown in Fig. 2.

The desired multiplicity level N is manually set into the special CAMAC crate controller (analyzer) which contains multiplicity ("greater than") logic. The selected multiplicity output is sampled by the delayed K^- trigger to allow for settling time and the gated output produces the streamer chamber trigger. In addition, unique outputs for each multiplicity level are provided by the analyzer, for use if unique multiplicities of tracks are desired. The analyzer also contains slow (20 MHz) scalers and the CAMAC readout logic. The scaler data can be read into the computer along with the five 16-bit words of latch data and the 4 bits of multiplicity data (digital sum). The scalers and readout circuits will not be described in this paper.

3. Discriminator and Gated Latch

The circuitry of the discriminator, gated-latch, and associated strobe and readout functions are shown in Fig. 3. The input circuit is terminated in 50 Ω and is protected against transient damage by the 4 diode network; the two series diodes in the signal path must be matched for forward drop. The first MC1020 performs as a simple comparator and translator to MECL levels while the second MC1020 serves to further "sharpen" the signal threshold. The threshold is adjusted by a simple voltage divider over the range -50 mV to -500 mV.

The MC1020 comparator is followed by a differentiator of the "delay" type which results in a standardized MECL pulse of about 8 ns width. Coincidence with the externally supplied strobe pulse occurs in a MECL 1023 gate, which is followed by a conventional crosscoupled flip-flop (latch) composed of MC1010's. An LED indicator is driven from the latch via a MC1039 MECL-TTL translator. Each coincidence output pulse also is translated in an emitter-coupled pair (MC1025) to a NIM output pulse which can be processed in conventional NIM logic if desired. For use as an ungated discriminator (no strobe) the strobe mode switch is put into the "OFF" position. In either case the input to output delay of this pulse is about 20 ns, the width is about 8 ns, and the risetime is about 2 ns.

The strobe gate input (NIM) is translated to MECL level in the MC1020 comparator with a fixed bias of -220 mV, and further standardized in a second MC1020. For better speed the gate signal is fanned out in four MC1010 gates each driving four coincidence gates for a total of 16 channels. The MC1010 gates also perform the gating function for the "strobe off" mode, a positive input on the MC1010 fanout permanently enabling the coincidence gate.

The flip-flop reset input (NIM) is also converted in a tandem pair of MC1020's and is OR'ed in a MC1010 with the CAMAC reset function C·S2. Normally the latches are reset by the fast input for rejected events and are reset by the computer via CAMAC for accepted and processed events.

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An additional CAMAC function is Inhibit which is translated by a MC1017 to MECL levels, and acts as a third input to the coincidence gate. This gate is normally used for a beam gate.

Data readout from the 16 latches is in standard CAMAC format using the N line for readout control. Latch signals are converted to TTL in MC1039 translators and gated in N7401 open collector gates connected to the Dataway.

The discriminator described here is extremely simple and inexpensive and is not meant to be comparable with a modern tunnel diode discrete circuit discriminator. However it is quite acceptable for many low rate noncritical applications. In this particular case the phototube signals are all large compared to the nominal threshold (-100 mV for this experiment) so that slewing and risetime considerations are minimized. The nominal gate width to be used in this experiment is 20 ns. With this gate width the coincidence overlap range is about 30 ns. Note that the discriminator is dc coupled; however, since it includes a differentiator, it is slope sensitive — all pulses must be "fast" to give a discriminator output. The repetition rate is quite fast; although only 20 MHz was needed, a channel has been measured beyond 50 MHz with a 10 ns input pulse. Threshold sensitivity curves are shown in Fig. 4 for two settings, -50 mV, and -100 mV, measured with a fast ($\approx$ 1 ns) risetime pulser. Slewing with a fast 10 ns pulse is about 2 ns over the range 2X - 10X threshold.

4. Digital Addition Logic

The positive true latch outputs, denoted by b-1 to b-16, form the inputs to the digital addition logic. As mentioned previously in Section 2 the basic principle of the multiplicity is the successive parallel addition of latch signals module-by-module, finally to be analyzed in a separate module. Figure 5 shows the digital addition logic in each module, based upon the use of MC1019 full adder having a nominal propagation delay of 7 ns. In order to use the adder the input must be encoded in binary format. Thus the first step in the addition process is to encode the latch signals into two sets of 4 line binary encoded data in the "8 Line Encoder Logic," which is described in Section 5. Note that the "8" bit in either half represents an overflow, hence these signals go directly to the MC1001 overflow OR gate, thence to the analyzer where an overflow (m > 7) is indicated.

The first rank of MC1019 adders connected as a conventional ripple adder sums the two halves resulting in a 3 bit sum (0 through 7) and a carry output, representing m > 7. This carry overflow is OR'ed in the carry OR gate to be transmitted to the analyzer. After this rank of addition there is an OR of the adder 1, 2, and 4, and encoder 8 outputs. It can be seen that this function indicates a data sum in the module of m $\geq$ 1. The logic signal is converted to NIM in the emitter-coupled pair (MC1025); the overall delay of this output is about 50 ns.

The accumulated binary sum from the previous modules enters via an auxiliary printed circuit connector located above the CAMAC 86 pin printed circuit connector. This 3 bit sum is added to the 3 bit sum for the current module in a second rank of MC1019 ripple carry adders. The total, representing the new accumulated sum, is passed on to the next module at MECL levels via the same auxiliary connector. Note that the final carry from the second rank of adders is OR'ed into the overflow OR gate since it indicates m > 7. The overflow from the previous module is also OR'ed in the overflow gate to transmit a previous overflow through to the analyzer. The complement of overflow is also sent out of the module, but this is used only if the next module is the analyzer.

The overall delay from the discriminator input to the digital multiplicity output of the module is approximately 50 ns.

5. The Eight Line Encoder

Multiplicity, or polling, logic does not readily exist in integrated circuit form. One direct approach is to use single bit adders to form sums of pairs of inputs. Then these intermediate sums are added in a second rank of adders, etc. until a fully encoded sum results. With this approach, for 16 input lines, it takes 22 chips (MC1019) to encode the multiplicity into two sets of binary coded lines "1", "2", "4", "8". As shown in Fig. 5 it then takes 3 more adder chips to combine these into a single set of sum lines weighted "1", "2", and "4", plus an OR gate for the overflow.

A better solution to the encoding problem however, in terms of chip count, was found by implementing the early stages of addition directly in logic gates instead of full adders where the carry function input is not fully utilized. In this manner a design was developed using 13 gating chips instead of the 22 adder chips. It does not pay, however, to implement with logic gates beyond the level selected, as the function becomes increasingly complex; note that only 3 more adder chips are required to add the two sets of "1", "2", "4", sums, after the initial encoding.

The logic diagram of the eight line encoder is shown in Fig. 6. Each set of four input lines is converted to a "1", "2", "4" sum as an intermediate stage. This logic is fairly simple and is based on the addition of two groups of two each. The "1" output for example should be given for an input multiplicity of 1 or 3, hence it is an exclusive OR function. The "2" output should be given for 2 in one group and not 2 in the other, or 1 in each group. The "4" output of course is given only for the case of all four inputs. This logic can be written as follows:

$$\text{"1"} = (A \oplus B) \oplus (C \oplus D)$$

$$\text{"2"} = (A \oplus B) \cdot (C \oplus D) + (A \cdot B) \oplus (C \cdot D)$$

$$\text{"4"} = ABCD$$

The diagram shows both sets of these gates for the 8 inputs. Note that the OR function for the "2" bit is a wired emitter-OR of the MECL emitter follower outputs.

The two sets of "1", "2", "4" lines are added in the remaining logic shown in Fig. 6. It should be remembered that the encoded sum for each half has a maximum sum of 4. The "1" bit is the exclusive OR of the two input "1" bits. The "2" bit is the exclusive OR of the two input "2" bits, but must be exclusively OR'ed with the case where there are two one bits. The "4" bit as can be seen is the case of two "1"s and a "2" or two "2"s or a single "4" input. Of course the "8" output is given only for the case of two "4" inputs. Basically what is described here is a special case of conventional full adder logic.

6. Analog Output Circuits

The negative true latch outputs denoted a-1, to a-16 in Fig. 3 are used to generate two 8 level analog outputs as shown in Fig. 7. In this circuit the MC1035 is used as a feedback amplifier summing the individual currents at the node point. The gain in this configuration is approximately 1/8; thus each 800 mV signal at the input represents 100 mV at the output for a total range of 800 mV. The output is buffered and shifted back to NIM level by the 2N2905 emitter-follower which produces an output risetime of about 5 ns into 50 Ω. The total delay from the discriminator input to the analog output is about 30 ns.

The adjustment potentiometer is used to set the offset bias and adjust for optimum linearity of the 8 output levels.

7. The Analyzer

Only the multiplicity logic circuits of the analyzer, shown in Fig. 8, will be described here. Other functions not shown

include 20 MHz scalers and the necessary decoding and buffering functions common to a CAMAC controller.

The input sum data from all the latch modules enters via the CAMAC auxiliary connector. The three sum lines "1", "2", and "4" are immediately gated with overflow so that only the overflow line is true during the overflow condition, thus preventing spurious outputs during the overflow case. The 3 lines are then decoded in a MC1043 decoder to produce a unique output for each multiplicity number. These outputs are then strobed or sampled in a MC1004 to allow for system settling time, and the output is converted to NIM level by the MC1025 emitter-coupled pair. Note that the NIM strobe input is translated in a MC1035 Schmitt trigger. This is similar to the MC1020 shifting method described earlier and exists here only for historical reasons.

The multiplicity ("greater than") logic is implemented using a combination of the uniquely decoded outputs from the MC1043 and conventional gating. This function could be implemented in many ways but it is felt that the solution shown represents a reasonable trade off of chip count and propagation delay. In only one case the propagation delay is four gate stages; in all other cases it is 3 or less.

The final multiplicity output level is selected by a rotary switch, and after strobing is converted to NIM level again with a MC1025 emitter-coupled pair. Signals from the majority logic are conveyed through the switch on coaxial line to improve the transmission, even though the distance is quite short (4").

It should be pointed out that the nature of the decision could be changed by modifying the logic of the analyzer. For example, one could build an analyzer which produced an output for $N_1 < m < N_2$ where N_1 and N_2 are upper and lower bounds and m is the multiplicity level.

8. Packaging

The 16-channel discriminator latch is packaged in a triple width NIM module as shown in the photograph (Fig. 9). All front panel connections use LEMO connectors. The circuits are packaged on two boards which can be separated for servicing. Considerable attention has been given to the use of ground planes, component layout related to signal paths, decoupling and distribution of power. In fact a second printed circuit layout was done to improve these characteristics. The module draws 300 mA at + 6 V, and 2 A at - 6 V. The reduced voltage for the MECL and TTL circuits is dropped from the 6 V supplies through several 1 A diodes spaced over the boards for better decoupling.

Note that the strobe and reset are bridging inputs in which the coax goes to the high impedance circuit input and returns to the front panel for minimum disruption of the 50 Ω transmission.

The analyzer is packaged in a double width CAMAC module which is used in the crate control station. However, since it is one-of-a-kind, wire-wrap construction is used to minimize cost and development time and to facilitate changes.

Acknowledgements

The authors would like to thank Dr. A. Odian and Dr. F. Villa of Group D at SLAC for whose experiments this equipment has been built. Their many comments and suggestions have been sincerely appreciated.

We also point out the cooperation of the SLAC Electronics Fabrication Shop where the complex printed circuit work and fabrication was done. P. Arechiga of the Electronics Instrumentation Group wired the analyzer module.

Figure Captions

FIG. 1--System block diagram.

FIG. 2--Digital decision logic block diagram.

FIG. 3--Discriminator and latch circuit.

FIG. 4--Discriminator threshold curves.

FIG. 5--Digital addition logic.

FIG. 6--Eight line encoder logic.

FIG. 7--Analog summing circuit.

FIG. 8--Analyzer multiplicity logic.

FIG. 9--Photograph of the modules.

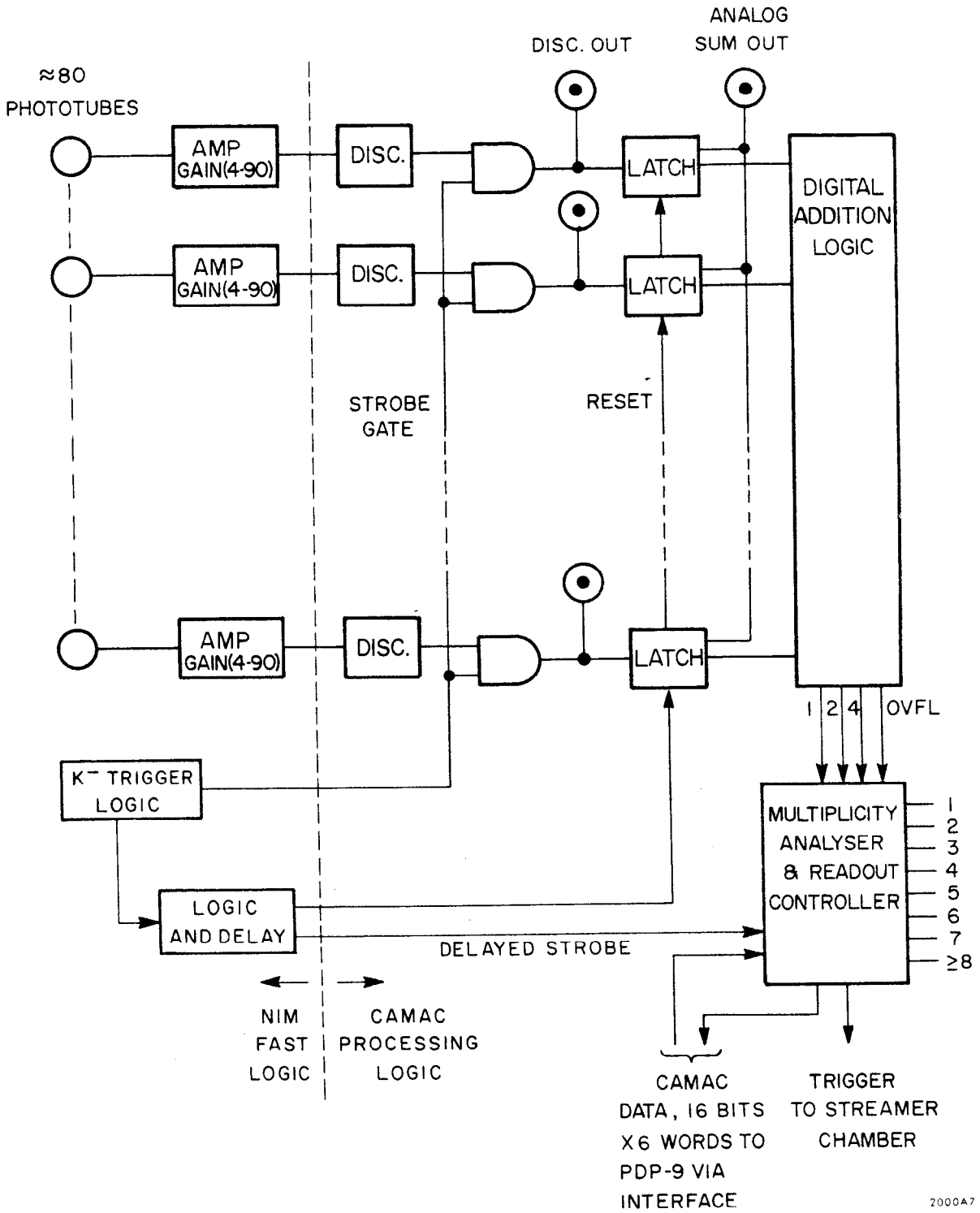

≈80
PHOTOTUBES
AMP
GAIN(4-90)
DISC.
DISC. OUT
ANALOG
SUM OUT
LATCH
DIGITAL
ADDITION
LOGIC
STROBE
GATE
RESET
1 2 4 OVFL
K⁻ TRIGGER
LOGIC
MULTIPLICITY
ANALYSER
& READOUT
CONTROLLER
1
2
3
4
5
6
7
≥8
LOGIC
AND DELAY
DELAYED STROBE
NIM
FAST
LOGIC
CAMAC
PROCESSING
LOGIC
CAMAC
DATA, 16 BITS
X6 WORDS TO
PDP-9 VIA
INTERFACE
TRIGGER
TO STREAMER
CHAMBER
2000A7

FIG. 1

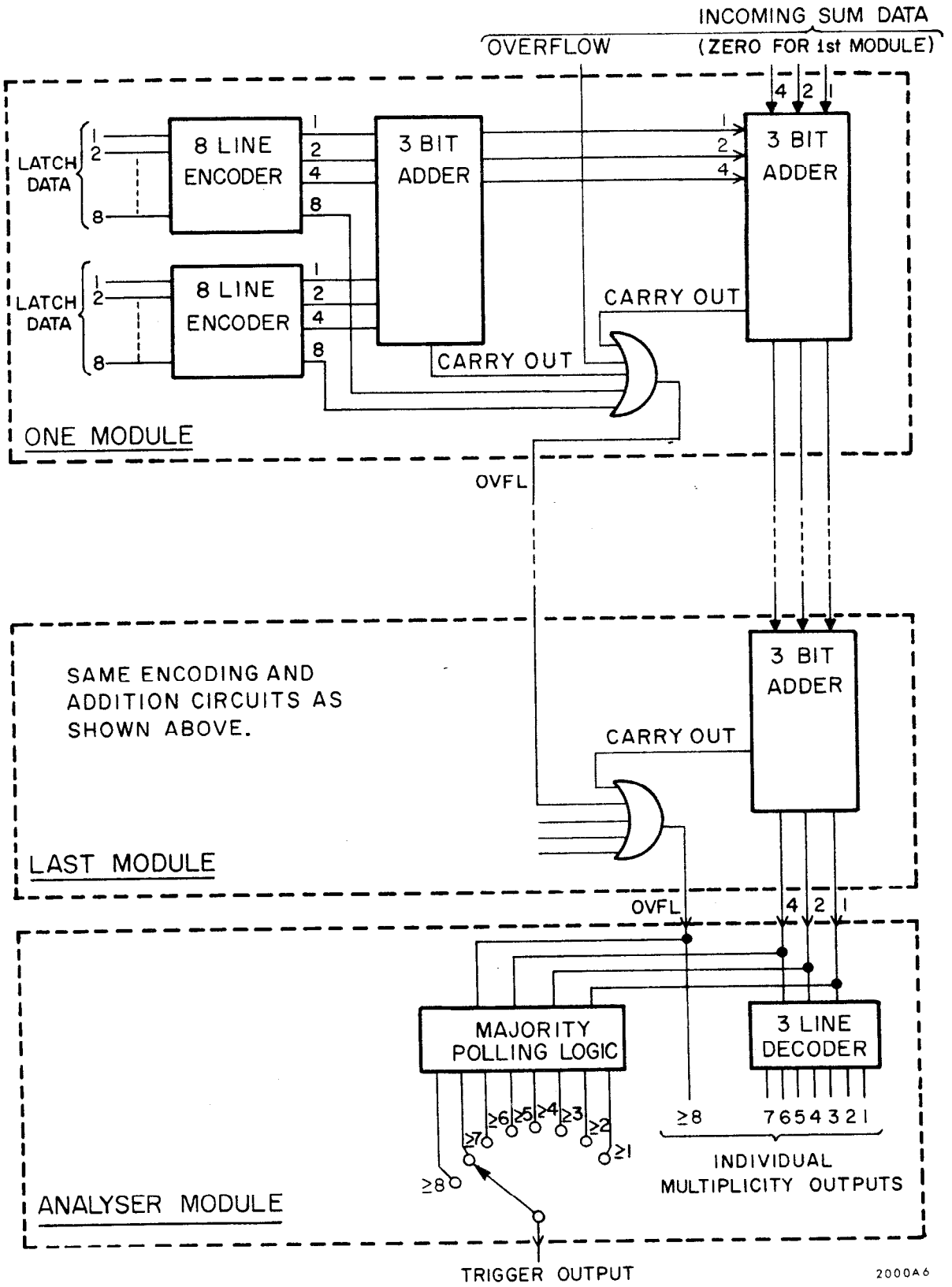

INCOMING SUM DATA
(ZERO FOR 1st MODULE)
OVERFLOW
4 2 1
LATCH DATA
1
2
8
8 LINE ENCODER
1
2
4
8
3 BIT ADDER
1
2
4
3 BIT ADDER
CARRY OUT
CARRY OUT
ONE MODULE
OVFL
SAME ENCODING AND ADDITION CIRCUITS AS SHOWN ABOVE.
3 BIT ADDER
CARRY OUT
LAST MODULE
OVFL
4 2 1
MAJORITY POLLING LOGIC
3 LINE DECODER
≥7
≥6
≥5
≥4
≥3
≥2
≥1
≥8
≥8
7 6 5 4 3 2 1
INDIVIDUAL MULTIPLICITY OUTPUTS
ANALYSER MODULE
TRIGGER OUTPUT
2000A6

FIG. 2

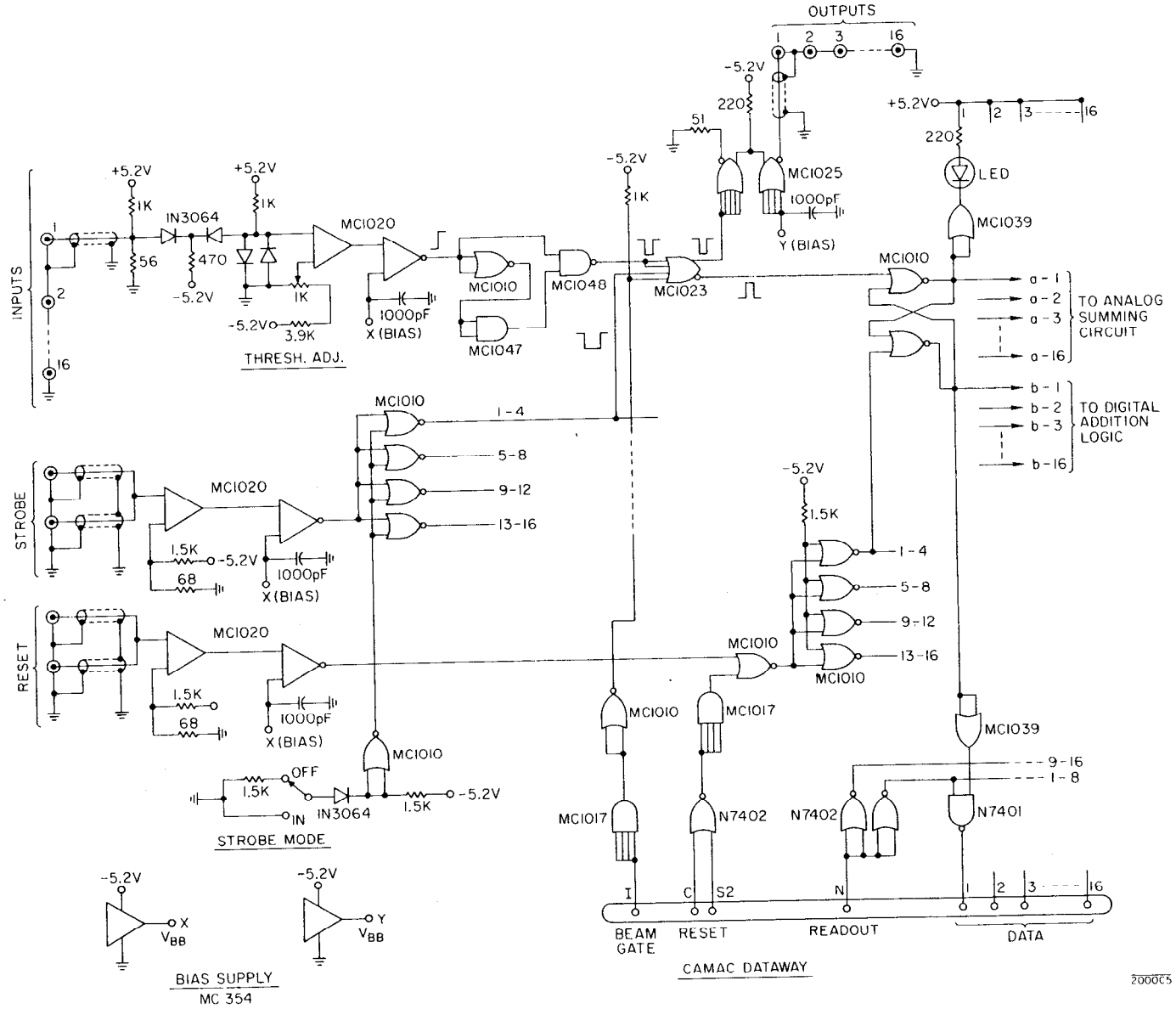

OUTPUTS
1 2 3 16
-5.2V
220
51
+5.2V
220
LED
MC1039
MC1025
1000pF
Y (BIAS)
INPUTS
+5.2V
1K
IN3064
56
470
-5.2V
MC1020
1K
-5.2V
3.9K
1000pF
X (BIAS)
THRESH. ADJ.
MC1010
MC1047
MC1048
-5.2V
1K
MC1023
MC1010
a-1
a-2
a-3
a-16
TO ANALOG SUMMING CIRCUIT
b-1
b-2
b-3
b-16
TO DIGITAL ADDITION LOGIC
STROBE
MC1020
1.5K
-5.2V
68
1000pF
X (BIAS)
MC1010
1-4
5-8
9-12
13-16
RESET
MC1020
1.5K
68
1000pF
X (BIAS)
-5.2V
1.5K
1-4
5-8
9-12
13-16
MC1010
MC1010
MC1010
MC1017
MC1039
9-16
1-8
OFF
1.5K
IN
IN3064
1.5K
-5.2V
MC1010
STROBE MODE
MC1017
N7402
N7402
N7401
-5.2V
X
V_{BB}
-5.2V
Y
V_{BB}
BIAS SUPPLY
MC 354
I
C
S2
N
1 2 3 16
BEAM GATE
RESET
READOUT
DATA
CAMAC DATAWAY
200005

FIG. 3

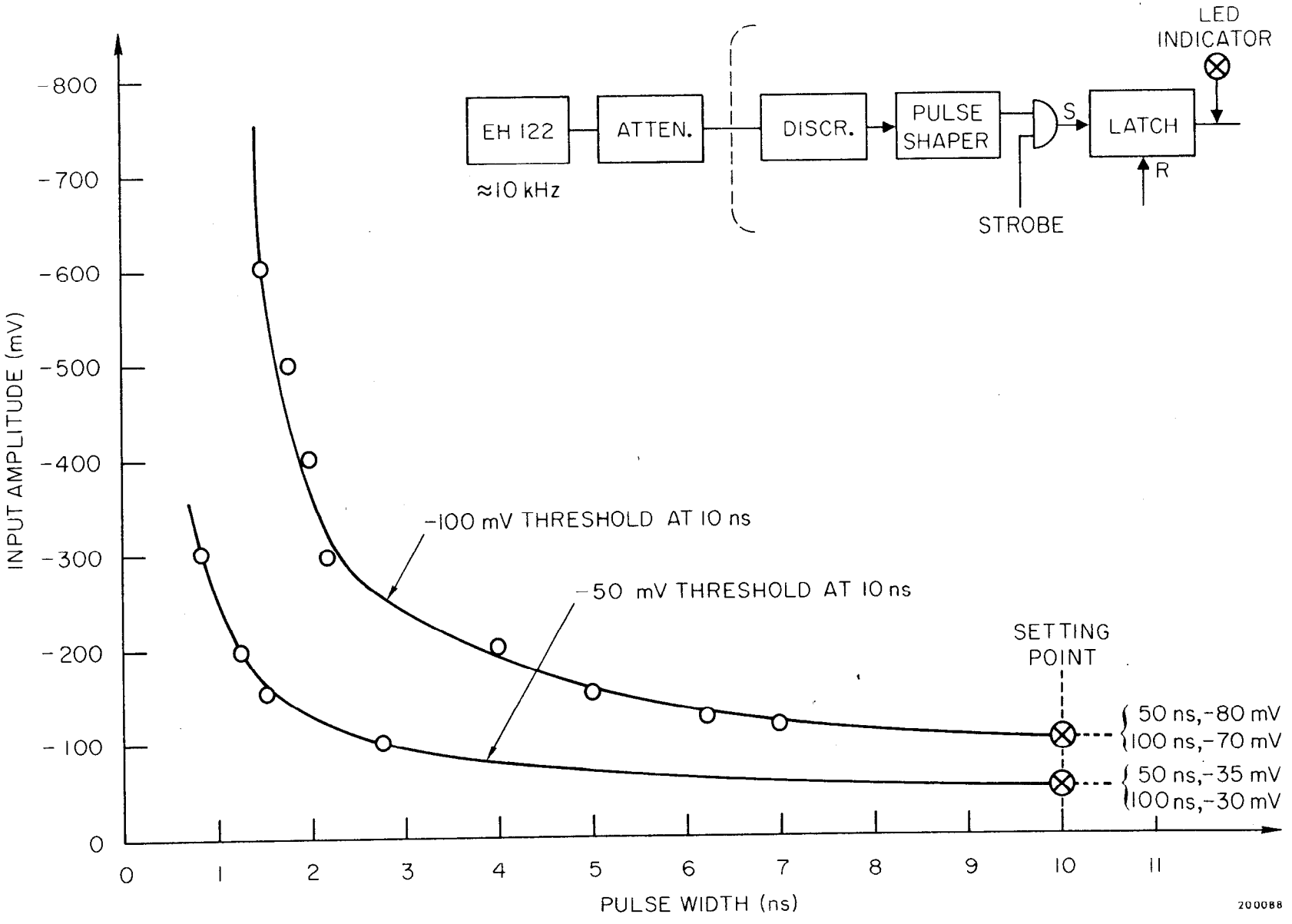

LED
INDICATOR
EH 122
ATTEN.
DISCR.
PULSE
SHAPER
S
LATCH
R
≈10 kHz
STROBE
INPUT AMPLITUDE (mV)
-800
-700
-600
-500
-400
-300
-200
-100
0
-100 mV THRESHOLD AT 10 ns
-50 mV THRESHOLD AT 10 ns
SETTING
POINT
50 ns,-80 mV
100 ns,-70 mV
50 ns,-35 mV
100 ns,-30 mV
0
1
2
3
4
5
6
7
8
9
10
11
PULSE WIDTH (ns)
200088

FIG. 4

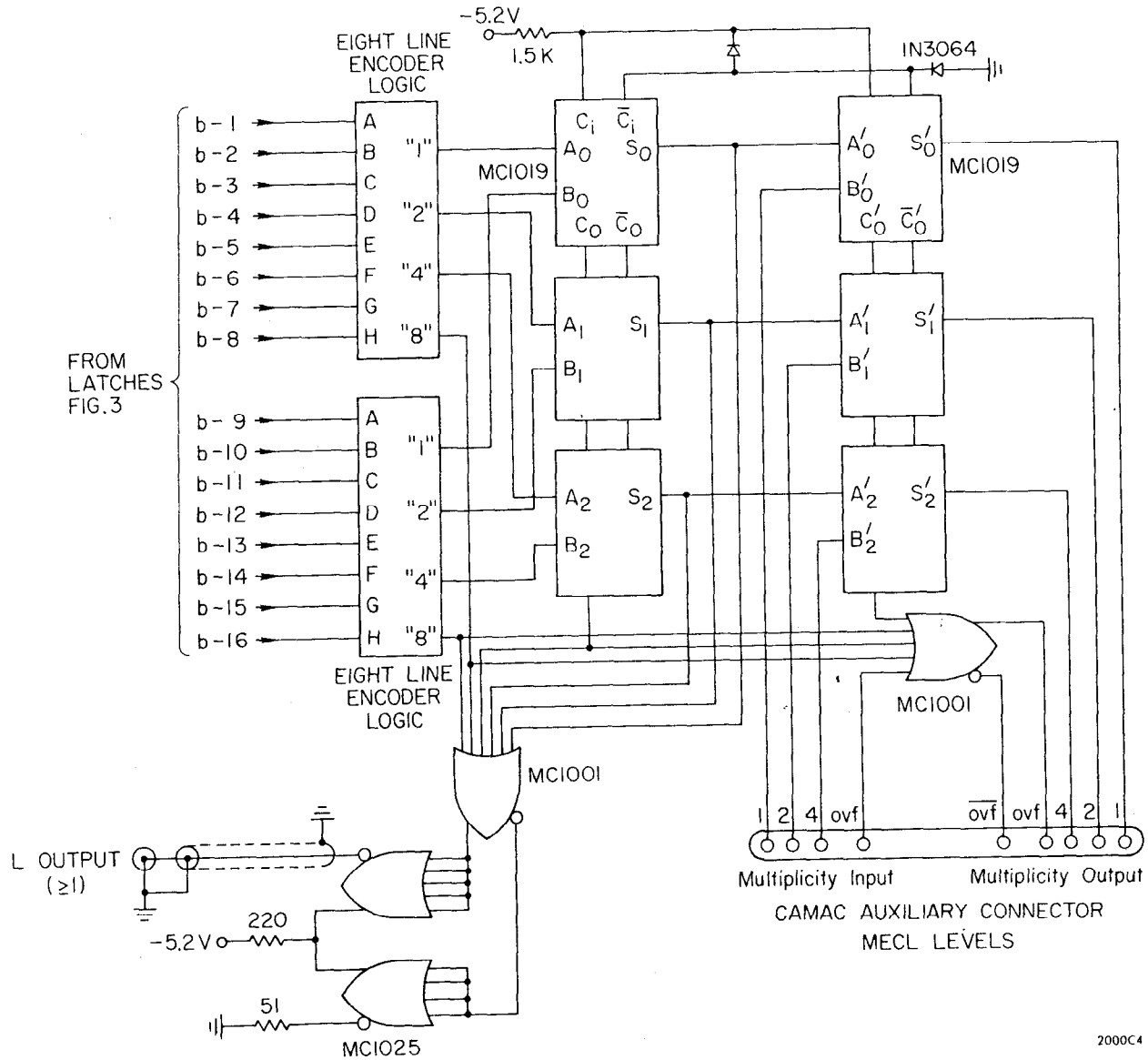

-5.2V
1.5 K
EIGHT LINE ENCODER LOGIC
IN3064
MC1019
MC1019
FROM LATCHES FIG.3
b-1
b-2
b-3
b-4
b-5
b-6
b-7
b-8
b-9
b-10
b-11
b-12
b-13
b-14
b-15
b-16
"1"
"2"
"4"
"8"
EIGHT LINE ENCODER LOGIC
MC1001
MC1001
L OUTPUT (≥1)
220
-5.2V
51
MC1025
1 2 4 ovf
ovf ovf 4 2 1
Multiplicity Input
Multiplicity Output
CAMAC AUXILIARY CONNECTOR
MECL LEVELS
2000C4

FIG. 5

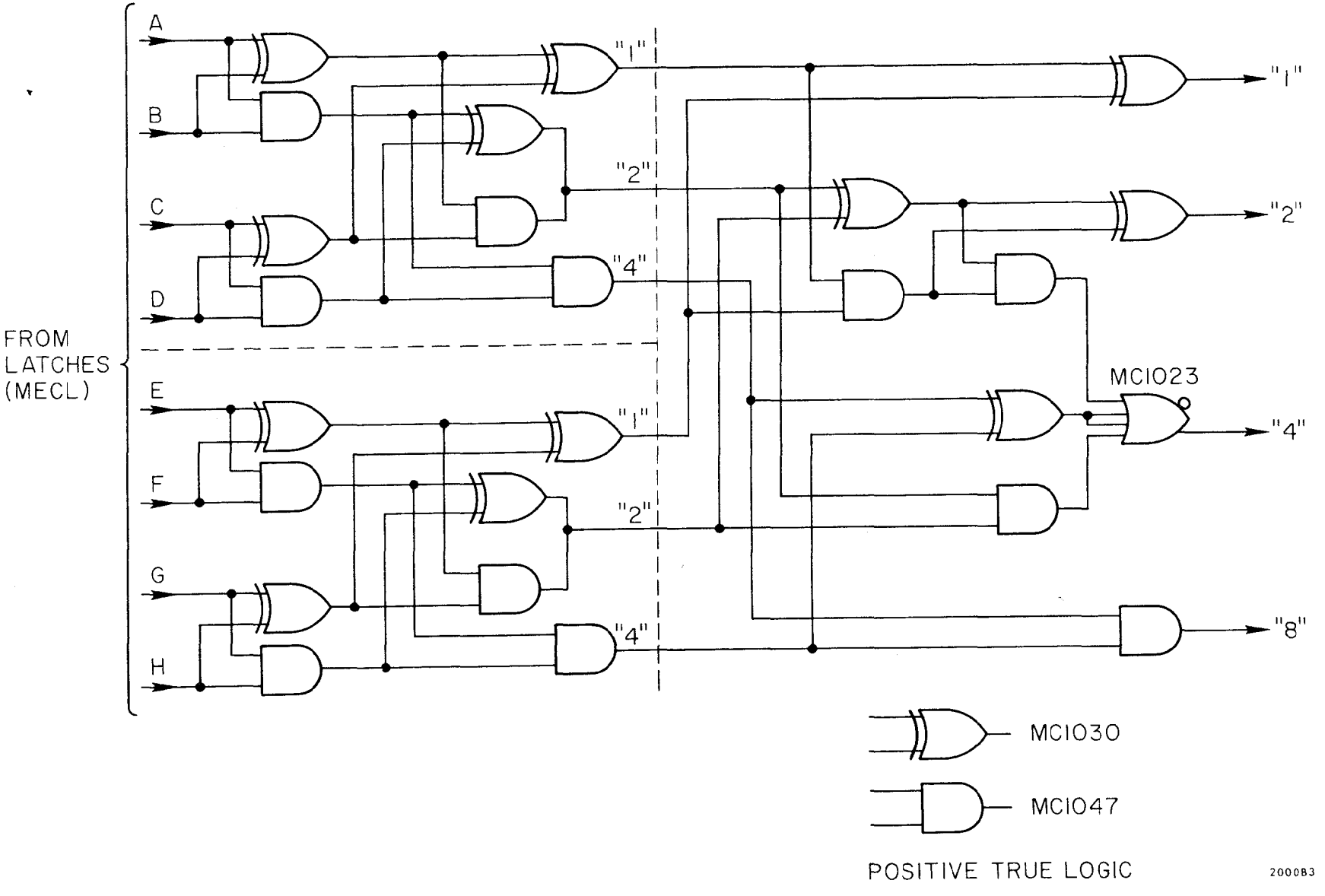

A
B
C
D
FROM
LATCHES
(MECL)
E
F
G
H
"1"
"2"
"4"
"1"
"2"
"4"
MC1023
"1"
"2"
"4"
"8"
MC1030
MC1047
POSITIVE TRUE LOGIC
200083

FIG. 6

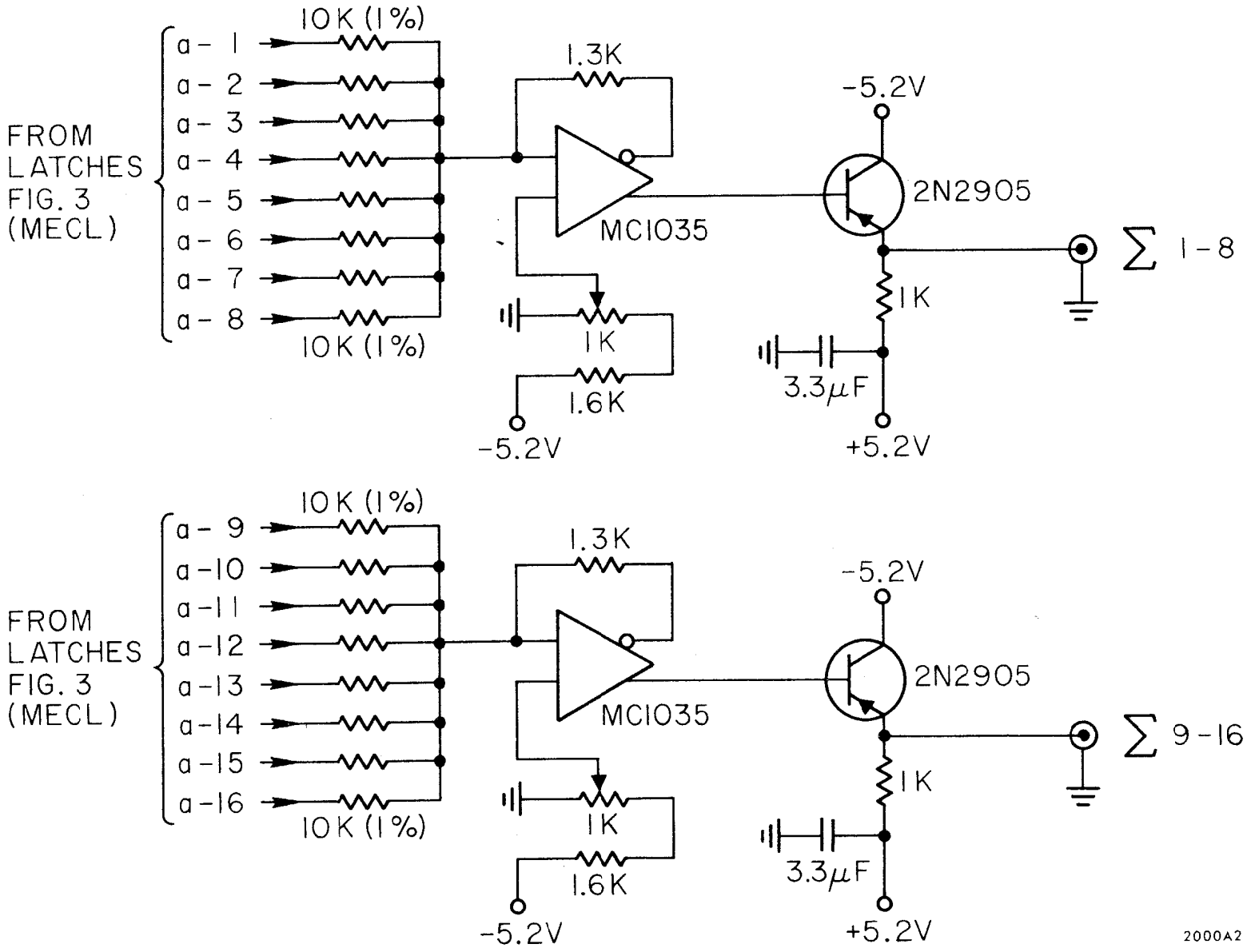

FROM LATCHES FIG. 3 (MECL)
a - 1
a - 2
a - 3
a - 4
a - 5
a - 6
a - 7
a - 8
10K (1%)
10K (1%)
1.3K
1K
1.6K
-5.2V
MC1035
2N2905
-5.2V
1K
3.3μF
+5.2V
Σ 1-8
FROM LATCHES FIG. 3 (MECL)
a - 9
a -10
a -11
a -12
a -13
a -14
a -15
a -16
10K (1%)
10K (1%)
1.3K
1K
1.6K
-5.2V
MC1035
2N2905
-5.2V
1K
3.3μF
+5.2V
Σ 9-16
2000A2

FIG. 7

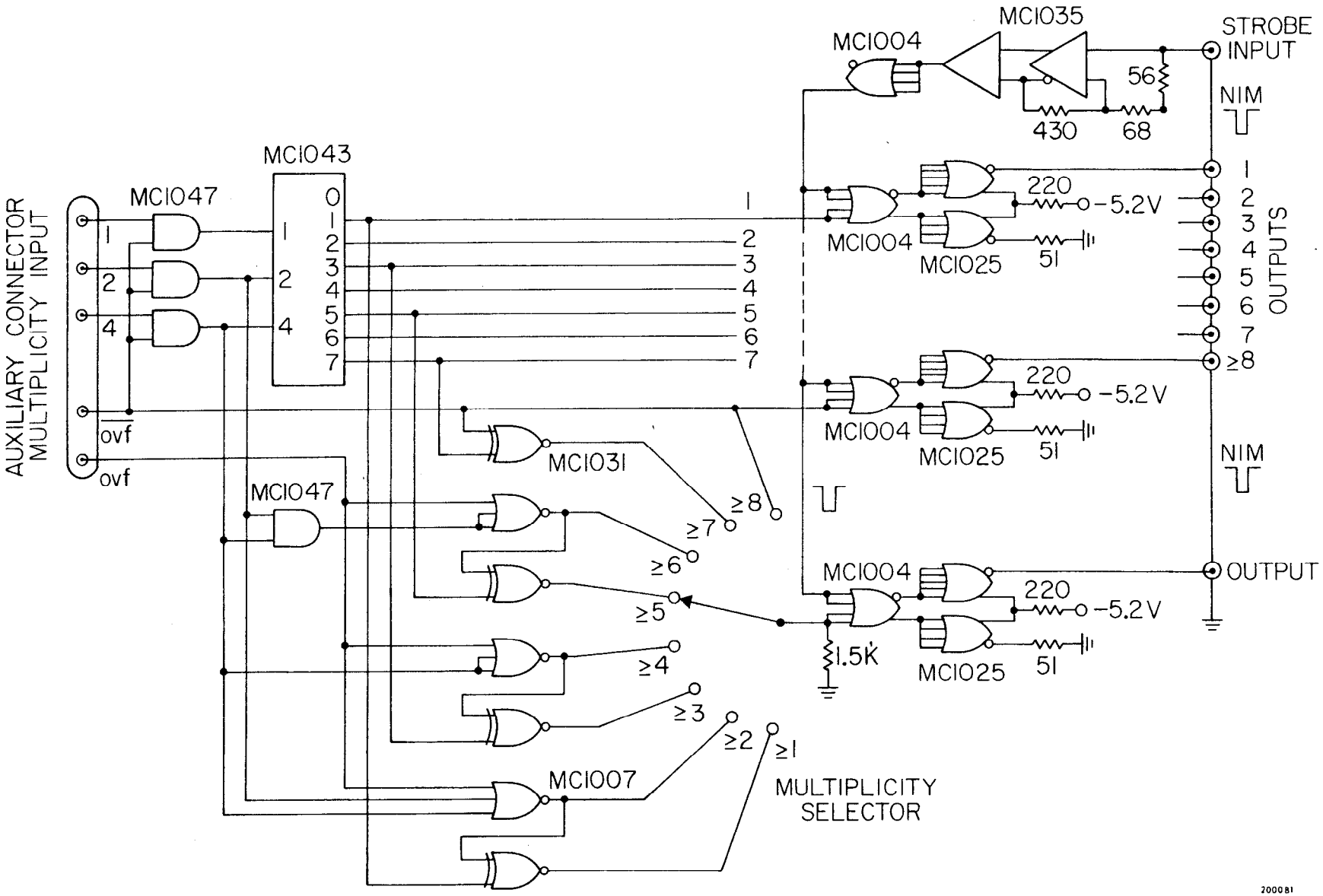
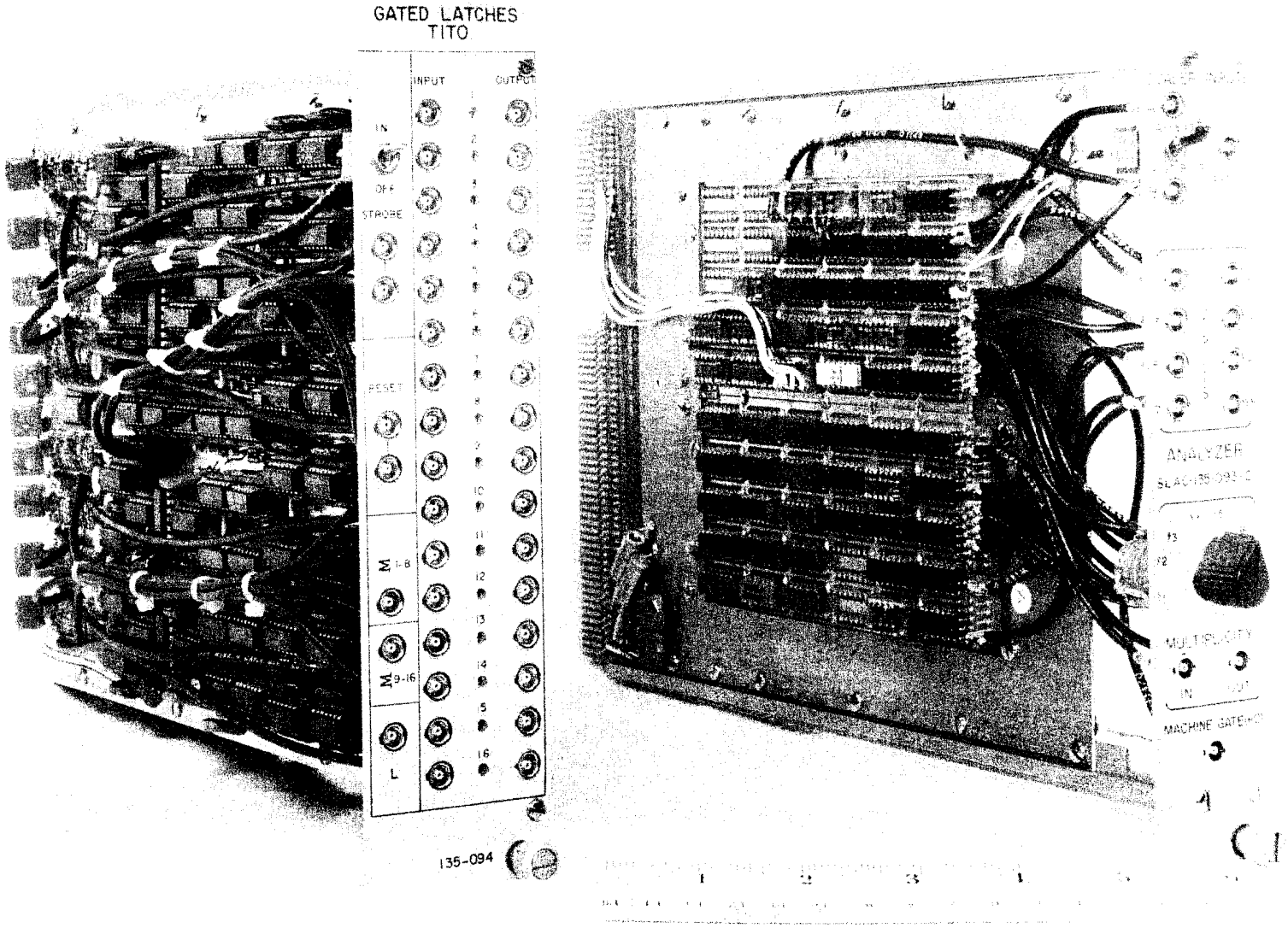

AUXILIARY CONNECTOR
MULTIPLICITY INPUT
1
2
4
ovf
ovf
MC1047
MC1043
MC1047
MC1031
MC1047
MC1007
MC1004
MC1035
MC1004
MC1025
MC1004
MC1025
MC1004
MC1025
STROBE
INPUT
NIM
56
430
68
220
-5.2V
51
220
-5.2V
51
NIM
220
-5.2V
51
1.5K
OUTPUTS
OUTPUT
≥8
≥7
≥6
≥5
≥4
≥3
≥2
≥1
MULTIPLICITY
SELECTOR
200081

FIG. 8


GATED LATCHES
TITO
INPUT
OUTPUT
IN
OFF
STROBE
RESET
M 1-8
M 9-16
L
135-094
ANALYZER
MULTIPLEXER
IN
OUT
MACHINE GATE

2000A9

FIG. 9