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STATUS OF INTER-LABORATORY DEVELOPMENT OF A WIRE CHAMBER INTEGRATED CIRCUIT *

by

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I. INTRODUCTION

In October, 1970, a small group of interested people met at the Lawrence Radiation Laboratory in Berkeley to discuss the possibility of collaborating on the development of a special integrated circuit for proportional wire chambers. Attendees of this initial meeting were H. Steiner and F. Kirsten of LRL, M. Atac of NAL, R. Lanza of MIT, A. Minten of CERN, and J.-L. Pellegrin and the writer of SLAC. It was decided that there was sufficient interest to organize a more general follow-up meeting in conjunction with the Nuclear Science Symposium in New York in November, 1970. H. Steiner mailed invitations to all known interested laboratories, and also to two semiconductor manufacturers, Fairchild and Motorola.

The two day meeting, held on November 2-3, 1970, was attended by about 60 people from essentially every major laboratory, including CERN. The first day was devoted to formal presentations, and the second to a round-table discussion involving manufacturers' representatives together with several laboratory representatives.

The final consensus of the New York meeting was that a sub-group should be formed to produce a specification with which to solicit manufacturers' proposals. Thus, immediately after the New York meeting, a Specifications Committee met at LRL-Berkeley to consolidate a specification. Participants in this effort were:

M. Atac, NAL: H. Steiner and F. Kirsten, LRL; I. Pizer and F. Sauli, CERN; R. Lanza, MIT; T. Nunamaker, University of Chicago; and J.-L. Pellegrin and the writer, SLAC. A preliminary specification[1] was subsequently issued from Berkeley on November 20, 1970.

Following the LRL Specifications Committee meeting, the writer was delegated the responsibility of submitting the specification to manufacturers, and of coordinating all proposals. This effort has essentially been continuous since the early part of December, 1970. The major developments to date are summarized in the remainder of this paper.

II. SUMMARY OF THE SPECIFICATION

The general features of the preliminary specification can be seen in the circuit of Fig. 1, the timing diagram of Fig. 2, and the specifications summary of Table I.

Several aspects of the specification should be noted. First, it was not explicitly required to use TTL as opposed to ECL logic; nor to use horizontal rather than vertical partitioning of functions. It was recognized that either of these options might have distinct advantages when the detailed design is considered. Also, although the original idea was to develop a monolithic circuit, the option of a hybrid circuit was left open.

The one major technical decision inherent in the design is that a monostable shall be used for the delay element. If horizontal, rather than vertical, partitioning is used, then the monostable becomes an inseparable part of the circuit, and no other form of delay (such as a passive transmission or delay line) can be used. This was one of the basic decisions made at the original New York meeting.

A second technical point of note is that the original specification calls for a minimum input threshold of 5 ± 2 mV. This reflects the feeling at the time that the so-called "magic" gas mixtures would be generally used, and the 0.5 to 1 mV thresholds required for other gases such as Ar-CO_2 would not be necessary. At a proposal review meeting at SLAC on April 13, 1971, this part of the specification was changed to

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read "1 mV typical, 2 mV maximum", reflecting the consensus that a circuit with the lower threshold would be generally more useful.

III. PROPOSAL REVIEW

In December, 1970, the specification was sent to 5 manufacturers: Motorola, Fairchild and Texas Instruments in the U.S.; Valvo-Phylips in Germany; and SESCOSEM in France. All companies responded except Valvo-Phylips. Motorola expressed interest, but stated that their facilities were loaded and they could not consider the job until April. Fairchild indicated that a formal proposal for a monolithic would be forthcoming. Texas Instruments indicated a similar intention. SESCOSEM, after some prodding, eventually submitted a proposal for a monlithic.

There ensued a lengthy period of negotiation in order to secure formal proposals. Fairchild's plan to submit a proposal for a monolithic collapsed because of lack of internal support from the various departments involved. The Texas Instruments effort was stalled first because of a management change, and second when CERN independently requested a proposal for a hybrid.

Finally, on February 25, 1971, a proposal for a monolithic development was received from Texas Instruments, and on March 10, a follow-up proposal for a 2-channel hybrid was received. On March 29, Fairchild also submitted a hybrid proposal. In view of these developments, the existing MECL circuit developed by Pellegrin at SLAC was submitted to Motorola in order to obtain a quotation on a hybrid; the verbal quotation was received April 12, just prior to a review meeting held at SLAC on April 13. (The formal quotation was received on April 19, 1971.) Also, just prior to this meeting, SESCOSEM submitted their proposal for a 3-chip vertically integrated monolithic.

A proposal review meeting was held at SLAC on April 13, 1971. Attendees were: M. Atac and Ron Martin, NAL; T. Nunamaker, University of Chicago; Ray Martin, LASL; R. Lanza, MIT; B. Jackson, F. Kirsten, H. Steiner, J. O'Keefe, S. Parker, LRL; and J.-L. Pellegrin and the writer, SLAC. The various circuit options which were considered are shown in Table II. The main data of interest are as follows:

1. Development of a monolithic will cost $40,000. Production cost per channel projected at $2 - $3.

2. Cost of TTL hybrid from Fairchild or Texas Instruments projected at $4 - $5 in 100,000 quantities.

3. Motorola quotation on TEDDY of > $10/channel is not competitive.

4. SESCOSEM proposal contained no indication of method of implementation.

5. Information from CERN included for interest only. No formal proposals received from Phylips or GE-Marconi.

The major conclusion of the meeting was to concentrate further efforts on developing a TTL hybrid version of the circuit, to be followed by a monolithic at a later time. This decision was made principally because of the shorter development time for a hybrid, as well as the lower development cost, plus the lack of encouragement for an ECL hybrid or monolithic from Motorola. The projected production cost of the TTL hybrid of the order of $5/channel in large quantities was considered sufficiently attractive to solve the short-term requirements. It should be emphasized, however, that the ultimate goal is to attempt to develop a monolithic, in order to achieve lowest possible costs as well as optimum reliability. The hybrid of course may point out problems which make further development of a monolithic impractical or economically unattractive.

As noted previously, the threshold requirement was changed to 1 mV typical, 2 mV maximum. The meeting concluded with the decision to pursue further development of a TTL hybrid with Fairchild and Texas Instruments in parallel, with the added requirement of a lower threshold voltage.

At that time it was estimated that the most optimistic date for delivery of production hybrids would be about September 1, 1971. This is no longer a realistic target date.

IV. SPECIFICATION REVIEW

Several additional points concerning the specifications were discussed at the April 13 meeting:

1. The preferred input circuit specification was changed to make $1\,K\Omega \leq Z_{in} \leq 2\,K\Omega$. Protection required as originally specified. See Fig. 3a.

2. A preferred test circuit is shown in Fig. 3b. Any ac-coupled circuit which produces the desired pulse shape is acceptable.

3. Crosstalk - 100 times overdrive on one channel should not cause triggering of adjacent channels.

4. Delay trim - Monostable delay must be accurate to ± 2.5%, adjustable 100 nsec to at least 500 nsec. If internal trimming only is used, it should be performed at a setting of 300 nsec.

5. Channels should not respond to positive pulses of 100 times over threshold.

These points were subsequently relayed to Fairchild and Texas Instruments by letter.

V. PROTOTYPE TESTING

At the April 13 meeting the following standard tests were suggested for evaluating prototypes:

1. Threshold vs. pulse width
2. Delay vs. amplitude (slewing)
3. t_{pd} to FAST out vs. V_{in}
4. Monostable delay jitter vs. Vcc, ΔT, rep rate
5. Coincidence curve at min. WRITE gate width
6. Crosstalk for 40 db overdrive
7. Response to positive inputs
8. Operation in 20 KG field
9. Operation on Chamber - time resolution using $Ar\text{-}CO_2$

It was further agreed that a number of laboratories would independently evaluate the prototype before any general conclusion was reached. Participating laboratories will include NAL, LRL, LASL, MIT, University of Chicago and SLAC.

VI. STATUS OF FAIRCHILD PROPOSAL

The original Fairchild proposal specified two packages, one containing 4 amplifier channels, the other containing 4 one-shots plus logic. The circuits are shown in Figs. 4 and 5. The package outline is shown in Fig. 6.

In June, two prototype circuits of each type were delivered to SLAC. Tests on the amplifiers immediately revealed a problem in that input thresholds were much higher than specified. This was traced to the fact that for a high driving impedance, current offsets inherent in the μA733 amplifier limited reliable thresholds to considerably higher than 10 mV. Fairchild recognized this as a fundamental problem and is preparing a new proposal based on a μA760, rather than the μA733.

The logic portion was given a cursory test. The main problem here appears to be that there is an excessive spread in monostable delay between channels, and no provision for external trimming of each channel.* The units were subsequently sent to LRL and MIT for further testing.

The original prototypes were produced at no cost to the laboratories. It appears that the next round of development on an improved circuit, after satisfactory evaluation of a breadboard, will cost between $5,000 and $10,000. This amount will have to be raised and an order placed before further work can proceed.

VII. STATUS OF TEXAS INSTRUMENTS PROPOSAL

The original proposed circuit is shown in Fig. 7. The proposed package is a 24-pin dual in-line for 2 horizontal channels. The original circuit front-end was examined by Ron Martin of NAL. He concluded that the SN75107 could not meet the 5 mV threshold requirement, let alone something lower. Texas responded to the request for a 1 mV threshold by stating that they thought it could be achieved, but would require $4500 to produce 5 prototype units. This amount was raised between LRL, NAL, MIT, Chicago and SLAC, and an order was placed in late July. Work is now underway, and prototypes are expected in about 6 weeks.

CERN has independently pursued a hybrid development and according to a letter dated 20 July 1971 from F. Sauli, has decided to accept a Texas Instruments proposal. The circuit differs slightly from the original proposal (see Fig. 8). Principally, the threshold requirement is still 5 ± 2 mV; only internal timing components are specified; and no input protection is specified.

VIII. OTHER PROPOSALS

A Motorola representative is reviewing their original ECL hyb rid proposal for possible further action.

A number of different hybrid manufacturers have reviewed the specification and some have forwarded quotations. The purely hybrid manufacturer is purposely being discouraged from participation because of our long-range interest in a completely monolithic circuit.

* Note - Fairchild has reviewed this and states that the one-shots were never internally trimmed. They feel that the width tolerance can be met without the need for external trimming.

IX. CONCLUSION

Progress is being made toward achieving a special TTL integrated circuit for wire chambers. Input sensitivity appears to pose the major problem in the design.

The time scale of development is much longer than anticipated. The major delays have been caused by the lack of support within the companies, probably in large part due to the relatively small anticipated production volume.

After a successful prototype is received, hopefully within 2 months, the question of the development of a monolithic will be re-opened.

X. ACKNOWLEDGEMENT

Many people from different laboratories have contributed to this project. It is hoped that the most important contributions have been mentioned at the beginning of this report. Particular credit should go to H. Steiner of Berkeley who initiated the first organization meeting; and F. Kirsten of Berkeley who authored the original specification.

XI. REFERENCES

1. "Multiwire Proportional Chambers. Preliminary Specifications for a Monolithic Integration of the Wire Electronics", Lawrence Radiation Laboratory, Berkeley, California, November 20, 1970.

TABLE I

SPECIFICATION SUMMARY

I. AMPLIFIER	
Input	- 5 mV to - 500 mV, negative; $T_F \sim 20$ nsec, $T_R \sim 200$ nsec
V_T	- 5 mV to - 100 mV ± 2 mV or ± 10%; T.C. 1%/°C 0° to 70°C
Positive signals	Insensitive to +500 mV signals
Protection	No damage for 100 pF at ± 5 KV through 2,000 Ω
Gain	4 mV change gives full output
Fast out	Width 30 ± 10 nsec, < 10 nsec T_R, T_F delay ≤ 40 nsec ± 20%
II. MONOSTABLE DELAY	
Output pulse	Adjustable 100 nsec to 10 μsec; T_R, $T_F \leq$ 10 nsec
Propagation delay	$T_{PD} \leq$ 40 nsec ± 20% from FAST out
Temp. Coeff. of width	< ± .05%/°C
External R C trim	Required
Power supply coeff. of width	≤ ± 1% for ± 10% change
Duty cycle	≤ 50%
III. GATED LATCH	
Minimum write gate width	≤ 20 nsec
Minimum coincidence curve	≤ 40 nsec
IV. GENERAL	
Outputs must be wire OR-able	
No unusual cooling requirements	
Direct out and gated out must be TTL compatible	
Operating range 0° to 70°C	

TABLE II

PROPOSAL SUMMARY

	Manufacturer	Hybrid	Fixed Cost	Production Cost	Monolithic Fixed Cost	Cost/Ch	Package	Comments
1.	Texas	x	$4.6K	$4.3/ch 5 mV	$40K	$2.5-3.25 (100K)	Mono- 16 pin DIP 1 or 2 ch Hybrid- 24 pin DIP 2 ch	Hybrid t_{pd} to fast out =55 ± 10 nsec >20 ns write gate required
2.	SESCOSEM				$38.7K	$2.34 (100K)	3 - 16 pin DIP's per 4 ch	
3.	Fairchild	x	0	$5.4 (100K) 1 mV			2 - 1.4" x 0.9" ceramic + plastic lid/4 ch	
4.	Motorola	TEDDY MECL	$7K	$10.37/ch (50K) 1 mV			1" x 1" ceramic per 2 ch	Not including MECL-TTL converter and output gates
5.	CERN (Phylips)	MECL		2.8 mV $5.8/ch (large Qty)			?	Data from Pizer/ Verweij
6.	CERN (GE Marconi)		$1.8K	$8/ch 50K			?	Data from Sauli via Kirsten

LIST OF FIGURES

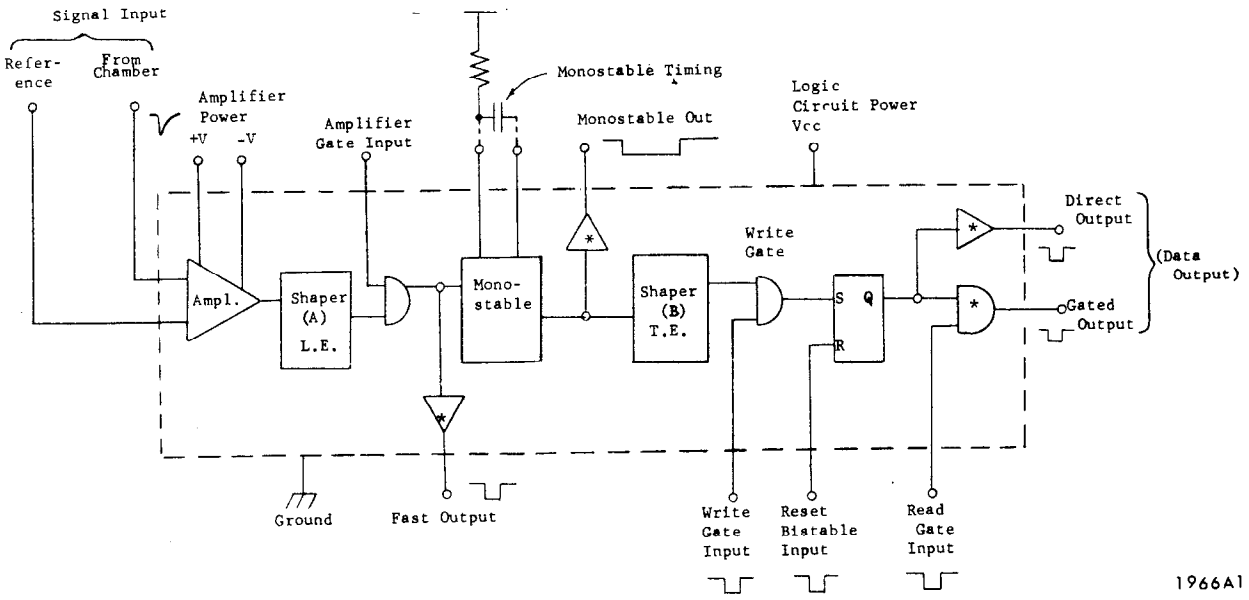

Signal Input
Refer-ence
From Chamber
Amplifier Power
+V
-V
Amplifier Gate Input
Monostable Timing
Monostable Out
Logic Circuit Power Vcc
Ampl.
Shaper (A) L.E.
Mono-stable
Shaper (B) T.E.
Write Gate
S
Q
R
Direct Output
Gated Output
(Data Output)
Ground
Fast Output
Write Gate Input
Reset Bistable Input
Read Gate Input
1966A1

Fig. 1

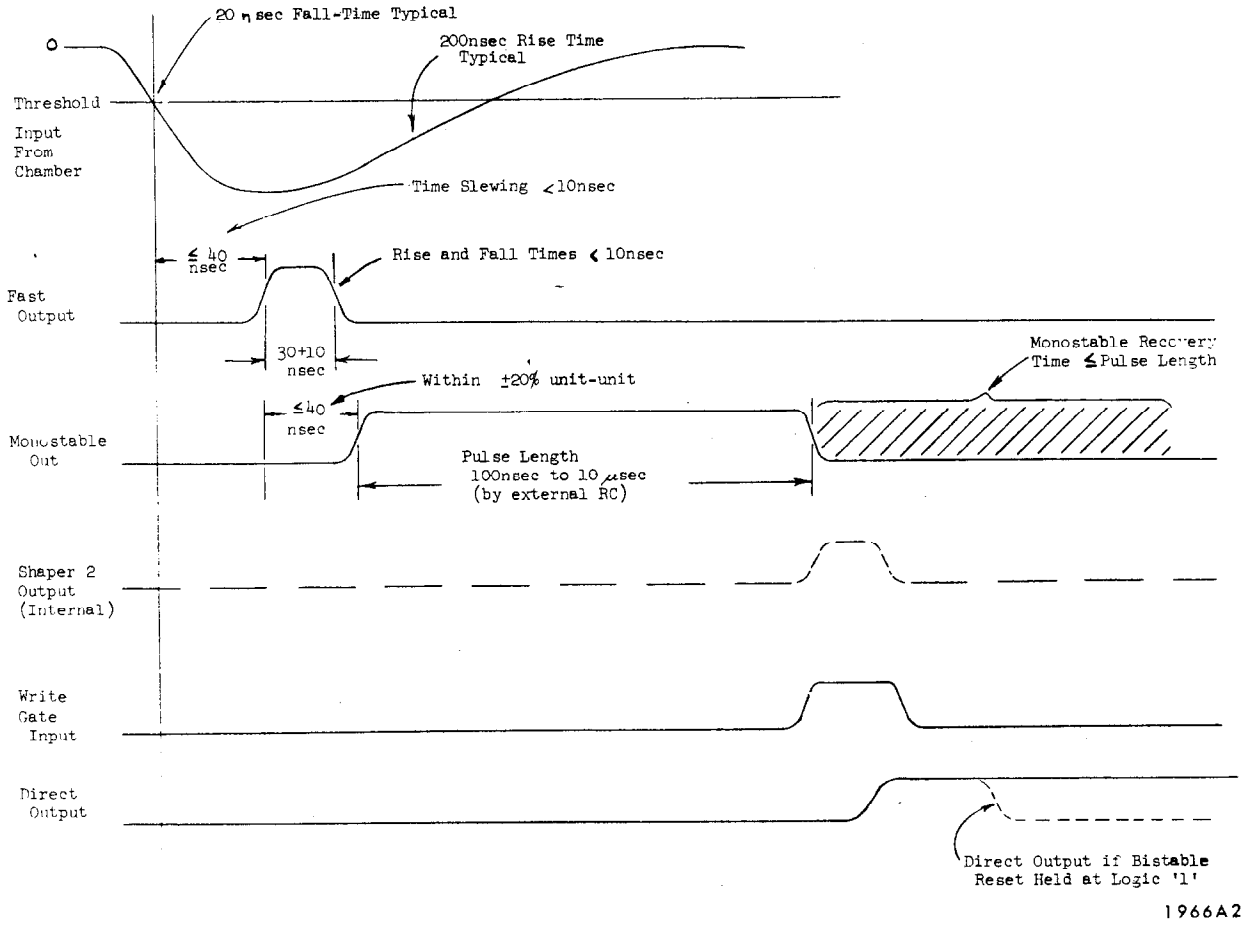
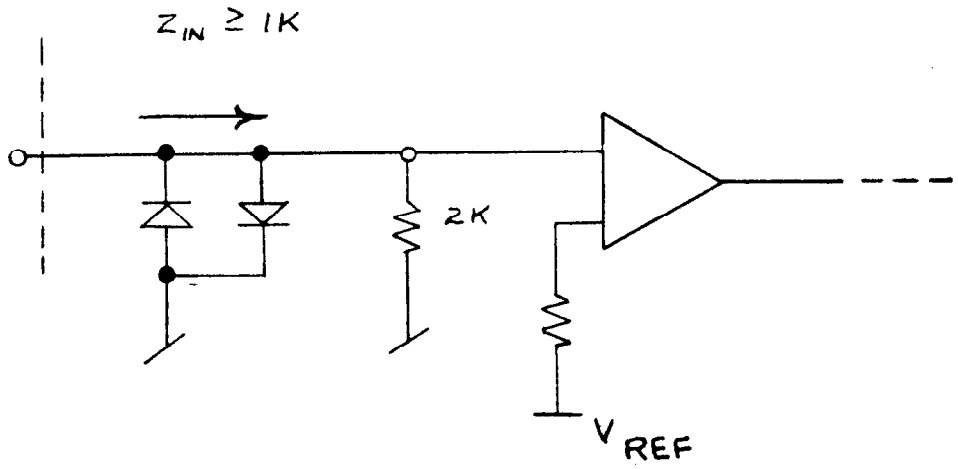
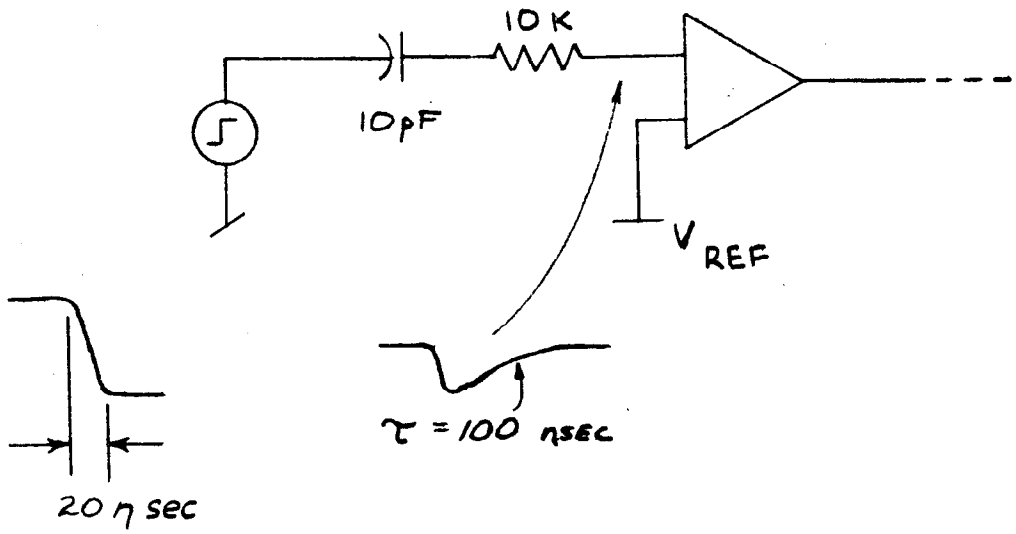

20 n sec Fall-Time Typical
0
200nsec Rise Time Typical
Threshold
Input From Chamber
Time Slewing < 10nsec
≤ 40 nsec
Rise and Fall Times < 10nsec
Fast Output
30+10 nsec
Monostable Recovery Time ≤ Pulse Length
Within ±20% unit-unit
≤40 nsec
Monostable Out
Pulse Length 100nsec to 10 μsec (by external RC)
Shaper 2 Output (Internal)
Write Gate Input
Direct Output
Direct Output if Bistable Reset Held at Logic '1'
1966A2

Fig. 2



(a)



(b)

1966A3

Fig. 3

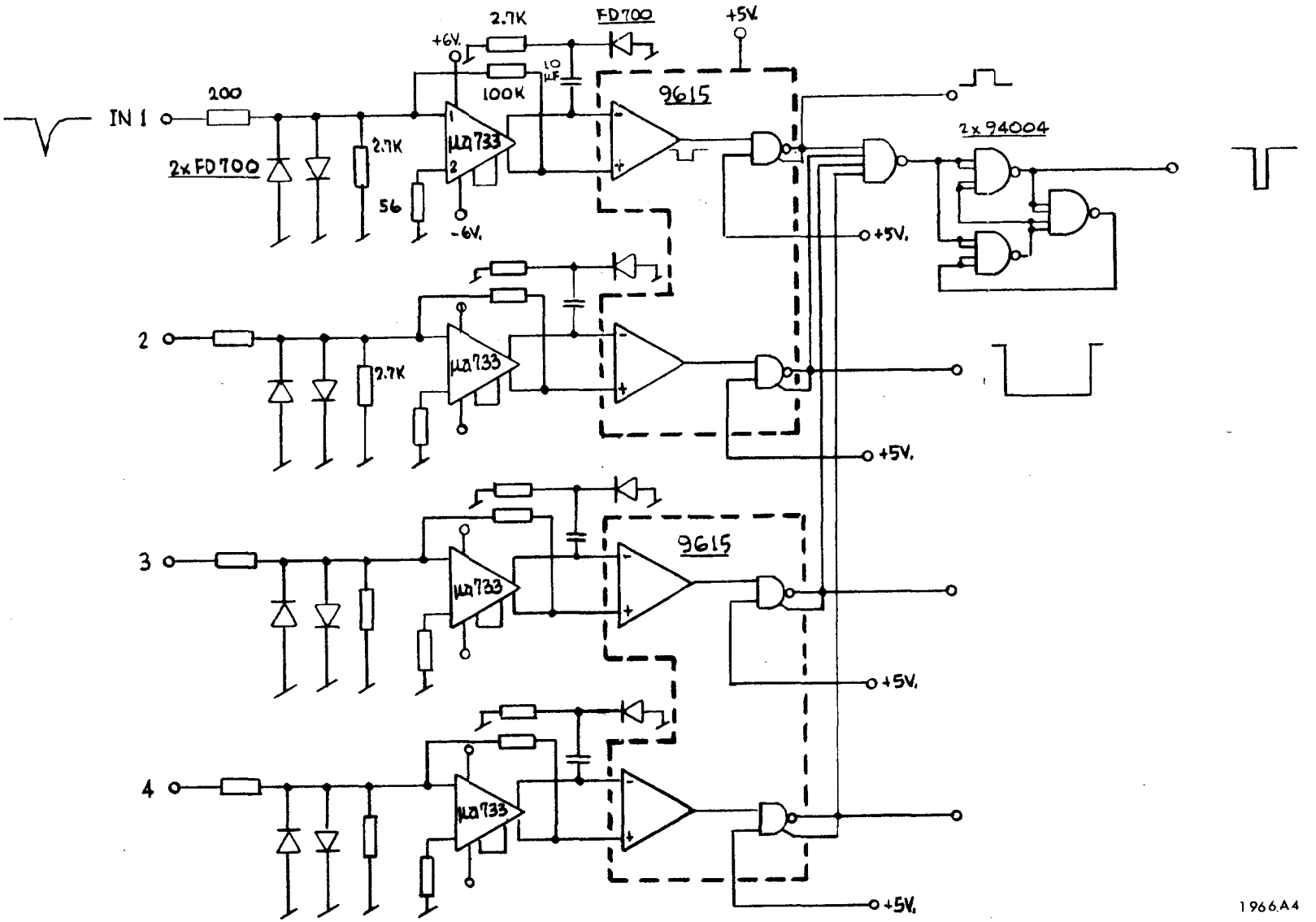

IN 1
200
2x FD700
2.7K
56
+6V.
-6V.
2.7K
100K
10 µF
FD700
+5V.
9615
µA733
2x 94004
+5V.
2
3
4
1966.A4

Fig. 4

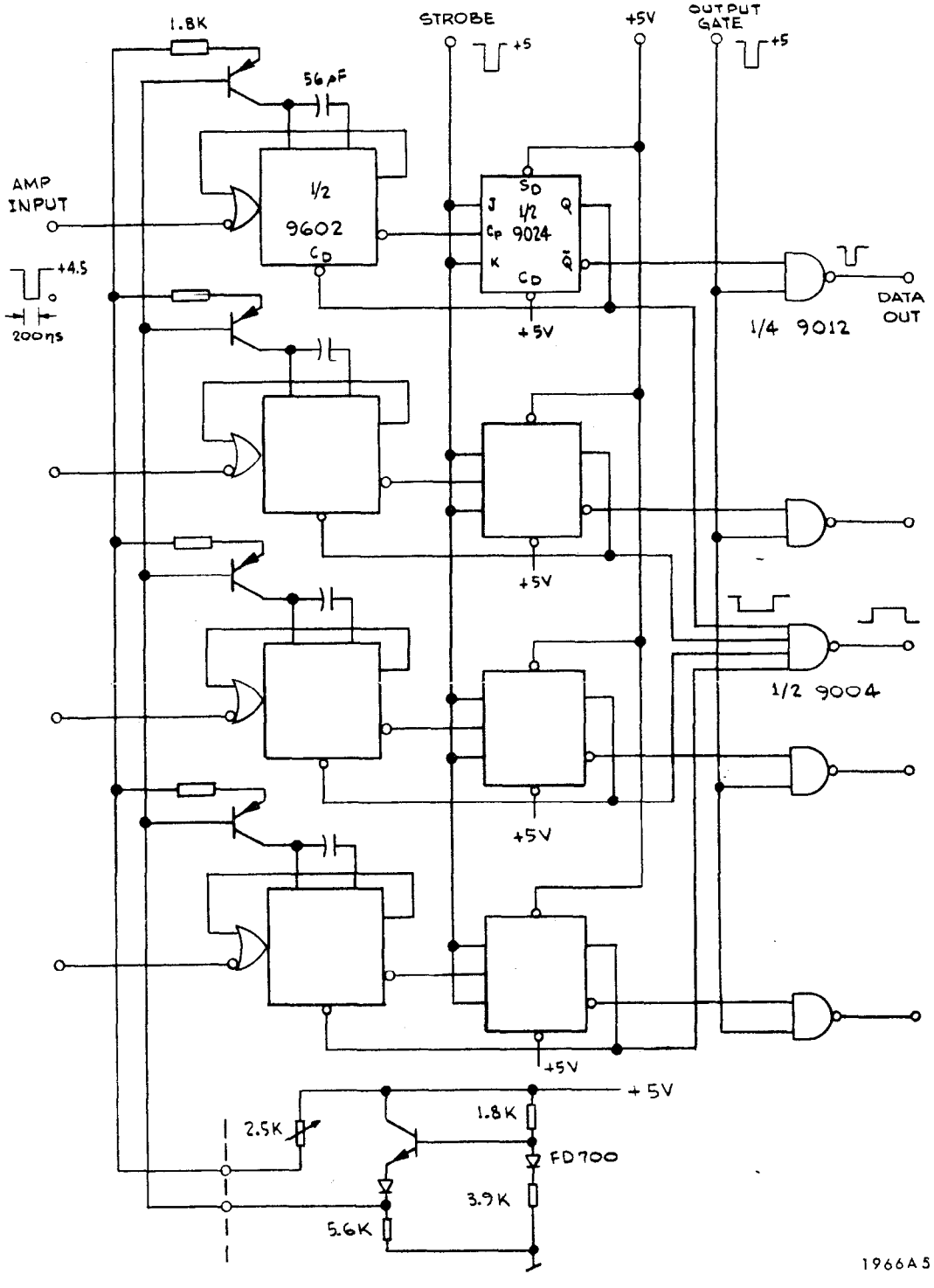

1.8K
STROBE
+5V
OUTPUT GATE
+5
56pF
1/2
9602
AMP INPUT
+4.5
200ns
1/2
9024
+5V
1/4 9012
DATA OUT
1/2 9004
2.5K
1.8K
FD700
3.9K
5.6K
1966A5

Fig. 5

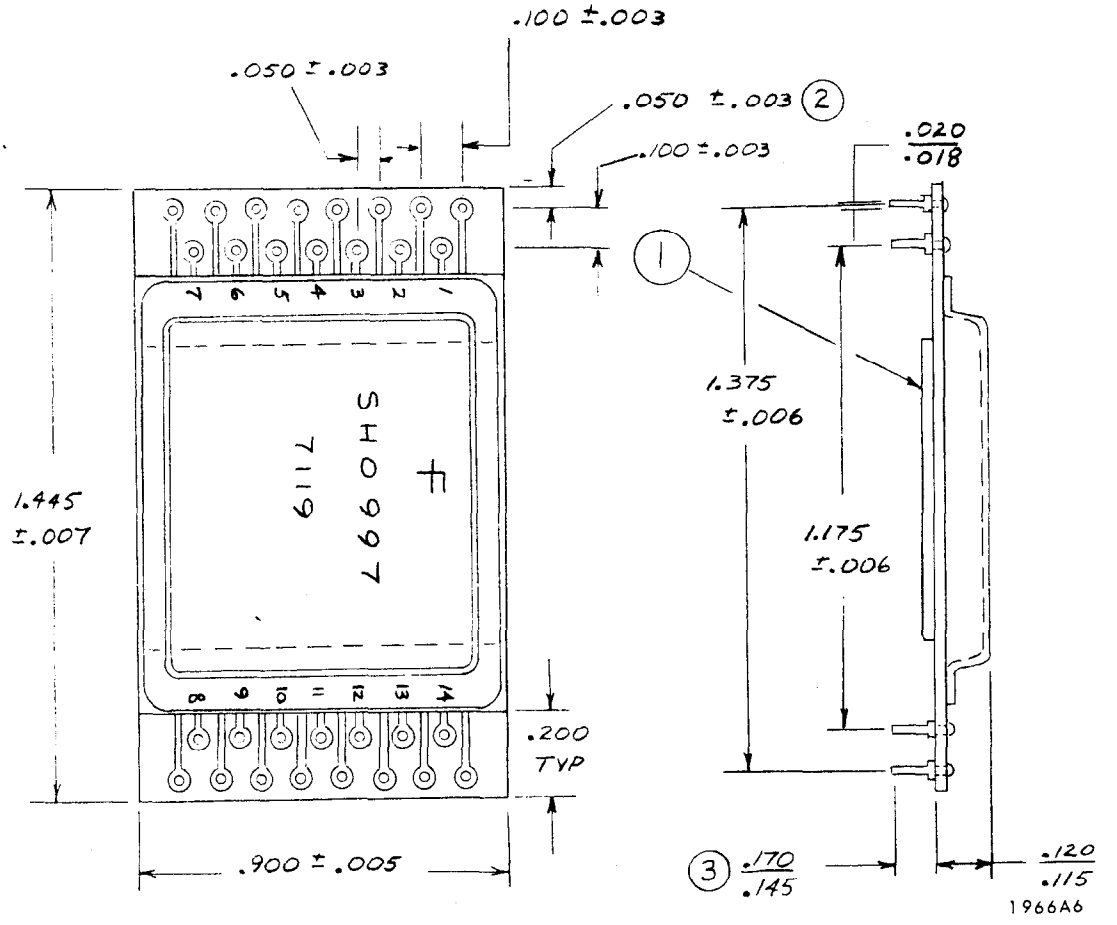

.100 ±.003
.050 ±.003
.050 ±.003
.100 ±.003
.020
.018
1.445
±.007
1.375
±.006
1.175
±.006
.200
TYP
.900 ±.005
.170
.145
.120
.115
1966A6

Fig. 6

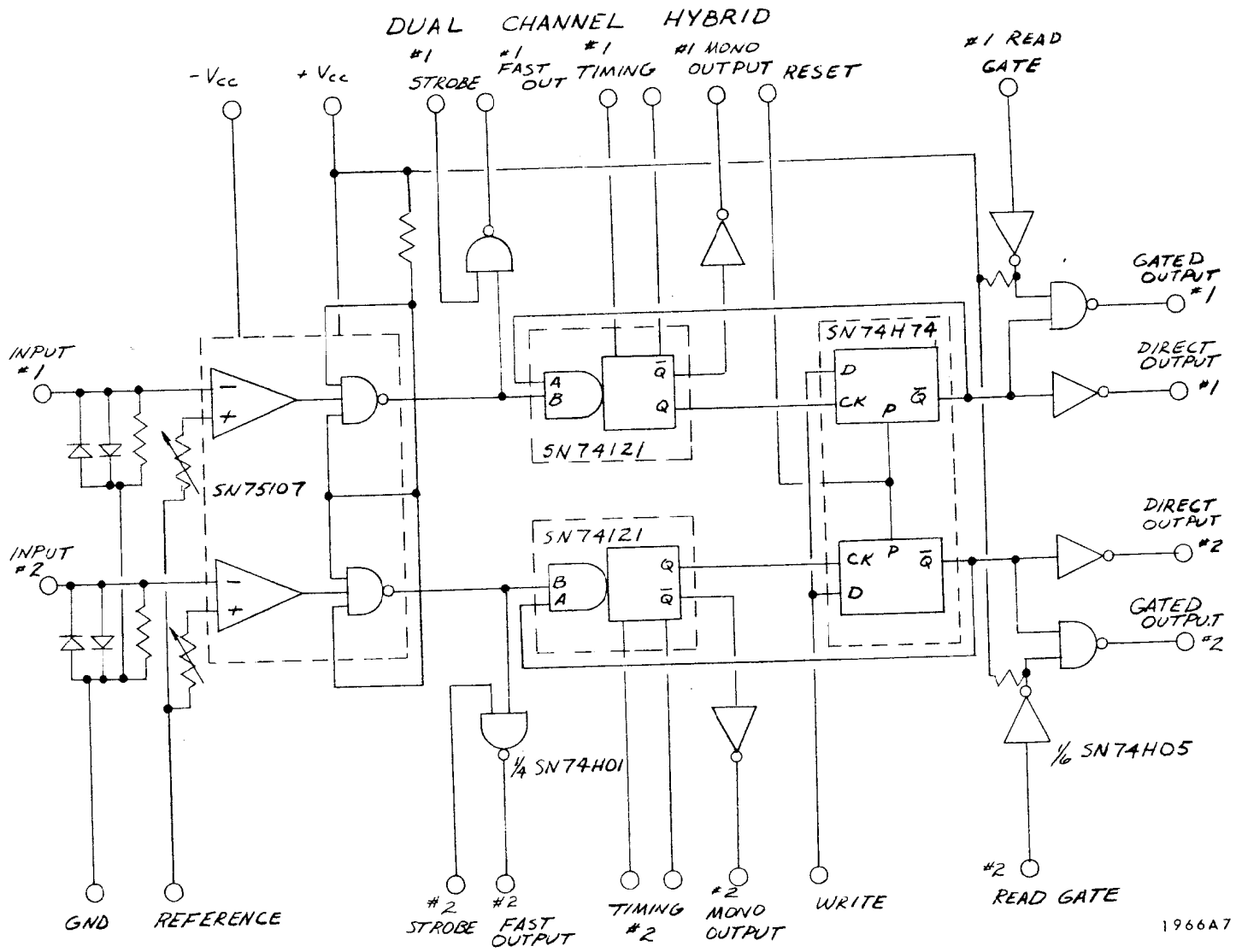
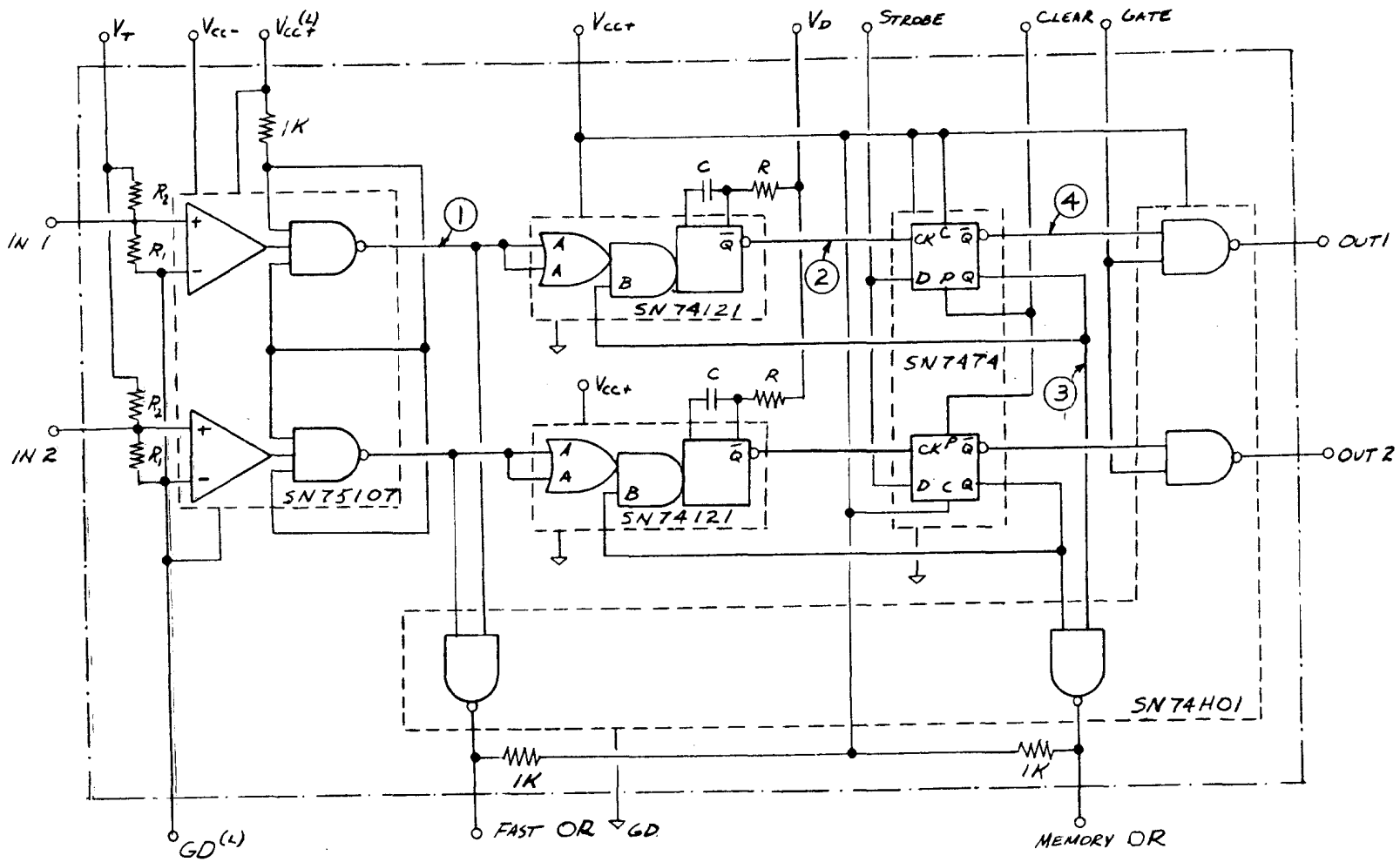

DUAL CHANNEL HYBRID
-Vcc
+Vcc
#1 STROBE
#1 FAST OUT
#1 TIMING
#1 MONO OUTPUT
RESET
#1 READ GATE
GATED OUTPUT #1
DIRECT OUTPUT #1
INPUT #1
SN75107
SN74121
SN74H74
INPUT #2
SN74121
DIRECT OUTPUT #2
GATED OUTPUT #2
1/4 SN74H01
1/6 SN74H05
GND
REFERENCE
#2 STROBE
#2 FAST OUTPUT
TIMING #2
#2 MONO OUTPUT
WRITE
#2 READ GATE
1966A7

Fig. 7



$V_{CC-} = -5V$
$V_{CC+} = +5V$
$V_T = +1V$
$V_D = V_{CC+}$ FOR 400 n sec

$R_1 = 2K\Omega$, 10%
$R_2 \simeq 90\ K\Omega$ (TRIM) [$60K < R_2 < 130K$]
$C = 150pF$
$R \simeq 2.7K\Omega$ (TRIM)

1966A8

Fig. 8